IP Core description

# axis\_red\_pitaya\_adc\_v3\_1 (for writing LTC2145-14)

Read analog data to axis bus interface.

Outputs:

* 32-Bit AXI4 Bus
  + m\_axis\_tvalid (Data available 🡪 transmit validation)
  + m\_axis\_tdata (Data)
* adc\_csn (chip select for ADC)

Inputs:

* aclk (Clock for analog measurement)
* adc\_dat\_a (Data 1. ADC)
* adc\_dat\_b (Data 2. ADC)

# axis\_red\_pitaya\_dac\_v2\_0 (for reading AD9767ASTZ)

Outputs:

* dac\_clk (clock [double frequency of conversion])
* dac\_rst (reset[disable clock input and reset state machine])
* dac\_sel (select channel[1🡪channel 1, 0🡪channel 2])
* dac\_wrt (write signal)
* dac\_dat (dac data)

Inputs:

* 32-Bit AXI4 Bus
  + s\_axis\_tvalid (transmit validation)
  + s\_axis\_tready (transmission ready) 🡨 output
  + s\_axis\_tdata (Data)
* aclk (Clock for analogue output)
* ddr\_clk (2xclock for analogue output)
* wrt\_clk (2xclock for analogue output)
* locked

# axis\_averager\_v1\_0

Stores nsemples samples with a sampling frequency of aclk, starting with the trig event and averages over naverages of these measurements.

Outputs:

* BRAM\_PORT\_A/ BRAM\_PORT\_B
  + bram\_porta\_clk (clock)
  + bram\_porta\_rst (reset)
  + bram\_porta\_addr (address of access)
  + bram\_porta\_wrdata (data writing)
  + bram\_porta\_rddata (data reading)
  + bram\_porta\_we (write enable)
* Finished (bit is set high if Measurement is finished)
* averages\_out (show actual measurement number)

Inputs:

* xx-Bit AXI4 Bus
  + s\_axis\_tvalid (transmit validation)
  + s\_axis\_tready (transmission ready) 🡨 output
  + s\_axis\_tdata (Data)
* aclk (clock)
* aresetn (reset core and Bram [0=reset; 1=nothing])
* user\_reset (reset Core and disable trigger [1=reset; 0=run])
* trig (trigger for next measurement start)
* nsemples (number of samples per measurement)
* naverages (number of measurements)

# axis\_bram\_writer\_v1\_0

Stores axis data every clock cycle as long as axis\_tvalid is set.

Outputs:

* BRAM\_PORT\_A
  + bram\_porta\_clk (clock)
  + bram\_porta\_rst (reset)
  + bram\_porta\_addr (address of access)
  + bram\_porta\_wrdata (data writing)
  + bram\_porta\_we (write enable)
* sts\_data (sample number equal bram\_porta\_addr)

Inputs:

* xx-Bit AXI4 Bus
  + s\_axis\_tvalid (transmit validation)
  + s\_axis\_tready (transmission ready) 🡨 output
  + s\_axis\_tdata (Data)
* aclk (clock)
* aresetn (reset core and Bram [0=reset; 1=nothing])