AEM10941 Evaluation Kit with PowerFilm Flexible PV Cell and CAP-XX Supercapacitor User Guide

Description

The AEM10941 is an ambient energy manager that extracts power from photovoltaic harvesters with high efficiency from 0.5V to 5V input voltage and simultaneously store energy in a rechargeable element and supply your system with two independent regulated voltages able to deliver up to 80 mA from 1.8 V to 4.5 V. It is able to coldstart with an input power as low as 3 µW at 380 mV.

The AEM10941 evaluation board with flexible solar cell allows users to test the e-peas IC and the **PowerFilm** PV cell and analyse its performances in a laboratory-like setting. It allows easy connections to the CAP-XX supercapacitor and the low voltage and high-voltage loads. It also provides all the configuration access to set the device in any one of the modes described in the datasheet. The control and status signals are available on standard pin headers, allowing users to configure it for any usage scenario and evaluate the relevant performances.

The AEM10941 evaluation board with **PowerFilm** flexible solar cell and CAP-XX supercapacitor is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes, etc) for the design of a highly efficient subsystem in your target application.

Applications

PV cell harvesting	Home automation
Industrial monitoring	E-health monitoring
Geolocation	Wireless sensor nodes

Device Information

Part Number	Dimensions
2EAEM10941C0011	27.94 mm x 27.94 mm
LL200-2.4-37	54 mm x 36.5 mm
MPT2.4-21	54 mm x 20.9 mm
Li-ion battery	10 mm x 23 mm x 4 mm
DMT3N4R2U224M3DTA0	21 mm x 14 mm
DMF3Z5R5H474M3DTA0	21 mm x 14 mm

Features

Two-way screw terminals

- Source of energy (PV cell)
- Primary battery
- High-voltage load
- Low-voltage load

Three-way screw terminals

- Custom mode configuration

3-pin headers

- Energy storage element threshold configuration (CFG[2:0])
- Low drop-out regulators (LDOs) enabling
- Dual-cell supercapacitor configuration

One 2-pin header

- Primary battery configuration

Provision for five resistors

- Custom mode configuration
- Cold-start configuration
- Primary battery configuration

POWERFILM PV Modules

- Sample modules produces up to 1 mW indoors and 68 mW outdoors
- Thin-film materials assembled on flexible plastic substrate
- Custom size, power and configurations available

CAP-XX supercapacitor

- Provision for DMT, DMH, DMF and GA packages
- 4.2 V and 5.5 V Dual-cell supercapacitors
- Up to 1 F capacity

Appearance

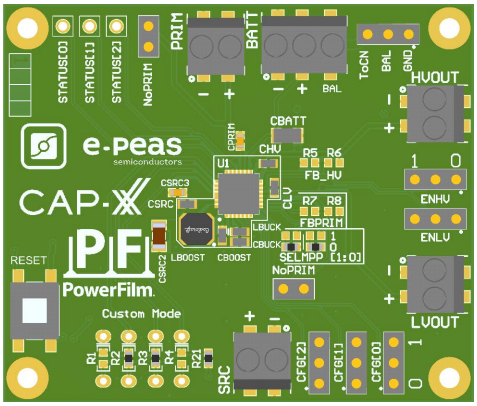


Figure 1: 2EAEM10941C0011

Figure 4: Li-ion battery

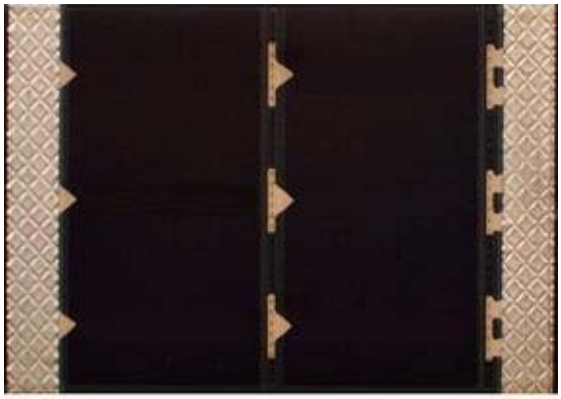


Figure 2: LL200-2.4-37

Figure 5: DMT3N4R2U224M3DTA0

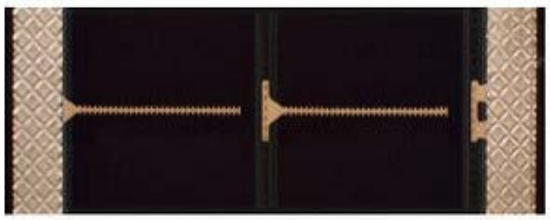


Figure 3: MPT2.4-21

Figure 6: DMF3Z5R5H474M3DTA0

1. Connections Diagram

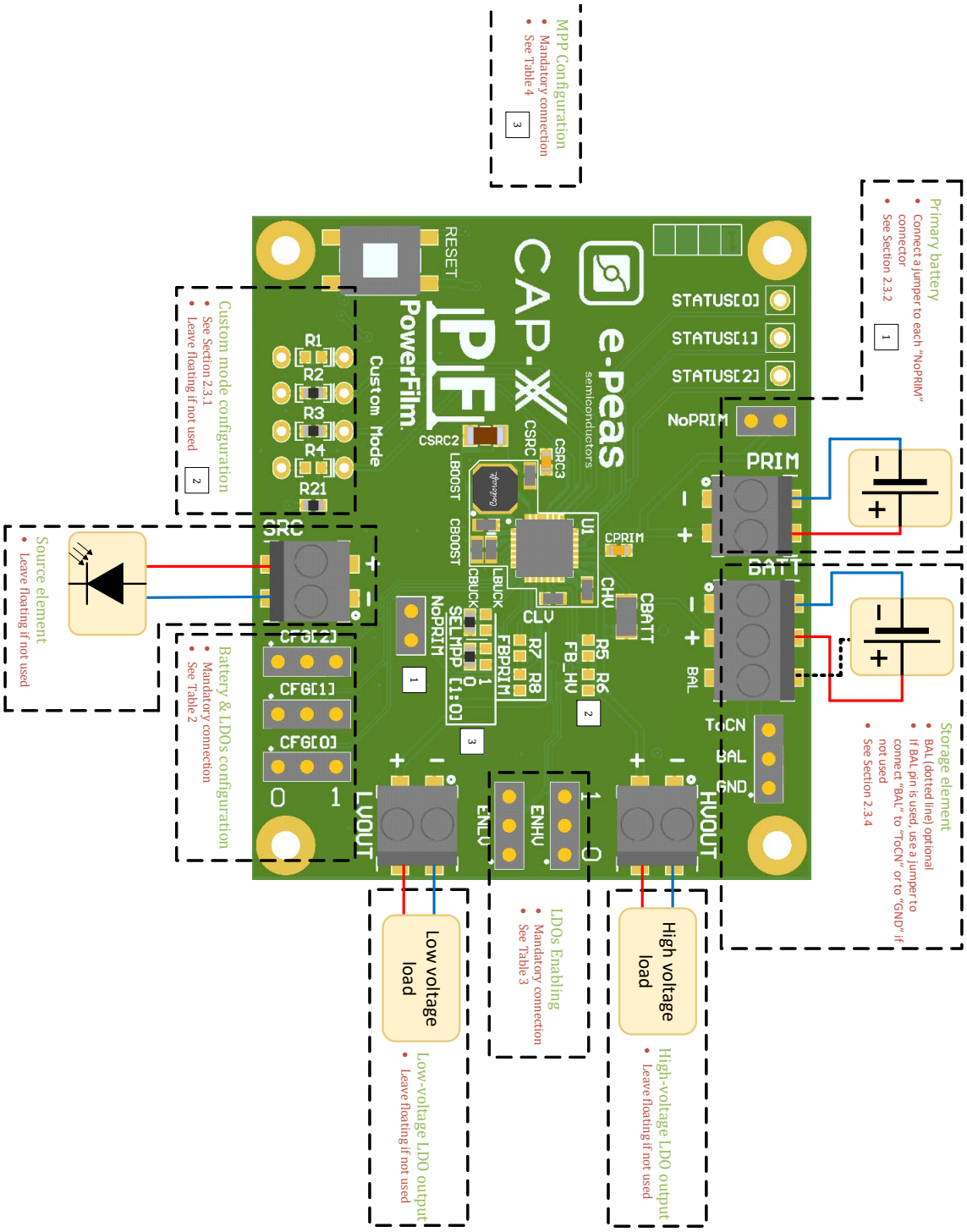


Figure 1: Connection diagram

1.1. Signals Description

NAME	FUNCTION	CONNECTION	
		If used	**If not used**
Power signals			
SRC	Connection to the harvested energy source.	Connect the source element.	Leave floating.
BATT	Connection to the energy storage element.	Connect the storage element in addition to CSTO (150 µF).	Do not remove CBATT
BAL	Connection to mid-point of a dual-cell supercapacitor	Leave R30 empty.	Use R30 to connect "BAL" to "GND"
PRIM	Connection to the primary battery	Connect primary battery and remove R26	Use R26 to connect "PRIM" to "GND"
LVOUT	Output of the low-voltage LDO regulator.	Connect a load	
HVOUT	Output of the high-voltage LDO regulator.	Connect a load	
Configuration signals			
CFG[2:0]	Configuration of the threshold voltages for the energy storage element.	Connect jumpers (see Table 2)	Cannot be left floating.
SELMPP[1:0]	Configuration of the MPP ratio.	Connect with 0 Ω resistor (see Table 4).	Cannot be left floating.
FB_PRIM	Configuration of the primary battery.	Use resistors R7-R8 and jumpers (see Section 2.4.2).	Leave R8 empty.
FB_HV	Configuration of the high-voltage LDO in the custom mode	Use resistor R5-R6 (see Section 2.4.1).	Leave R5-R6 empty.
Control signals			
ENHV	Enabling pin for the high-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating.
ENLV	Enabling pin for the low-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating.
Status signals			
STATUS[2]	Logic output. Asserted when the AEM performs the MPP evaluation.	May be connected to a monitoring circuit	Can be left floating
STATUS[1]	Logic output. Asserted if the battery voltage falls under Vovdis or if the AEM is taking energy from the primary battery.	May be connected to a monitoring circuit	Can be left floating
STATUS[0]	Logic output. Asserted when the LDOs can be enabled.	May be connected to a monitoring circuit	Can be left floating

Table 1: Pin description

2. General Considerations

2.1. Safety Information

Always connect the elements in the following order:

1. Reset the board - see Section 2.2 “Reseting the board”.
2. Completely configure the PCB (resistors);

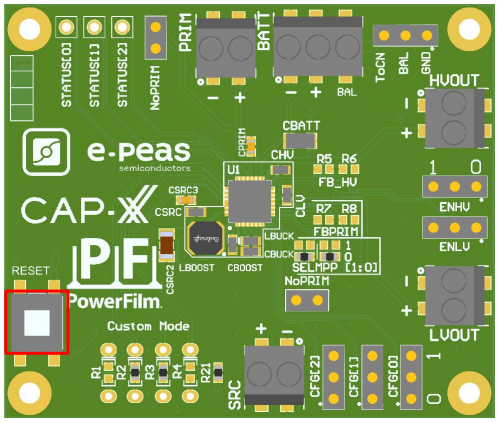
   MPP configuration (SELMPP[0], SELMPP[1] - see Table 4,
   Battery and LDOs configuration (CFG[2:0] and, if needed, R1-R2-R3-R4-R5-R6) - see Table 2,
   Primary battery configuration (R7-R8) - see Section 2.4.2,
   LDOs enabling (ENHV and ENLV) -Section 2.3,
   Balun circuit connection (BAL) - see Section 2.4.4,
3. Connect the storage elements on BATT and optionally the primary battery on PRIM.
4. Connect the high and/or low voltage loads on HVOUT/LVOUT (optional).
5. Connect the source on SRC.

To avoid damage to the board, users are urged to follow this procedure. To store the board, disconnect SRC and the load. Disconnect the storage element (if possible) and reset the board.

2.2. Reseting the board

How to reset the AEM10941 evaluation board:

To reset the board, simply disconnect the source and the optional primary battery and briefly press the “RESET” button.



2.3. Basic Configurations

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V_{OVCH}	V_{CHRDY}	V_{OVDIS}	V_{HV}	V_{LV}	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Custom mode - see Section 2.3.1				1.8 V	

Table 2: Usage of CFG[2:0]

ENLV	ENHV	LV output	HV output
H	H	Enabled	Enabled
H	L	Enabled	Disabled
L	H	Disabled	Enabled
L	L	Disabled	Disabled

Table 3: LDOs enabling

SELMPP[1]	SELMPP[0]	Vmpp/Voc
L	L	70%
L	H	75%
H	L	85%
H	H	90%

Table 4: Usage of SELMPP[1:0]

2.4. Advanced Configurations

A complete description of the system constraints and configurations is available in Section 8 “System configuration” of the AEM10941 datasheet.

A reminder on how to compute the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found at the e-peas website.

2.4.1. Custom mode

In addition to the pre-defined protection levels, the custom mode allows users to define their own levels via resistors R1 to R4 and to tune the output of the high voltage LDO via resistors R5-R6. The custom mode is accessible via the configuration 000 and the removal of resistor R21.

By defining RT = R1 + R2 + R3 + R4 (1MΩ ≤ RT ≤ 100 MΩ):

R1 = RT (1V / V_{OVCH})
R2 = RT (1V / V_{CHRDY} - 1V / V_{OVCH})
R3 = RT (1V / V_{OVDIS} - 1V / V_{CHRDY})
R4 = RT (1 - 1V / V_{OVDIS})

By defining RV = R5 + R6 (1MΩ ≤ RV ≤ 40MΩ):

R5 = RV (1V / V_{HV})
R6 = RV (1 - 1V / V_{HV})

Make sure the protection levels satisfy the following conditions:

V_{CHRDY} + 0.05 V ≤ V_{OVCH} ≤ 4.5 V
V_{OVDIS} + 0.05 V ≤ V_{CHRDY} ≤ V_{OVCH} - 0.05 V
2.2 V ≤ V_{OVDIS}
V_{HV} ≤ V_{OVDIS} - 0.3V

If unused, leave the resistor footprints (R1, R4, R5 and R6) empty.

2.4.2. Primary battery configuration

If the primary storage is used, its battery protection levels have to be defined. To do so, use resistors R7 - R8. Please add a 1 µF capacitor in parallel with the primary battery too. This capacitor must remain connected to the circuit at all time.

By defining RP = R7 + R8 (100 kΩ ≤ RP ≤ 10MΩ):

R7 = $V_{PRIM,MIN}$ / 4 * RP * 1 / 2.2 V
R8 = RP - R7

If unused, leave resistor R29 in place.

2.4.3. Cold-start configuration

The cold-start voltage Vcs (i.e. the voltage needed at startup to turn on the AEM10941) is by default at its minimum value of 380mV. This voltage can be increased by the use of resistors R9-R10.

By defining RC = R9 + R10 (100kΩ ≤ RC ≤ 10MΩ):

R9 = 0.38V * RC / Vcs
R10 = RC - R9

If unused, do not mount resistors R9-R10.

2.4.4. Balun circuit configuration

When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balun circuit configuration to ensure equal voltage on both cells. To do so:

Connect the node between the two supercapacitor cells to BAL (BATT connector)
Remove resistor R30

If unused, leave resistor R30 in place.

3. Powerfilm PV cells

PowerFilm designs and manufactures custom solar cells, modules, panels and power solutions for energy harvesting and portable power applications using proprietary thin-film silicon technology. In business for over 30 years, we continue to provide a wide range of rugged, high-performance solutions across IoT, Transportation, military, and consumer markets.

Our proprietary PV material is inherently sensitive to collecting low intensity light, making it ideal for low power indoor/outdoor IoT and energy harvesting applications where light conditions are always changing. Indoor Series panels have excellent performance under artificial lighting, whether that is a dim warehouse (200 lux) or a bright retail store (1000 lux). Classic application panels are optimized for collecting outdoor light directly from the sun or indirectly in shaded areas.

Starting with polyimide plastic, our panels are manufactured using high throughput, roll-to-roll processes. With only simple adjustments, we can print solar cells and modules in many different custom sizes and configurations, helping our customers solve IoT power problems in innovative ways.

Cell name	Illuminance	Vmax (V)	Imax(µA)	Vop (V)	Iop (µA)	Pop (µW)
LL200-2.4-37	200 lux	2.4	60	1.6	43	69
	1000 lux	2.7	200	2.1	214	449
MPT2.4-21	1/4 sun	3.2	4000	2.4	3200	7680
	1 sun	3.5	16500	2.7	14200	38340

Table 5: PowerFilm PV Modules. Vop, Iop, and Pop represent guaranteed minimum performance. Other listed values are average or typical behavior. All panels are tested for performance under a cool white LED spectrum.

Supercap Charge Time			220mF DMT3N4R2U224M3DTA0		470mF DMF3Z5R5H474M3DTA0	
	Illuminance	PV Module	Cold-Start (0-3.6V)	Normal Operation [h] (3-4.12V)	Cold-Start (0-3.6V)	Normal Operation [h] (3-4.12V)
Warehouse	200 Lux	2x LL200-2.4-37	4.00	2.00	8.54	4.27
Bright Retail Store	1000 Lux	LL200-2.4-37	0.80	0.40	1.71	0.85
Shaded Outdoors	1/4 Sun	MPT2.4-37	0.08	0.04	0.16	0.09
Direct Sunlight	1 Sun	MPT2.4-37	0.02	0.01	0.04	0.02

Table 6: Expected behevior based on minimum PV performance specification with 90% charge efficiency

4. Cap-xX supercapacitors

CAP-XX is a world leader in the design and manufacture of thin, flat supercapacitors and energy management systems used in portable and small-scale electronic devices.

The unique feature of CAP-XX supercapacitors is their very high power density and high energy storage capacity in a space-efficient prismatic package. These attributes are essential in power-hungry consumer and industrial electronics, and deliver similar benefits in automotive and other transportation applications.

Voltage (V)	Capacitance (mF)	ESR (mΩ)	Dimensions (mm)	Height (mm)	Part name
4.2	220	300	21 x 14	2.2	DMT3N4R2U224M3DTA0
4.5	35	300	20 x 20	0.4	DMHA14R5V353M4ATA0
5.5	470	45	25.5 x 14	0.2	DMF3Z5R5H474M3DTA0
5.5	1000	40	30 x 14	3.7	DMF4B5R5G105M3DTA0

Table 7: Cap-xX supercapacitors

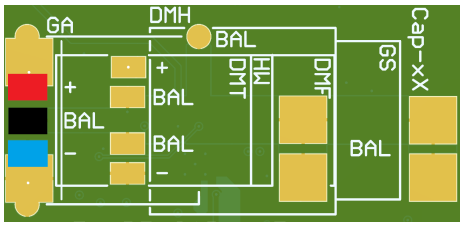
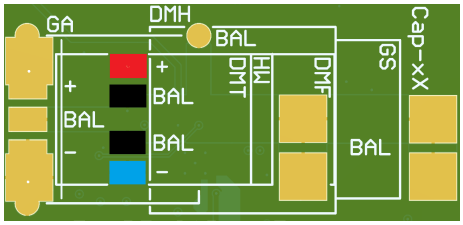
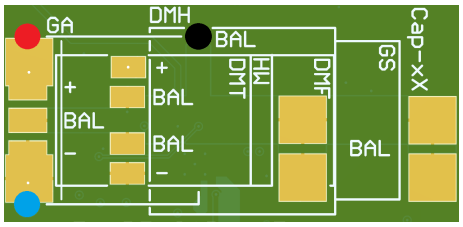
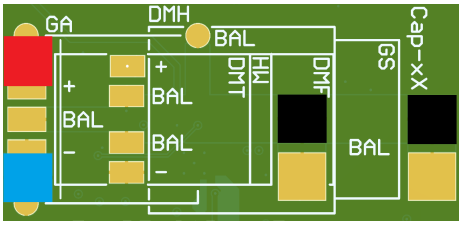
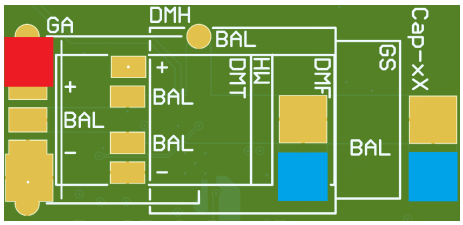
Package name	Footprint	Comment
DMF/DMT		Use Jumper to Connect “BAL” to “ToCN”
DMH		Use Jumper to Connect “BAL” to “ToCN”
A		Use Jumper to Connect “BAL” to “ToCN” This model is not delivered in this evaluation kit
Dual cell S/W		Use Jumper to Connect “BAL” to “ToCN” This model is not delivered in this evaluation kit
Single cell S/W		Use Jumper to Connect “BAL” to “GND” To fit on the board, the supercapacitor must be flipped on its back This model is not delivered in this evaluation kit

Table 8: Footprint description

This footprint is available on the inferior face of the PCB. The red colour represents the positive voltage, the blue is the ground and the black is to be connected to the balancing pin. Those three potentials are available on the screw terminal on the top side.

5. Functional Tests

This section presents a few simple tests that allow the user to understand the functional behaviour of the AEM10941. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety Information”. If a test has to be restarted make sure to properly reset the system to obtain reproducible results.

The following functional tests were made using the following setup:

Configuration: SELMPP[1:0] = LL, CFG[2:0] = HLL, ENHV = H, ENLV = H
Storage element: Capacitor (4.7 mF + CBATT)
Load: 10kΩ on HVOUT, LVOUT floating
SRC: current source (1mA or 100µA) with voltage compliance (4V)

Feel free to adapt the setup to match your system as long as you respect the input and cold-start constraints (see Section 1 “introduction” of AEM10941 datasheet).

5.1. Start-up

The following example allows users to observe the behaviour of the AEM10941 in the wake-up mode.

Setup

Place the probes on the nodes to be observed.
Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”.

Observations and measurements

BATT: Voltage rises as the power provided by the source is transferred to the storage element (see Figure 2).
SRC: Regulated at Vmpp, which is a voltage equal to the open-circuit voltage (Voc) times the MPP ratio defined in Table 4. Vsrc equals Voc during MPP evaluation (see Figure 3). Note that Vsrc must be higher than 380 mV to coldstart.
HVOUT/LVOUT: regulated when voltage on BATT first rises above Vchrdy (see Figure 2).
STATUS[0]: Asserted when the LDOs are ready to be enabled (see Figure 2).
STATUS[2]: Asserted each time the AEM10941 performs a MPP evaluation (See Figure 3).

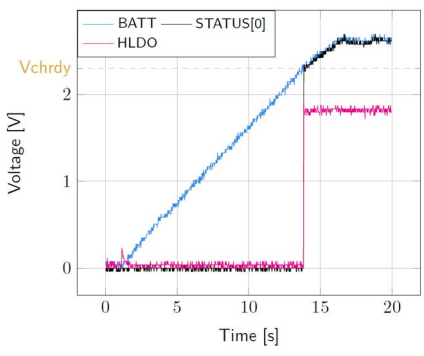


Figure 2: STATUS[0] and HVOUT evolution with BATT

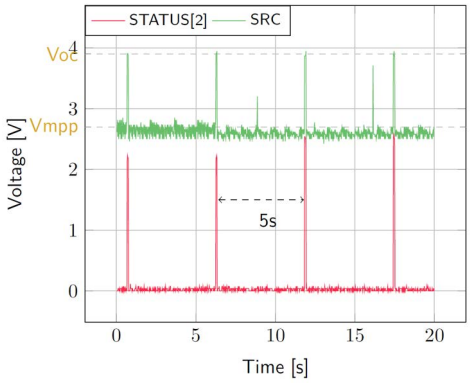


Figure 3: SRC and STATUS[2] while energy is extracted from SRC (BATT under V_{OVCH})

5.2. Shutdown

This test allows users to observe the behaviour of the AEM10941 when the system is running out of energy.

Setup

Place the probes on the nodes to be observed.
Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1). Do not use a primary battery.
Let the system reach a steady state (i.e. voltage on BATT between V_{CHRDY} and V_{OVCH} and STATUS[0] asserted).
Remove the Dracula PV cell and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and measurements

BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage remains stable after crossing V_{OVDIS} (see Figure 4).
STATUS[0]: De-asserted when the LDOs are no longer available as the storage element is running out of energy. This happens 600 ms after STATUS[1] assertion (see Figure 4).
STATUS[1]: Asserted for 600ms when the storage element voltage (BATT) falls below V_{OVDIS} (see Figure 4).

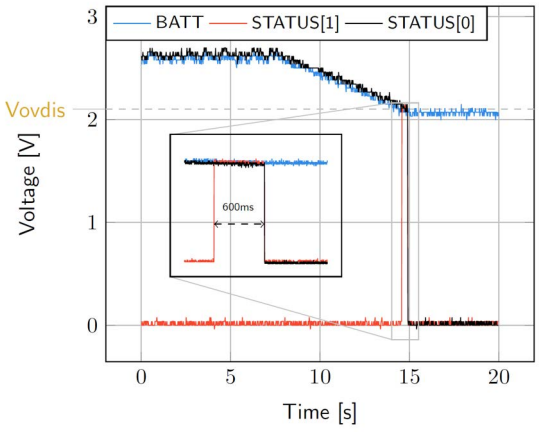


Figure 4: LDOs disabled around 600 ms after BATT reaches Vovdis

5.3. Switching on primary battery

This example allows users to observe switching from the main storage element to the primary battery when the system is running out of energy.

Setup

Place the probes on the nodes to be observed.

Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 "Safety Information". Configure the board in the desired state and start the system (see Section 3.1). Connect a primary battery (example: 3.1V coin cell with protection level at 2.4V, R7 = 68kΩ and R8 = 180kΩ).

Let the system reach a steady state (i.e. voltage on BATT between V_{CHRDY} and V_{OVDIS} and STATUS[0] asserted).

Remove the PV cell and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and measurements

BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches V_{OVDIS} and than rises again to BATT as it is recharged from the primary battery (see Figure 5).

STATUS[0]: Never de-asserted as the LDOs are still functional (see Figure 5).

HVOUT: Stable and not affected by switching on the primary battery (see Figure 5).

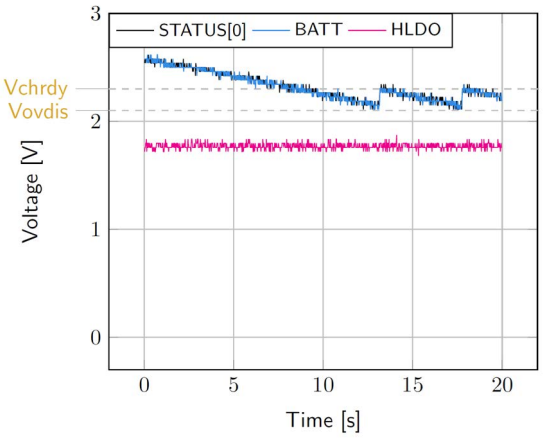


Figure 5: Switching from SRC to the primary battery

5.4. Cold start

The following test allows the user to observe the minimum voltage required to coldstart the AEM10941. To prevent leakage current induced by the probe the user should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behaviour.

Setup

Place the probes on the nodes to be observed.

Referring Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state. Connect to FB_COLD. Do not plug any storage element in addition to CBATT.

SRC: Connect your source element.

Observations and measurements

SRC: Equal to the cold-start voltage during the coldstart phase. Regulated at the selected MPPT percentage of V_{OC} when cold start is over. (See Figure 6). Be careful that the cold-start phase time will shorten with the input power. Limit it to ease the observation.

BATT: Starts to charge when the cold-start phase is over (see Figure 6).

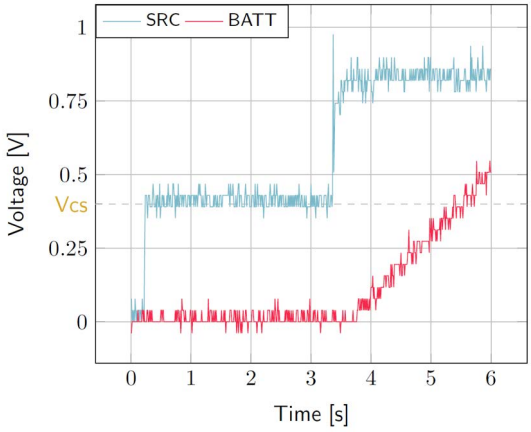


Figure 6: AEM10941 behaviour during cold start

5.5. Dual-cell supercapacitor balancing circuit

The following test allows the user to observe the balancing circuit behaviour that balances the voltage on both side of the BAL pin.

Setup

Following steps 1 and 2 explained in section 2.1 and referring to Figure 1, configure the board in the desired state. Disconnect the resistor R30.

BATT: Plug capacitor C1 between the positive (+) pin and the bal pin, and a capacitor C2 between the BAL pin and the negative (-) pin.

- C1 & C2 > 1 mF
- (C2 * V_{CHRDY}) / C1 ≥ 0.9V

SRC: Plug your source element to power up the system.

Observations and measurements

BAL: equal to half the voltage on BATT.

Warning regarding measurements:

Any item connected to the PCB (load, probe, storage device, etc.) involves a leakage current. This can negatively impact the measurements. Whenever possible, disconnect unused items to limit this effect.

6. Performance Tests

This section presents the tests to reproduce the performance graphs found in the AEM10941 datasheet and to understand the functionalities of the AEM10941. to be able to reproduce those tests, you will need the following:

1 voltage source
2 source measure units (SMUs)
1oscilloscope

To avoid damaging the board, follow the procedure in Section 2.1 “Safety information”. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results.

6.1. LDOs

The following example instructs users on how to measure the output voltage stability of the LDOs (Figure 16 and Figure 17 of the AEM10941 datasheet).

Setup

Referring to Figure 1, follow steps 1 and 2 explained in the section 2.1. Configure the board in the desired state and plug your storage element(s)
VBOOST: connect SMU1. configure it to source voltage with a current compliance of 200 mA.
HVOUT / LVOUT: connect SMU2 to the LDO you want to measure. Configure it to sink current with a voltage compliance of 5V for HVOUT or 2.5V for LVOUT.

Manipulations

Impose a voltage between V_{OVCH} and 5V on SMU 1 to force the AEM to start.
Sweep voltage on SMU1 from V_{OVDIS} + 50 mV to 4.5 V
Repeat with different current levels on SMU2 (from 10µA to 80mA for HVOUT and from 10µA to 20mA for LVOUT).

Measurements

HVOUT/LVOUT: Measure the voltage.

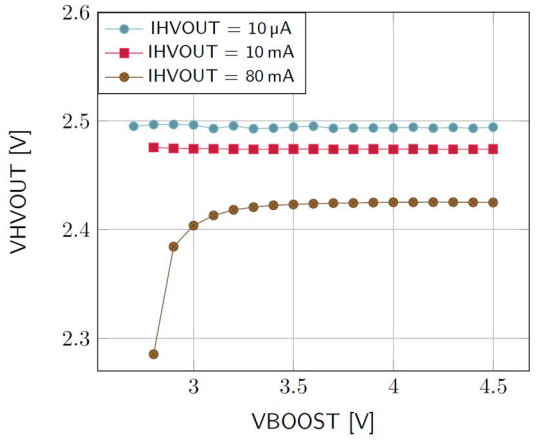


Figure 7: HVOUT at 2.5V

6.2. BOOST efficiency

This test allows users to reproduce the efficiency graphs of the boost converter (Figure 14 of the AEM10941 datasheet).

Setup

Following steps 1 and 2 explained in the section 2.1 and referring to Figure 1, configure the board in the desired state.
VBUCK: Connect a 2.3 V voltage source to prevent VBUCK to sink from VBOOST.
SRC (: Connect SMU1. Configure it to source current with a voltage compliance of 0 V.
VBOOST: Connect SMU2. Configure it to source voltage with a current compliance of 200 mV
STATUS[2] Connect to one of the SMU to detect falling edge.

Manipulations

Impose a voltage between V_{OVCH} and 5V on SMU 2 to force the AEM to start. When done, impose a voltage between V_{OVDIS} + 50mV and V_{OVCH}.
Sweep voltage compliance on SMU1 from V_{OVDIS} + 50 mV to 4.5 V
Repeat with different current levels on SMU1 (from 100µA to 100mA) and with different voltage levels on SMU2 (from V_{OVDIS} + 50 mV to V_{OVCH}).

Measurements

STATUS[2]: Dot not make any measurements while high (boost converter is not active during MPP calculation).
SRC: Measure the current and the voltage.

VBOOST: Measure the current and the voltage. Repeat the measurement a copious number of times to be sure to capture the current peaks. Figure 8 has been obtained by averaging over 100 measurements configured with a 100 ms integration time.

Deduce input and output power (P = U x I) and efficiency (η = Pout/Pin).

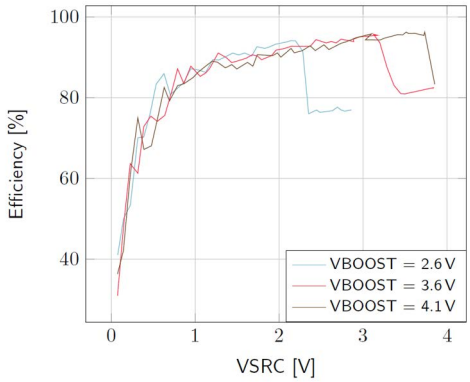


Figure 8: Boost efficiency for ISRC = 1mA

6.3. Custom mode configuration

This test allows users to measure the custom protection levels of the storage element set by resistors R1 to R6.

Setup

Referring to Figure 1, follow steps 1 and 2 explained in Section 2.1. Connect CFG[2:0] = LLL to select custom mode, remove R2, R3 and R25 and choose R1 to R6 to configure the battery protection levels and HVOUT output voltage.

Place the probes on the nodes to be observed.

SRC: connect your source element to power up the system.

Manipulations

Remove the source element after the voltage on BATT has reached steady state (between V_{CHRDY} and V_{OVCH}).

Measurements

Measure the following nodes to ensure the correct behaviour of the AEM10941 with respect to the custom configuration:

STATUS[0]: Asserted when the LDOs can be enabled (i.e. when BATT first rises above V_{CHRDY}).

STATUS[1]: Asserted when BATT falls below V_{OVDIS}.

BATT: Rise up and oscillate around V_{OVCH} as long as the source element has not been removed.

HVOUT: Equal to the value set by R5-R6

7. PV cell characterization

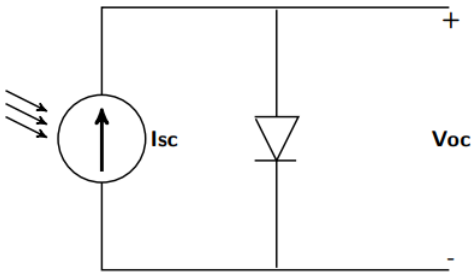


Figure 9: PV cell first order model

A photovoltaic cell can be modelled at first approximation by a light-controlled current source in parallel with a diode as illustrated in Figure 9. This allows to model the two main characteristics of a PV cell: open-circuit voltage (Voc) and short-circuit current (Isc).

The open-circuit voltage corresponds to the forward voltage of the diode at no load while the short-circuit current is the current delivered by the current source (i.e. when shorting the + and - terminals).

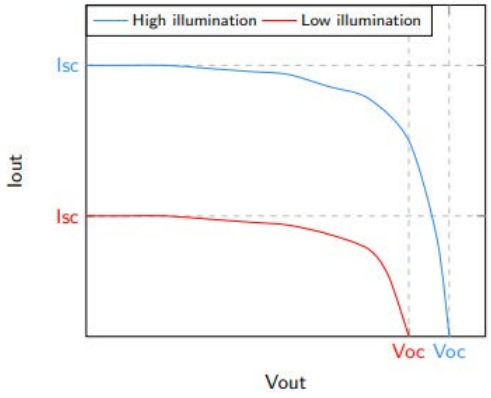


Figure 10: Typical I-V curve of a PV cell for high and low illumination level

Typical current vs voltage graph of a PV cell for different illumination levels can be observed in Figure 10. Knowing that P = I * V, the associated power vs voltage curves can be drawn as shown in Figure 11. For a given technology, the maximum extracted power is achieved at a voltage corresponding to a given ratio of the open-circuit voltage (between 70% and 90%). This ratio is, in first approximation, independent of the illumination level: as can be seen in Figure 11, Vmpp / Voc ≈ Vmpp / Voc .

As presented in Table 4, the MPP configuration of the AEM10941 allows you to select the voltage ratio that optimizes the power extraction according to the characteristics of your PV cell.

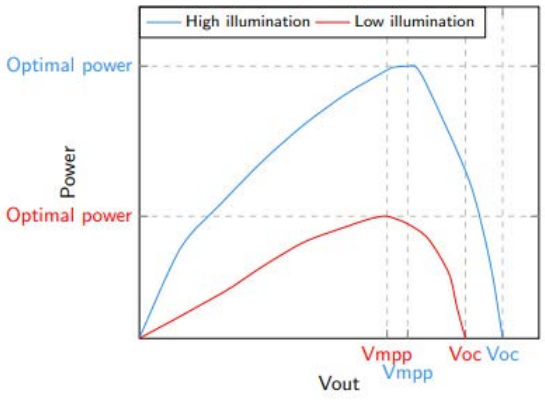


Figure 11: Typical power-V curve of a PV cell for high and low illumination level

As can be seen in Figure 11, the power significantly decreases with the voltage beyond the optimum Vmpp. It is then recommended to configure the Vmpp/Voc ratio to be slightly lower than the theoretical optimum and therefore avoid a significant drop of performance.

1. Revision History

Revision	Date	Description
1.0	February, 2022	Creation of the document

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