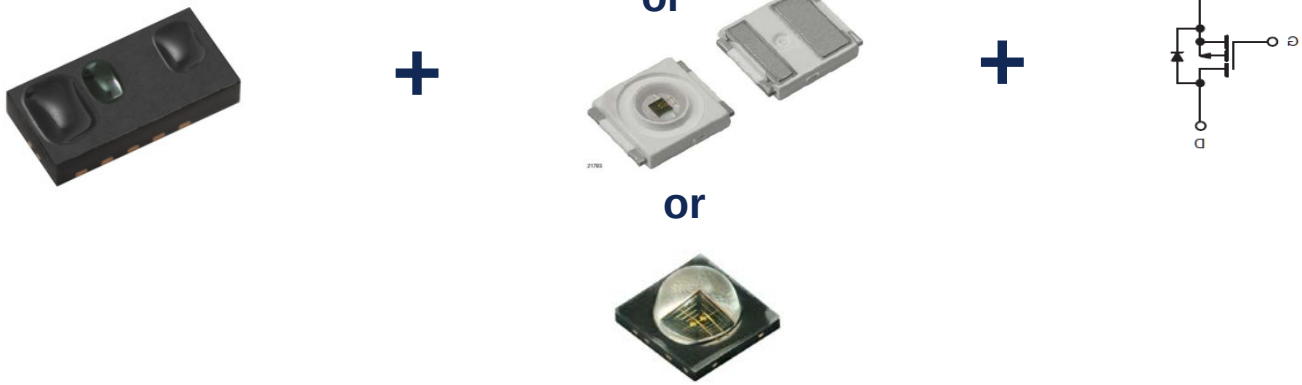
Higher Detection Distances with Proximity Sensor



R.S. 05.12.2013

VCNL40x0 with external high power emitter and external driver

As already shown within the AN: "***Extended Detection Range with VCNL Family of Proximity Sensor***" an external IRED could be connected to the VCNL`s to allow for increase of the detection range.

If even further higher distances need to be achieved VCNL`s internal current source with max. 200mA may not be sufficient enough.

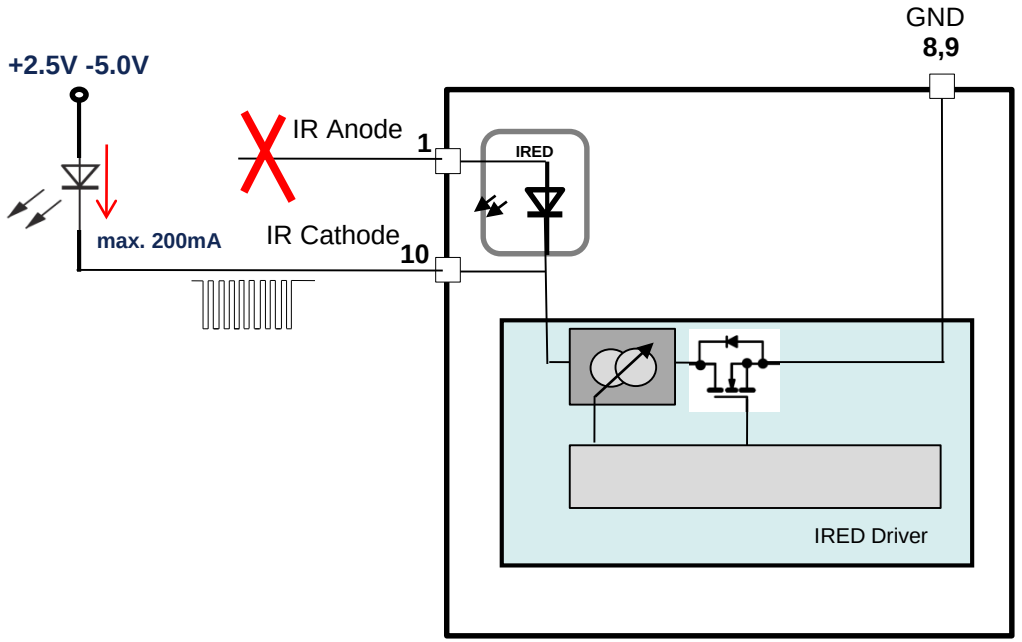


Fig.1 – VCNL4020 Principle Operation of the IRED Driver

VCNL40x0 with external high power emitter and external driver

Proximity detector is only “open” (active) for IRED burst time.
That means that an external driver needs to be driven by this burst and this is available at IR_Cathode.
The yellow signal below shows that only after asking for a proximity measurement the receiver gets its needed power supply and this also only for about that short period the burst lasts.

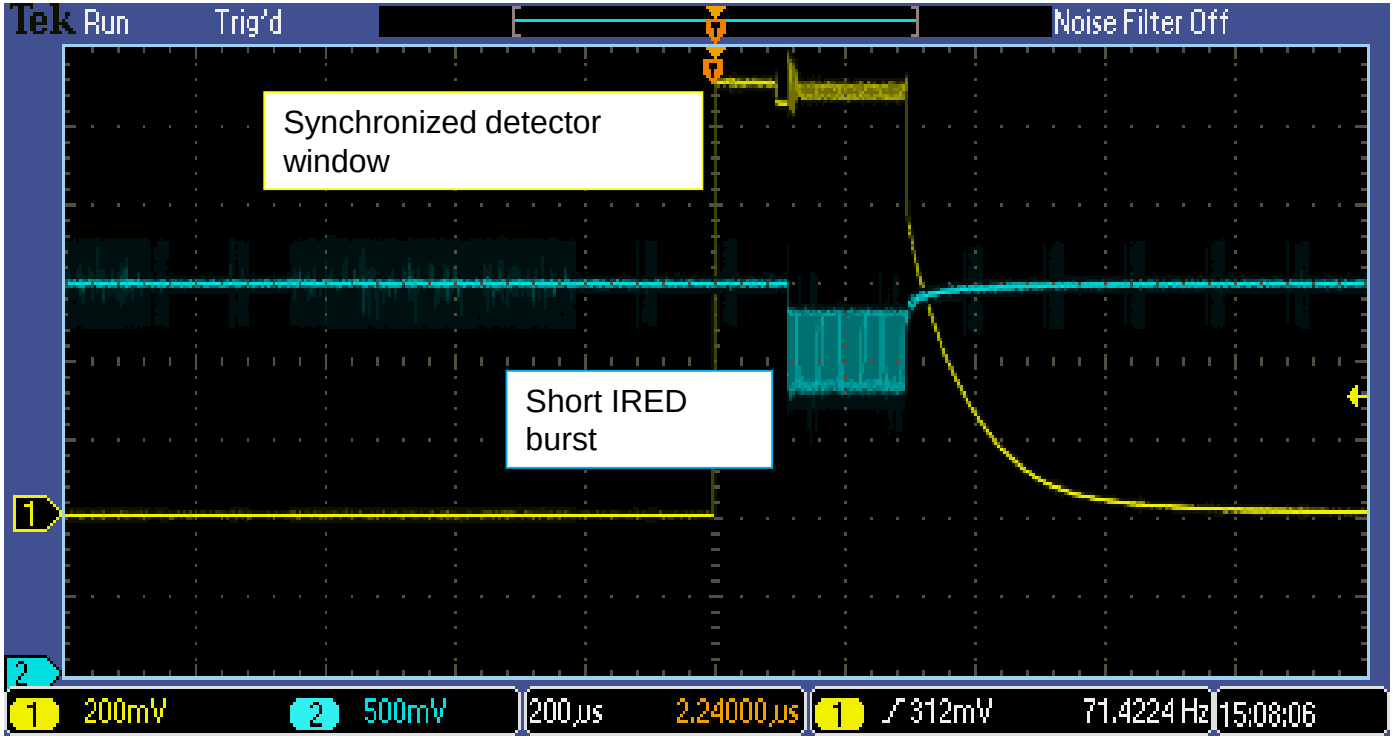


Fig.2 – Scope figures for IRED proximity burst and detector bias voltage

VCNL40x0 with external high power emitter and external driver

This proximity burst is a high frequency burst (390 kHz) and max. Power supply at this IR_Cathode pin is 3.3V.

One measurement cycle consists of transmitting and receiving a single burst signal. The burst length is fixed for all burst frequency settings.
The total measurement cycle has a duration of about 164µs. The burst length (IRED active) during this measurement cycle is 153µs. The duty cycle within the burst signal is 50%.

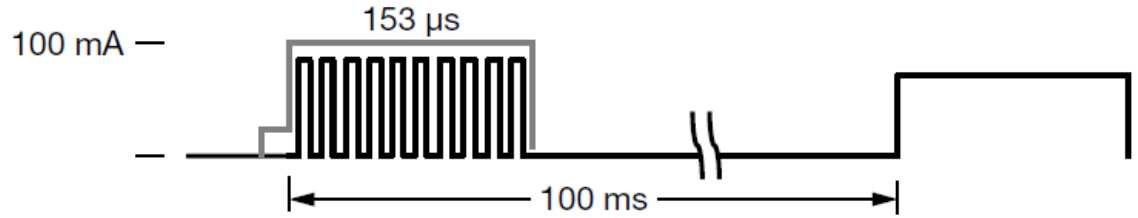


Fig.3 – Emitter Pulses

Total average power consumption is mainly related to the repetition rate these measurements are carried out.
Please see also: http://www.vishay.com/optoelectronics/opto-sensors-calculator/

VCNL40x0 with external high power emitter and external driver

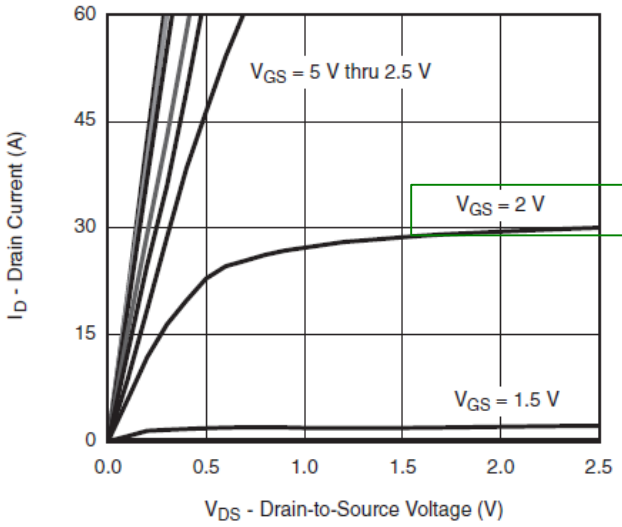
This proximity burst is a high frequency burst (390 kHz) and max. Power supply at this IR_Cathode pin is 3.3V.
So the selected FET transistor needs proper parameters to operate as driver.

The needed external P-Channel FET should be carefully selected

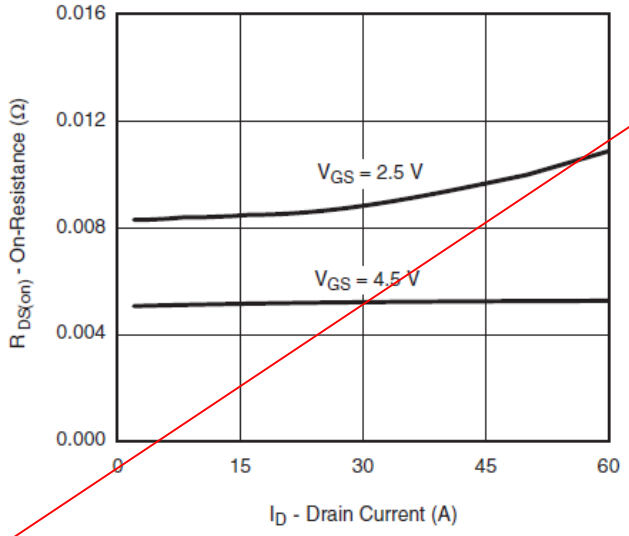
A quite low Gate-Source Voltage (V_{GS}) is needed
A quite low On Resistance ($R_{DS(on)}$) is needed
A quite low Input Capacitance (C_{iss}) is needed

Si4477DY

P-Channel 20-V (D-S) MOSFET

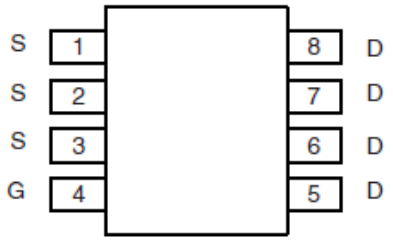


Output Characteristics



On-Resistance vs. Drain Current

SO-8



Top View

Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 18 A		0.0051	0.0062	Ω
		V_{GS} = - 2.5 V, I_D = - 14 A		0.0085	0.0105	

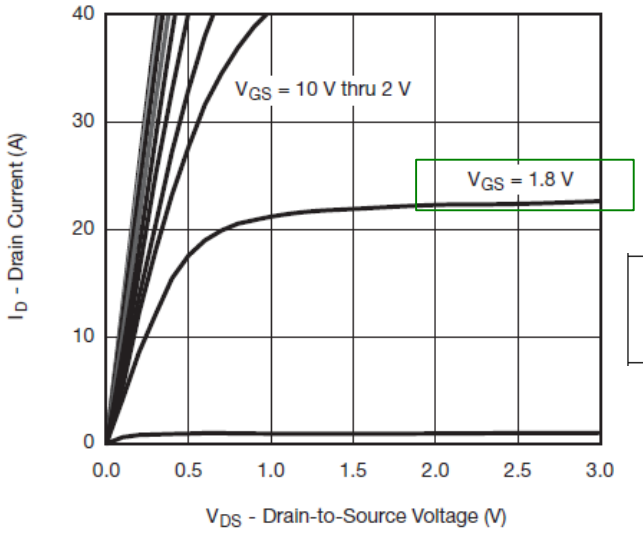
RDS(on) < = 0.01Ω

Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		4600		pF
Output Capacitance	C_{oss}			980		
Reverse Transfer Capacitance	C_{rss}			175		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 10 V, I_D = - 18 A		125	190	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 18 A		59	90	
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			19		
Gate Resistance	R_g	f = 1 MHz		1.3	2.6	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω I_D ≅ - 1 A, V_{GEN} = - 10 V, R_g = 1 Ω		13	20	ns
Rise Time	t_r			10	20	
Turn-Off DelayTime	$t_{d(off)}$			100	150	
Fall Time	t_f			25	40	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω I_D ≅ - 1 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		42	60	
Rise Time	t_r			42	60	
Turn-Off DelayTime	$t_{d(off)}$			100	150	
Fall Time	t_f			42	60	

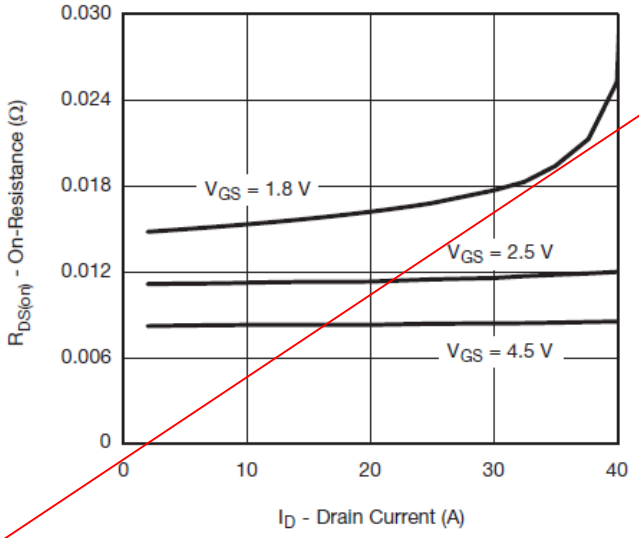
Fig.4 – Si4477DY datasheet extract

SiS407DN

P-Channel 20-V (D-S) MOSFET

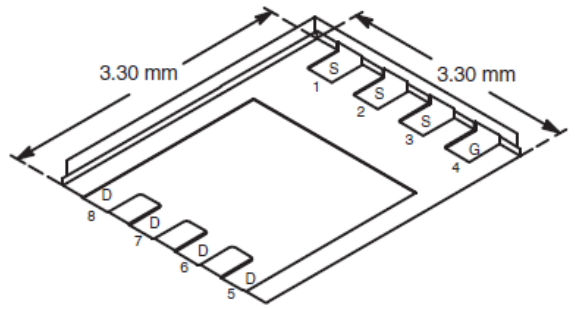


Output Characteristics



On-Resistance vs. Drain Current

PowerPAK 1212-8



Bottom View

Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 15.3 A		0.0082	0.0095	Ω
		V_{GS} = - 2.5 V, I_D = - 13.1 A		0.0115	0.0138	
		V_{GS} = - 1.8 V, I_D = - 5 A		0.0156	0.0195	

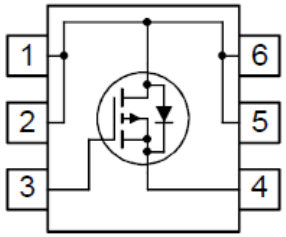
RDS(on) < = 0.01Ω

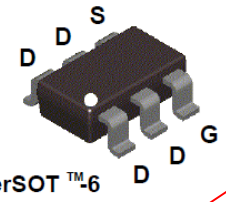
Dynamic[b]						
Input Capacitance	C_{iss}			2760		pF
Output Capacitance	C_{oss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		405		
Reverse Transfer Capacitance	C_{rss}			370		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 8 V, I_D = - 10 A		62.5	93.8	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 10 A		38	57	
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			10		
Gate Resistance	R_g	f = 1 MHz	0.9	4.4	8.8	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 1 Ω $I_D \cong$ - 10 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		23	35	ns
Rise Time	t_r			28	42	
Turn-Off DelayTime	$t_{d(off)}$			92	138	
Fall Time	t_f			38	57	

Fig.5 – SiS407DN datasheet extract

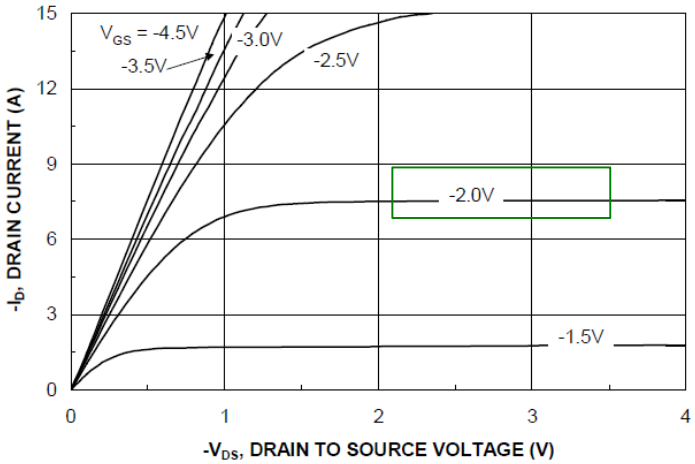
Si3441DV

P-Channel 2.5V Specified PowerTrench® MOSFET



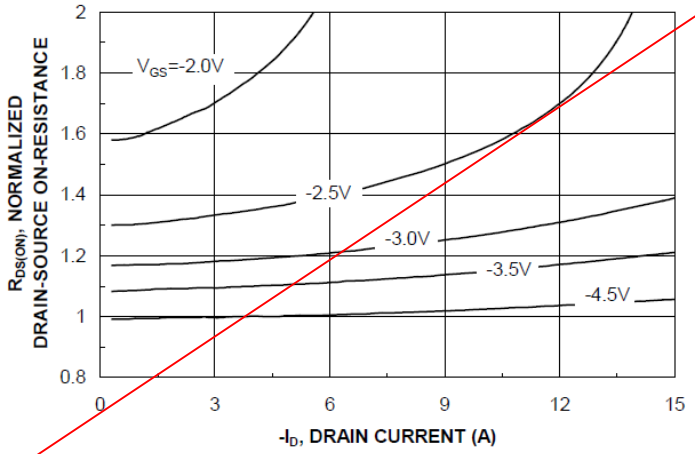


SuperSOT ™-6



$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –3.5 A V_{GS} = –2.5 V, I_D = –3.1 A V_{GS} = –4.5 V, I_D = –3.5A, T_J=125°C		60 82 77	80 110 112	mΩ

RDS(on) < = 0.1Ω



Dynamic Characteristics

C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V,		779		pF
C_{oss}	Output Capacitance	f = 1.0 MHz		121		pF
C_{rss}	Reverse Transfer Capacitance			56		pF

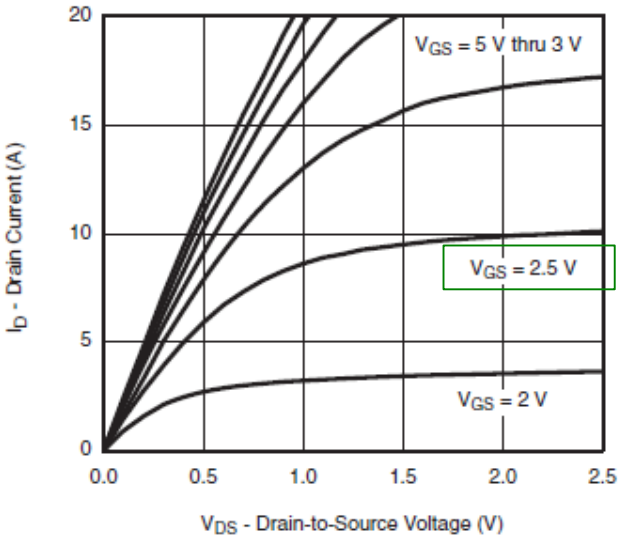
Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A,		10	20	ns
t_r	Turn–On Rise Time	V_{GS} = –4.5 V, R_{GEN} = 6 Ω		9	19	ns
$t_{d(off)}$	Turn–Off Delay Time			27	43	ns
t_f	Turn–Off Fall Time			11	20	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –3.5 A,		7.2	10	nC
Q_{gs}	Gate–Source Charge	V_{GS} = –4.5 V		1.7		nC
Q_{gd}	Gate–Drain Charge			1.5		nC

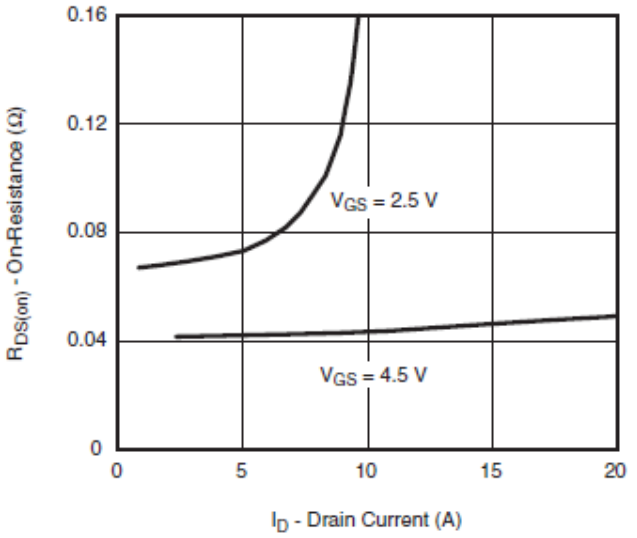
Fig.6 – Si3441DV datasheet extract

Si5459DU

P-Channel 20-V (D-S) MOSFET

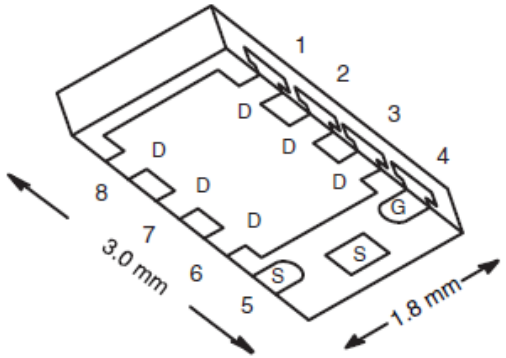


Output Characteristics



On-Resistance vs. Drain Current and Gate Voltage

PowerPAK® ChipFET Single



Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 6.7 A		0.043	0.052	Ω
		V_{GS} = - 2.5 V, I_D = - 1 A		0.068	0.082	

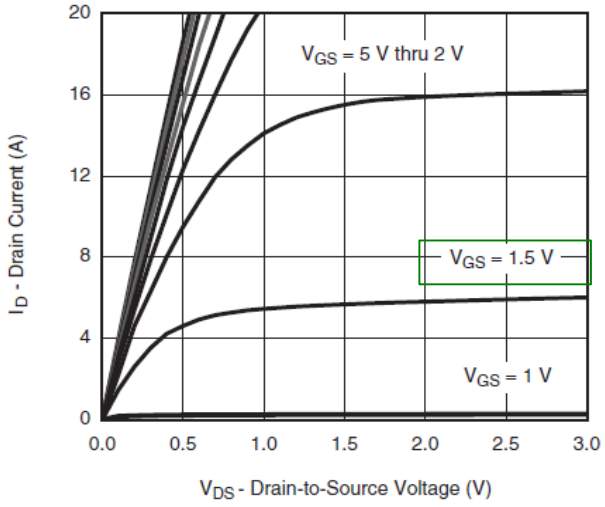
RDS(on) < = 0.05Ω

Dynamic[a]						
Input Capacitance	C_{iss}			665		pF
Output Capacitance	C_{oss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		140		
Reverse Transfer Capacitance	C_{rss}			115		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 10 V, I_D = - 6.7 A		17	26	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 6.7 A		8	12	
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			3		
Gate Resistance	R_g	f = 1 MHz	1.2	6	12	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 1.9 Ω $I_D \cong$ - 5.3 A, V_{GEN} = - 10 V, R_g = 1 Ω		6	12	ns
Rise Time	t_r			15	23	
Turn-Off Delay Time	$t_{d(off)}$			26	39	
Fall Time	t_f			9	18	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 1.9 Ω $I_D \cong$ - 5.3 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		21	32	
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			29	44	
Fall Time	t_f			13	20	

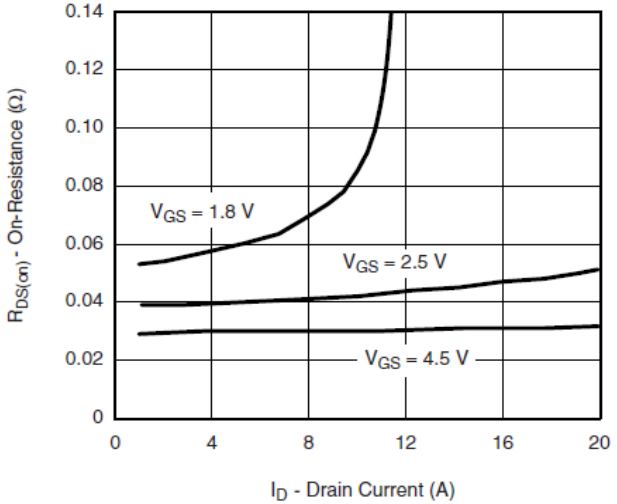
Fig.7 – Si5459DU datasheet extract

Si3447CDV

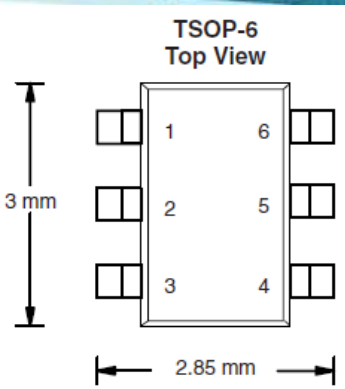
P-Channel 12-V (D-S) MOSFET

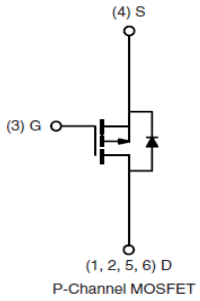


Output Characteristics



On-Resistance vs. Drain Current and Gate Voltage





Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 6.3 A		0.03	0.036	Ω
		V_{GS} = - 2.5 V, I_D = - 5.3 A		0.041	0.050	
		V_{GS} = - 1.8 V, I_D = - 1.5 A		0.055	0.068	

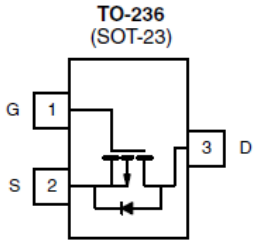
RDS(on) < = 0.04Ω

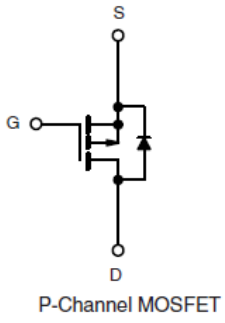
Dynamic[b]						
Input Capacitance	C_{iss}			910		pF
Output Capacitance	C_{oss}	V_{DS} = - 6 V, V_{GS} = 0 V, f = 1 MHz		260		
Reverse Transfer Capacitance	C_{rss}			220		
Total Gate Charge	Q_g	V_{DS} = - 6 V, V_{GS} = - 8 V, I_D = - 6.3 A		20	30	nC
		V_{DS} = - 6 V, V_{GS} = - 4.5 V, I_D = - 6.3 A		12	18	
Gate-Source Charge	Q_{gs}			1.6		
Gate-Drain Charge	Q_{gd}			3.4		
Gate Resistance	R_g	f = 1 MHz		6		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 6 V, R_L = 1.2 Ω $I_D \cong$ - 5 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		20	30	ns
Rise Time	t_r			40	60	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	t_f			20	30	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 6 V, R_L = 1.2 Ω $I_D \cong$ - 5 A, V_{GEN} = - 8 V, R_g = 1 Ω		10	15	
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	t_f			15	25	

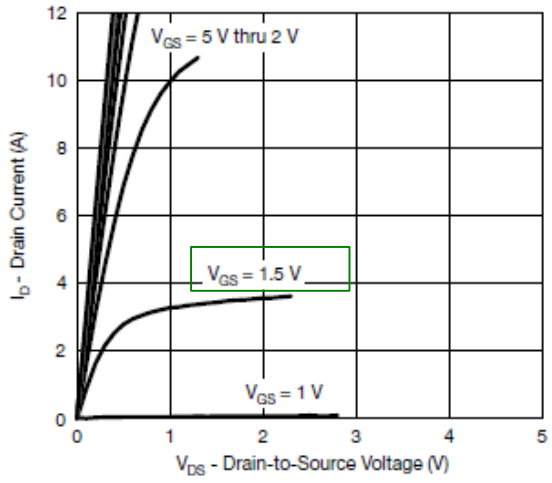
Fig.8 – Si3447CDV datasheet extract

SQ2315ES

Automotive P-Channel 12 V (D-S) 175 °C MOSFET



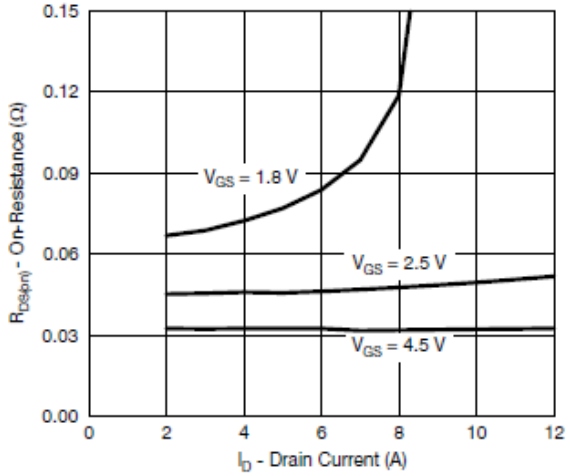




Output Characteristics

Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V	I_D = - 3.5 A	-	0.034	0.050	Ω
		V_{GS} = - 4.5 V	I_D = - 3.5 A, T_J = 125 °C	-	-	0.066	
		V_{GS} = - 4.5 V	I_D = - 3.5 A, T_J = 175 °C	-	-	0.075	
		V_{GS} = - 2.5 V	I_D = - 3 A	-	0.046	0.068	
		V_{GS} = - 1.8 V	I_D = - 2 A	-	0.067	0.092	

RDS(on) < = 0.05Ω



On-Resistance vs. Drain Current

Dynamic[b]							
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = - 6 V, f = 1 MHz	-	695	870	pF
Output Capacitance	C_{oss}			-	265	335	
Reverse Transfer Capacitance	C_{rss}			-	190	240	
Total Gate Charge[c]	Q_g	V_{GS} = - 4.5 V	V_{DS} = - 6 V, I_D = - 3.85 A	-	8.4	13	nC
Gate-Source Charge[c]	Q_{gs}			-	1	-	
Gate-Drain Charge[c]	Q_{gd}			-	2.4	-	
Gate Resistance	R_g	f = 1 MHz		4.1	8.2	12.3	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 6 V, R_L = 1.6 Ω $I_D \cong$ - 3.85 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		-	17	26	ns
Rise Time[c]	t_r			-	19	29	
Turn-Off Delay Time[c]	$t_{d(off)}$			-	28	42	
Fall Time[c]	t_f			-	13	20	

VCNL40x0 with external high power emitter and external driver

With high IRED currents the power supply,
the Proximity measurement repetition time
as well as the decoupling needs to be defined carefully

Reference Circuitry:
1 x VSMY7850X01 and 1 x FET: Si5459DU
or
1 x VSMY98545 and 1 x FET: Si5459DU

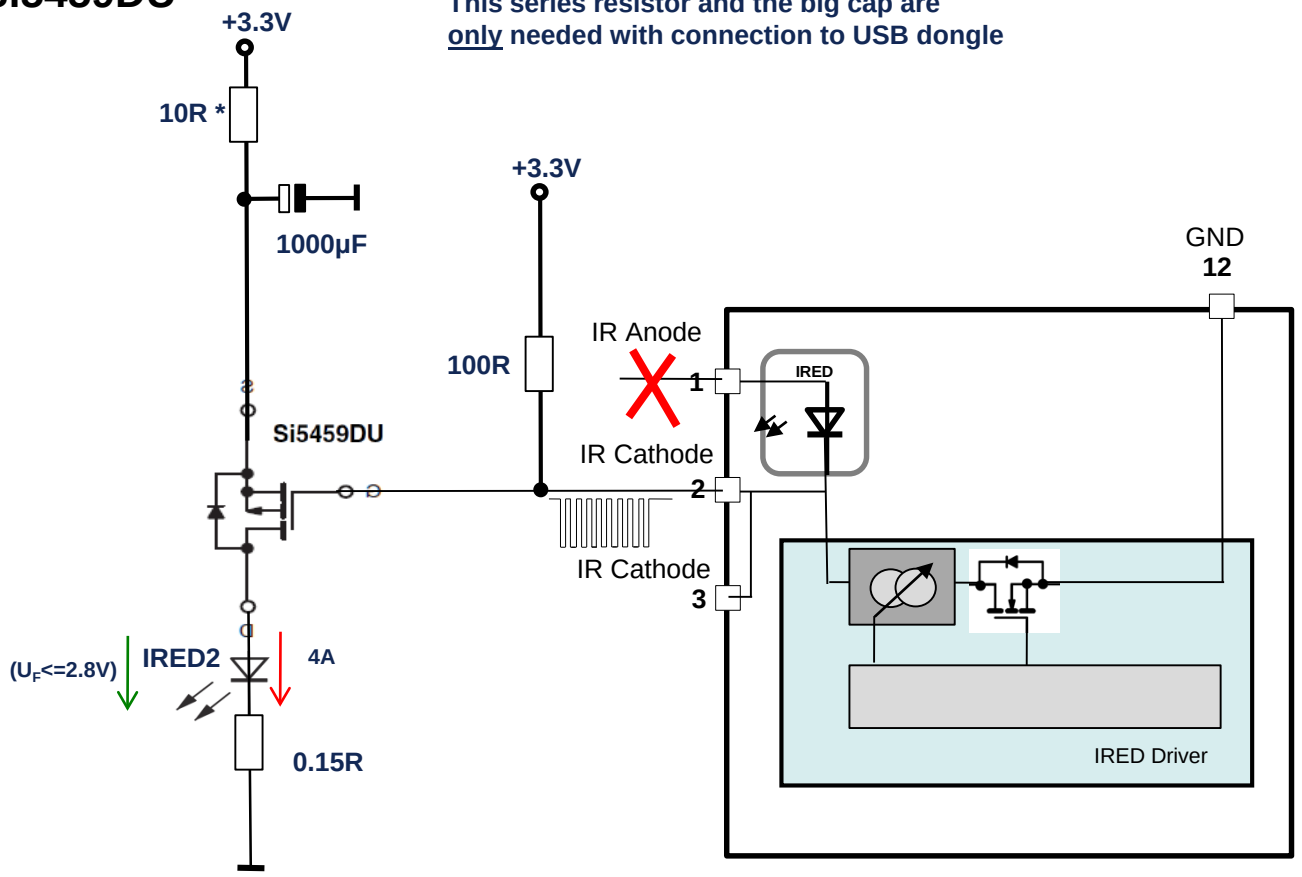


Fig.9 – Reference Circuitry with VSMY7850X01 (or VSMY98545) and Si5459DU

High Power Test Board:
2 x VSMY2850 and 2 x FET (Si5459DU)

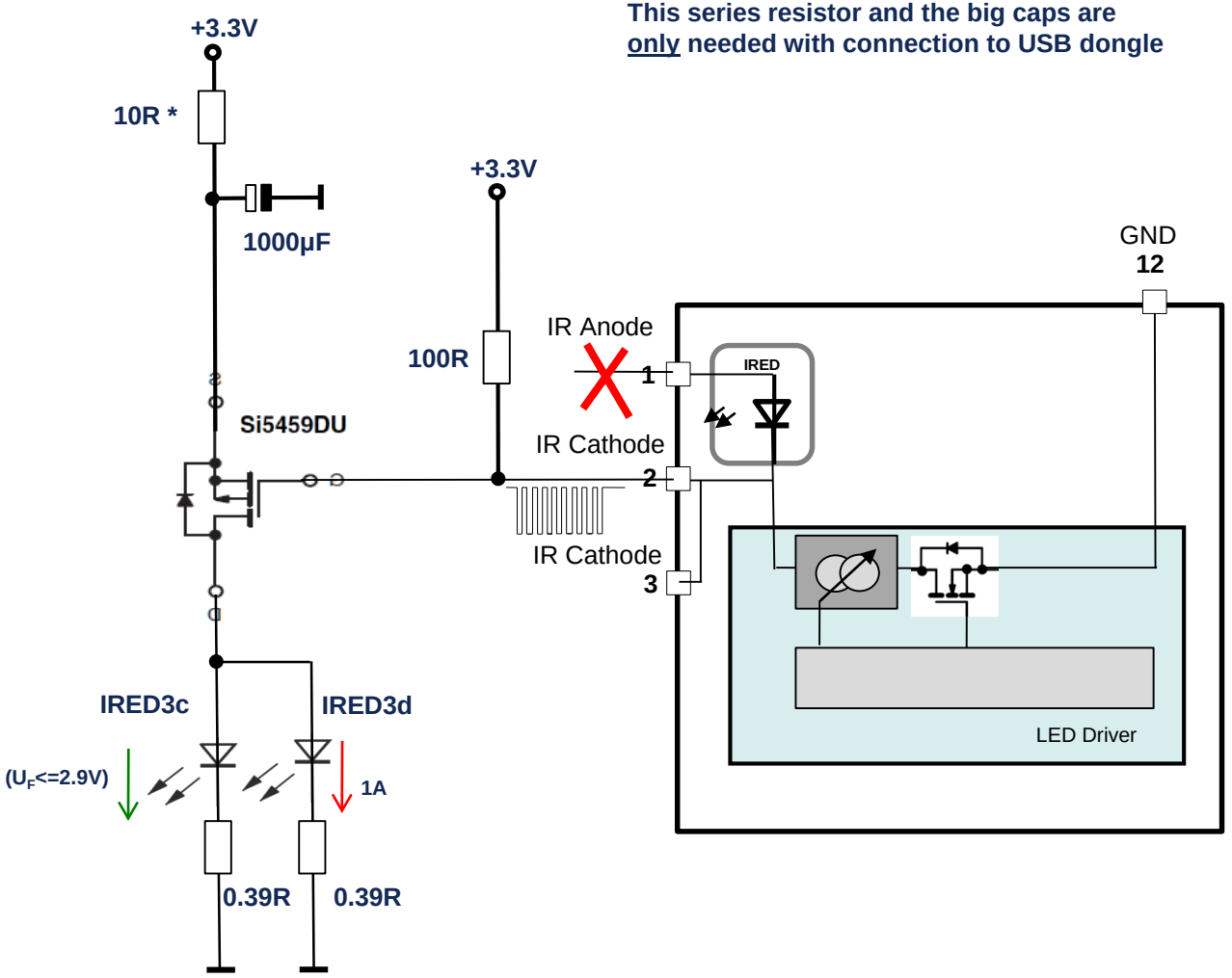


Fig.10 – Reference Circuitry with 2 x VSMY2850 and Si5459DU

High Power Test Board:
2 x 2 VSMY2850 and 2 x FET (Si5459DU)

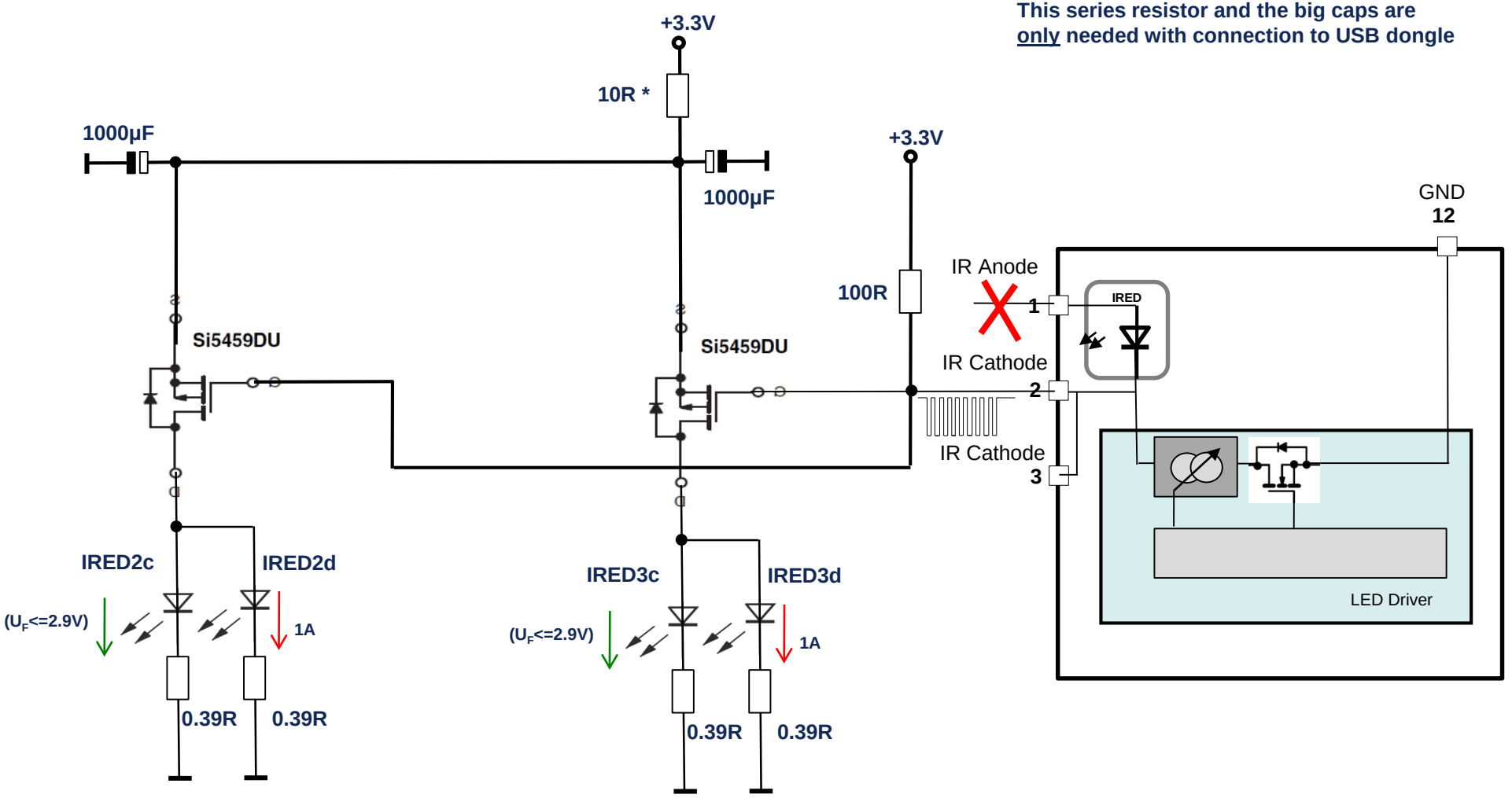


Fig.11 – Reference Circuitry with 2 x 2 x VSMY2850 and 2 x Si5459DU

Current calculation

with chosen $4A_{peak}$ with default setting of fast repetition rate for about 70 measurements/second for the VCNL40x0 Demo Tool results in an average current of just 22 mA !

70 measurement per second, emitter current = 4000 mA

ASIC: 2.71 mA x 164 µs x 70/1 s	=	**31.08 µA**
IRED: 4000 mA x 153 µs x 0.5 x 70/1 s	=	**21.42 mA**
	total:	**21.45 mA**

10 measurement per second, emitter current = 4000 mA

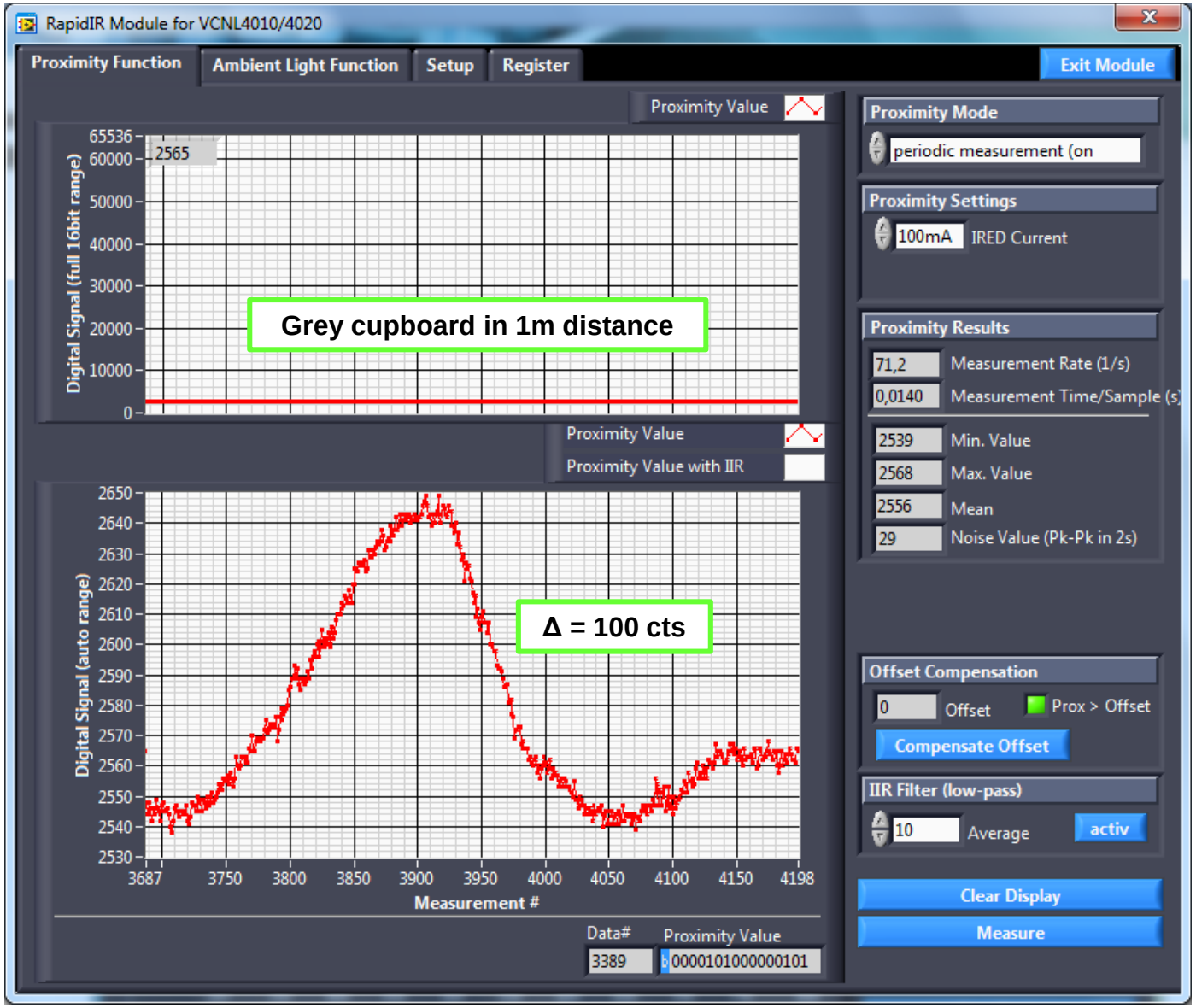
ASIC: 2.71 mA x 164 µs x 10/1 s	=	**4.44µA**
IRED: 4000 mA x 153 µs x 0.5 x 10/1 s	=	**3.06 mA**
	total:	**3.064mA**

Please see also: Designing VCNL4020 into an Application_ 84136 120522.pdf

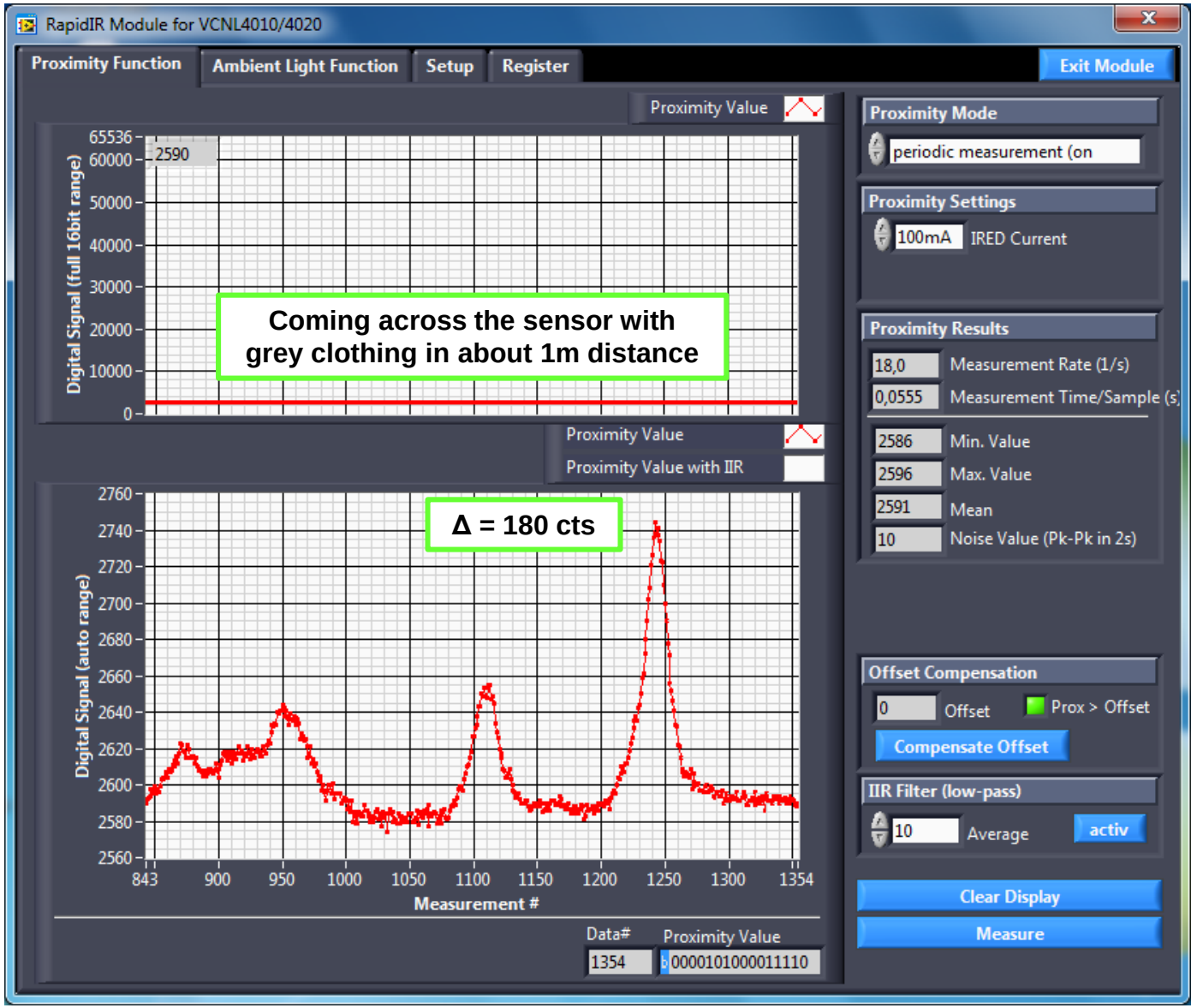
10 measurement per second, emitter current = 100 mA

ASIC: 2.71 mA x 164 µs x 10/1 s =	**4.45 µA**
IRED: 100 mA x 153 µs/1 s x 0.5 x 10/1 s =	**76.50 µA**
total:	**80.95 µA**

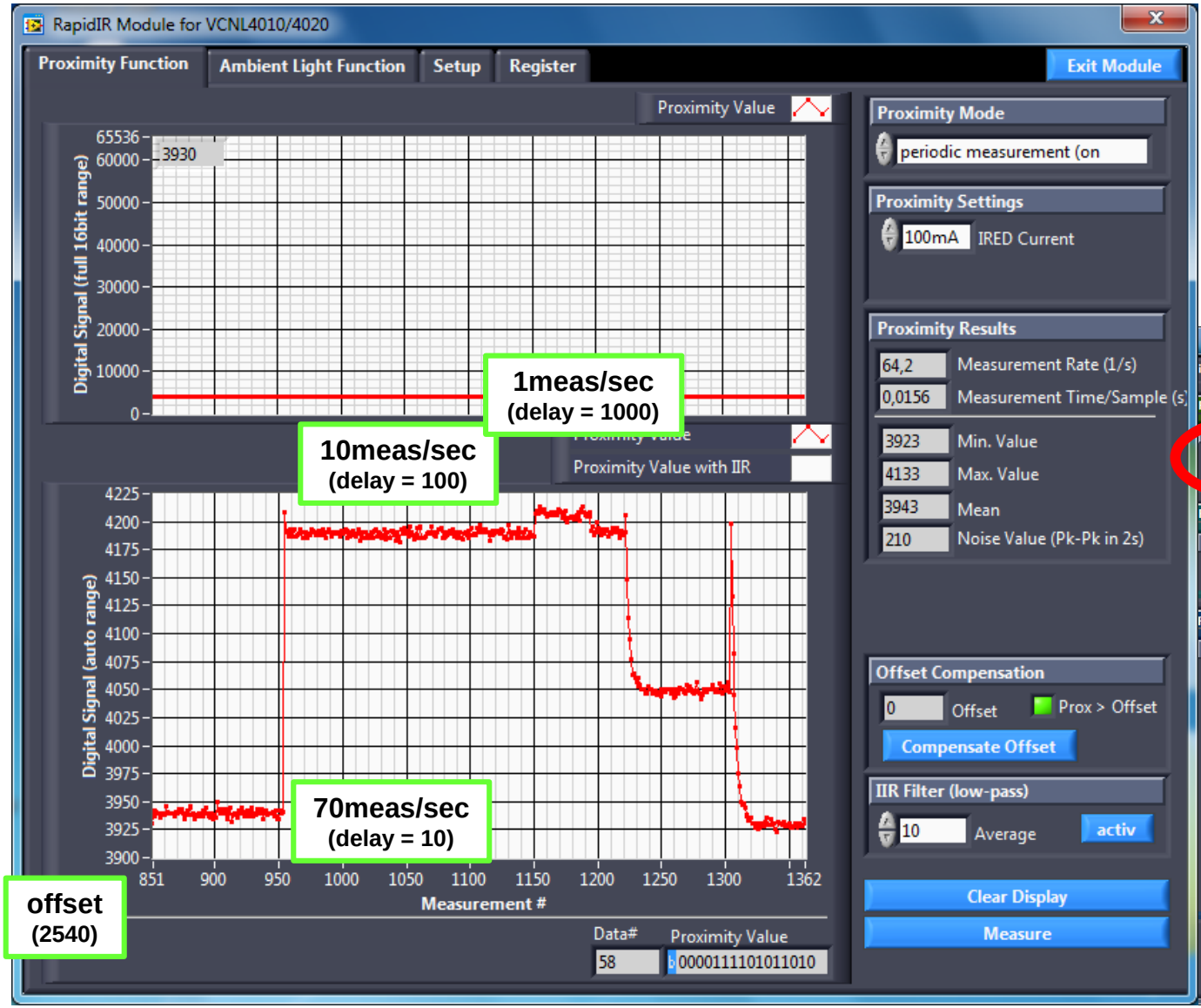
Updated Test Board:
2 x VSMY7850X01 and 2 x new FET (Si5459DU)

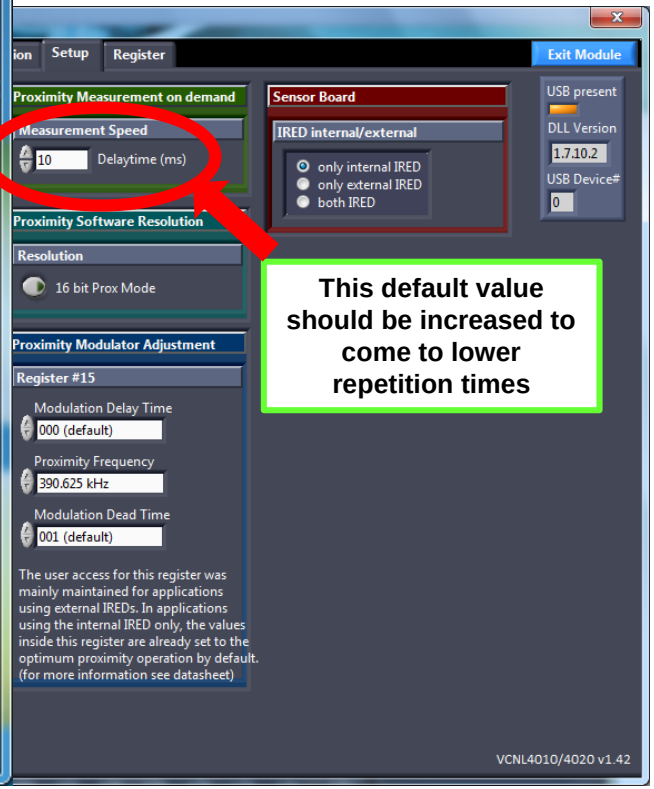


Updated Test Board:
2 x VSMY7850X01 and 2 x new FET (Si5459DU)



Updated Test Board:
2 x VSMY7850X01 and 2 x new FET (Si5459DU)
with power supply via USB dongle





This default value should be increased to come to lower repetition times

Delay & Dead Time Adjust

The AN: http://www.vishay.com/docs/84138/designingvcnl4010.pdf
or : http://www.vishay.com/docs/84136/designingvcnl4020.pdf show at page 14:

Modulation Delay Time

The proximity function works with a modulated signal. The proximity signal demodulator is frequency and phase sensitive and references to the transmitted signal. In case of external infrared emitters with additional driver stages, there might be signal delays that could cause signal loss. By adjusting the “delay time” setting, this additional delay can be compensated. The delay time can be set to values between 0 and 7. Using external infrared emitters the optimum setting is determined by trying different settings. The setting with highest readings for proximity at a certain reflection condition should be selected. Since most applications will use the internal emitter, the default value is 0.

Proximity Frequency

This parameter was used during the development of the VCNL4010. The default setting of f = 390 kHz is the optimum setting.

Modulation Dead Time

Due to the emitter rise and fall times, the modulation signal is not a perfect square wave. Instead a slight slope occurs at the start and end of the signal. The modulation dead time defines a time window or range where the slopes from the received modulated signal are blanked out. This function eliminates effects from slow slopes, glitches and other noise disturbances on the received signal. If the modulation dead time is set too long, a portion of the reflected signal will be lost in addition to the rise time slope. The modulation dead time can be set to values between 0 and 7. The default setting is 1. This setting is sufficient to suppress noise transients. It is NOT recommended to use the value “0” as a “dead time” setting. When using an external driver and emitters, it might be necessary to adjust this parameter. An external driver might cause slow slopes, unstable readings or higher noise. Such effects could be reduced by adjusting this parameter.

Especially modifying the Delay Time could lead to a significant increase of delta counts.
Beside the possible higher delta counts always the offset counts need to be compared

SHOWIN Technology Co.,Ltd.
Tel:886-4-2358-3636 Fax:886-4-2358-3737
No.14, 5th Rd., Industrial Park, Situn Dist., Taichung City 407, Taiwan

Lens	PN#	LED Type		Angle* (θ)	Distribution Type	Dimension (mm)	Holder Required (Y/N)	Remark
	FL-86 +Holder	Vishay	7850	15	Lambertian	ψ19.6x 11.95	Y	
	FL-87 +Holder	Vishay	7850	20	Lambertian	ψ19.6x 11.95	Y	
	FL-88 +Holder	Vishay	7850	25	Lambertian	ψ19.6x 11.95	Y	
	FL-35H +Holder	Vishay	7850	11	Lambertian	ψ21.4 x 11.21	Y	
	FL-32H +Holder	Vishay	7850	17	Lambertian	ψ21.4 x 11.21	Y	
	FL-33H +Holder	Vishay	7850	30	Lambertian	ψ21.4 x 11.21	Y	
	FL-95 +Holder	Vishay	7850	20	Lambertian	ψ21.4 x 11.21	Y	
	FL-112 +Holder	Vishay	7850	45	Lambertian	ψ21.4 x 11.21	Y	
	FL-113 +Holder	Vishay	7850	25	Lambertian	ψ21.4 x 11.21	Y	
	FL-115 +Holder	Vishay	7850	60	Lambertian	ψ21.4 x 11.21	Y	
	FL-110	Vishay	7850	6	Lambertian	21.5 x 21.5 t=12	Y	
	FL-103	Vishay	7850	8	Lambertian	ψ24.57 x 13.35	Y	
	FL-104	Vishay	7850	10	Lambertian	ψ24.57 x 13.35	Y	

High Power Board:
1 x VSMY7850X01 and added Showin Lens

High Power Board:
1 x VSMY7850X01 and added Showin Lens