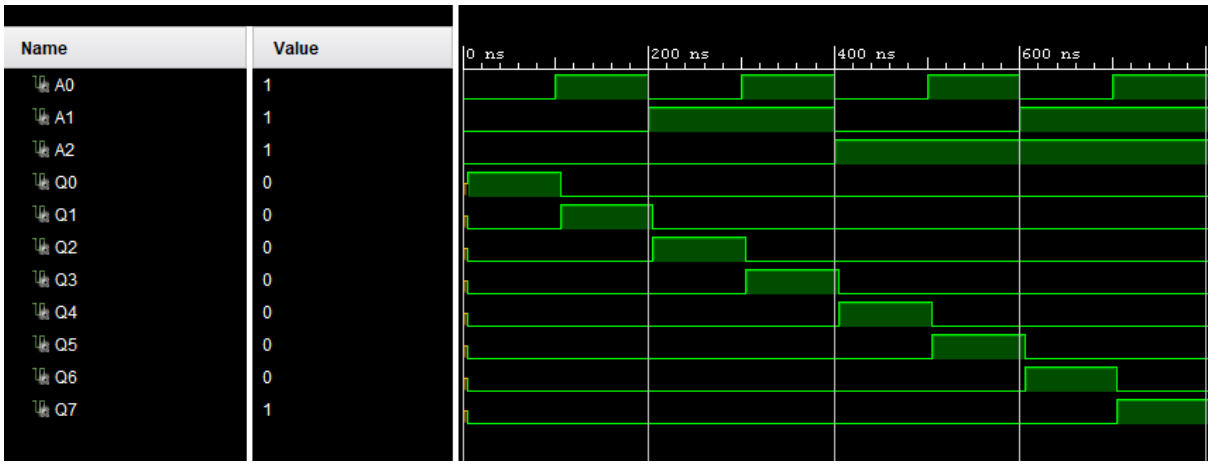
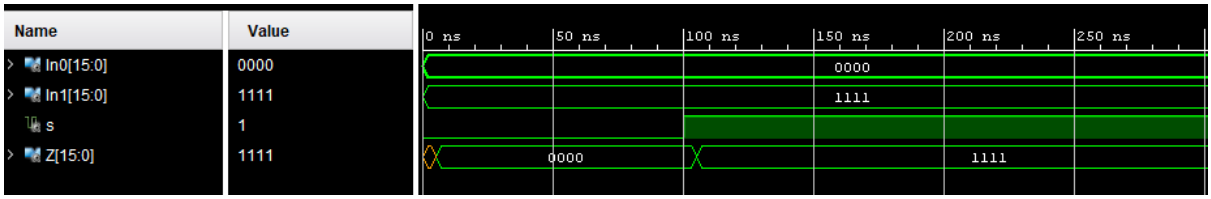
3 to 8 Decoder:



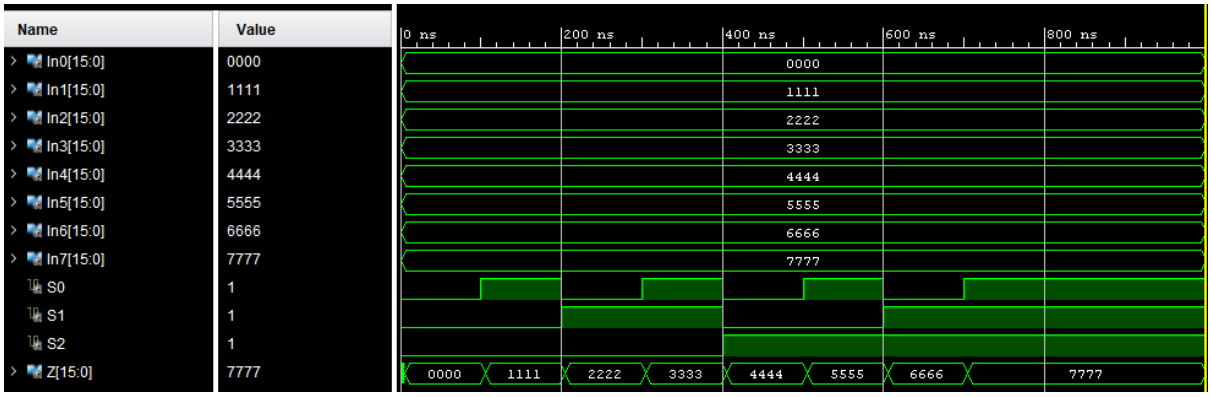
This test bench shows that all outputs (Q0-Q7) are low except for the one selected by the input lines (A0-A2). Eg, Q7 is high when A0, A1 and A2 are all high.

2 Input Multiplexer:



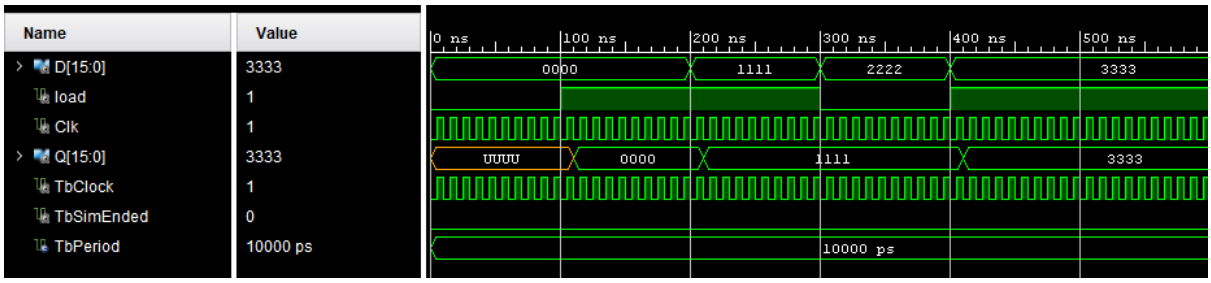
This test bench shows that the output is In0 when the selection line is low and In1 when the selection line is high.

8 Input Multiplexer:



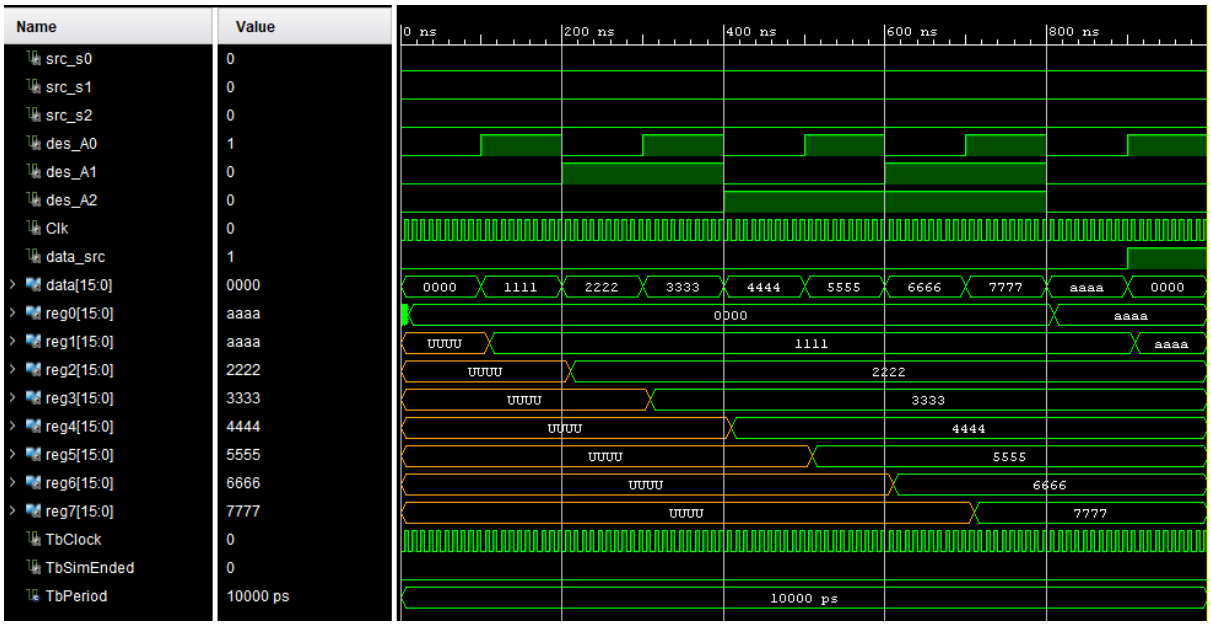
This test bench shows that the output corresponds to the values of the selection lines similar to the decoder and 2 input multiplexer. Eg, the output is In7 when all three selection lines are high.

Register:



This test bench shows that when the clock is high, the value in Q is loaded into D if and only if the load is high. Eg, the value 0000 is loaded into D on the falling edge of the clock when load is high but the value 2222 is not as the load is low.

Register File:



This test bench shows values being loaded into registers depending on the value of the destination lines. Eg, the value 7777 is loaded into reg7 when all the destination lines are high. This happens when data source is low.

Secondly, it shows the value AAAA being moved from register 0 to 1 when the all the source lines are low and only the first destination line is high. This happens when data source is high.