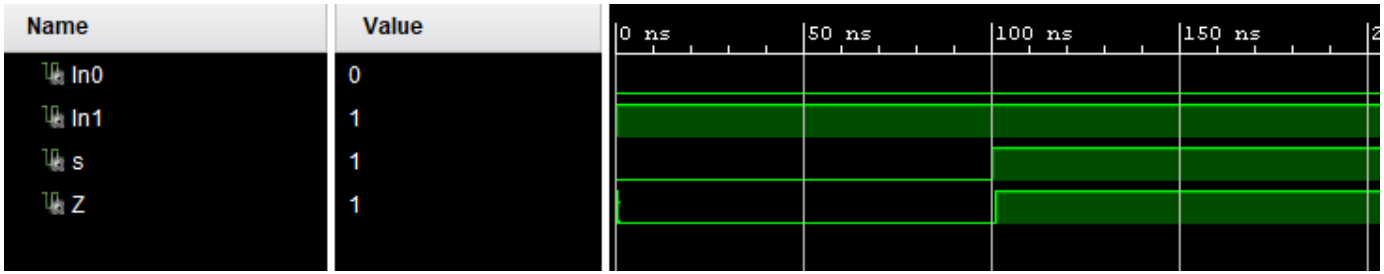
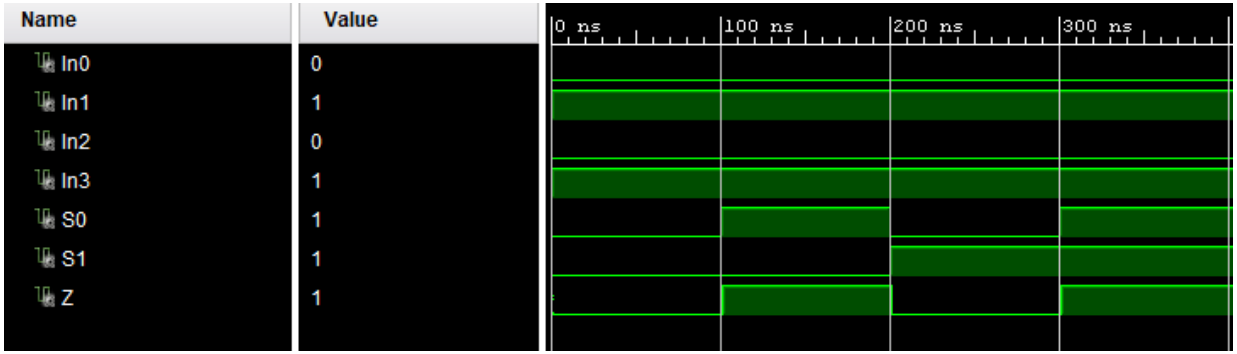
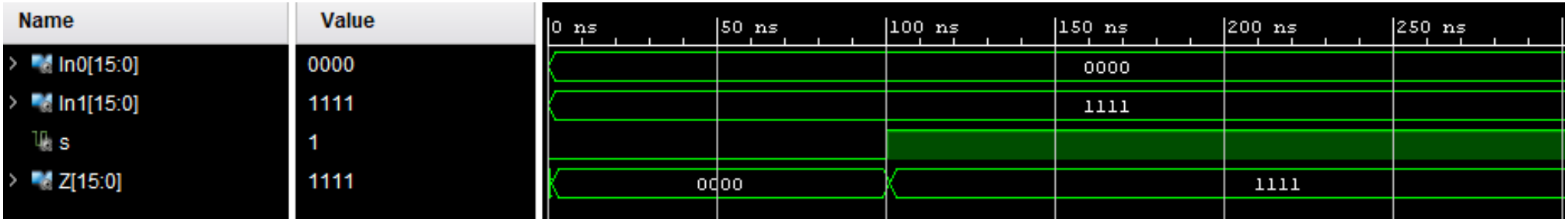
2 Input Multiplexer



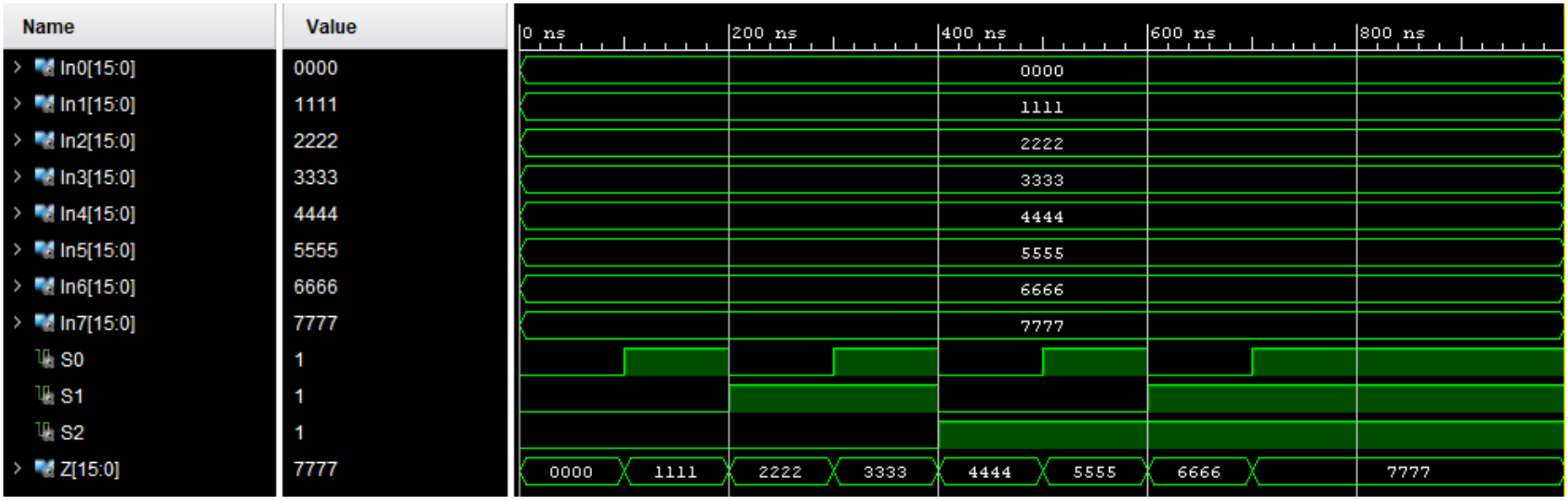
4 Input Multiplexer



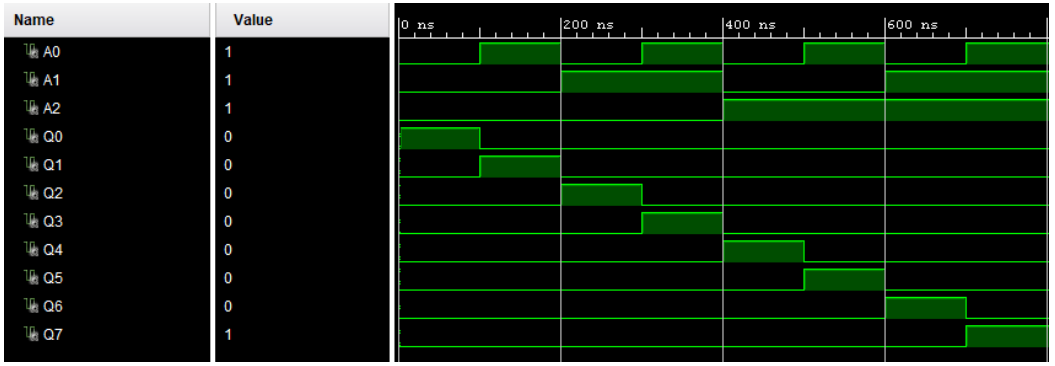
16 Bit 2 Input Multiplexer



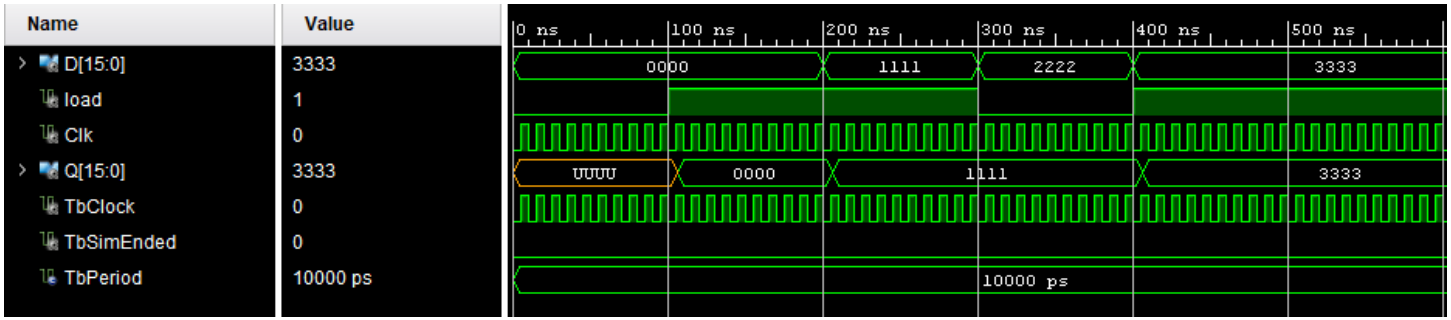
16 Bit 8 Input Multiplexer



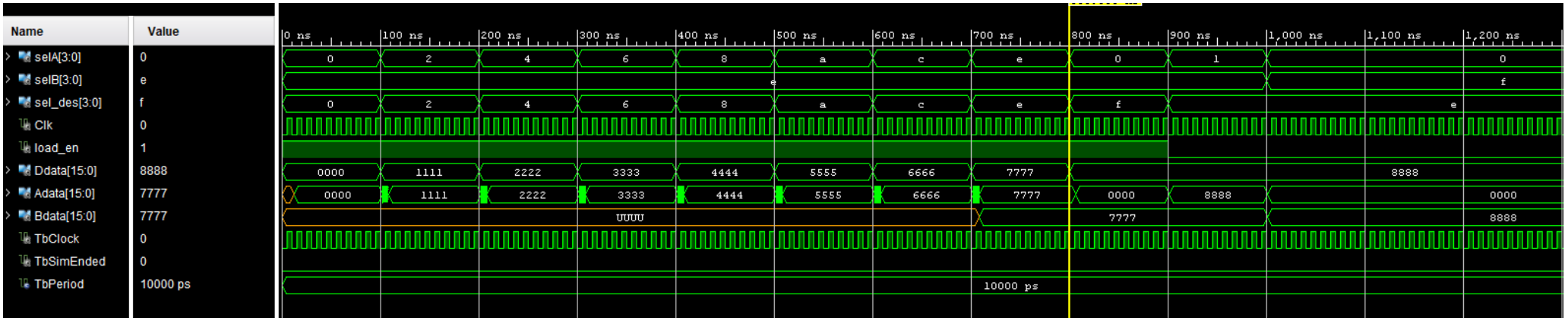
3 To 8 Decoder



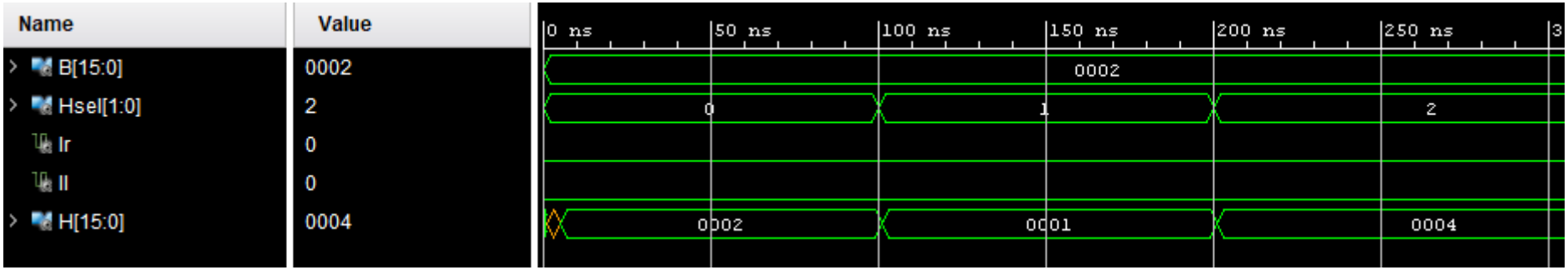
Register



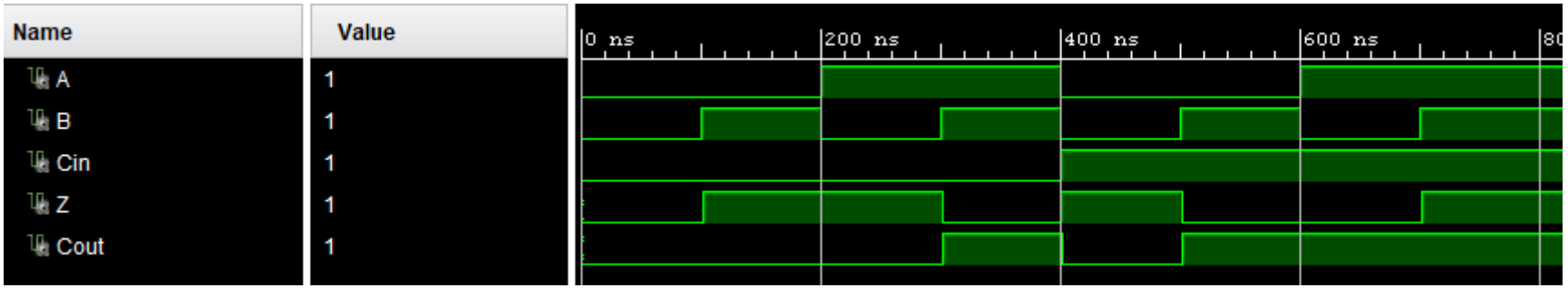
Register File



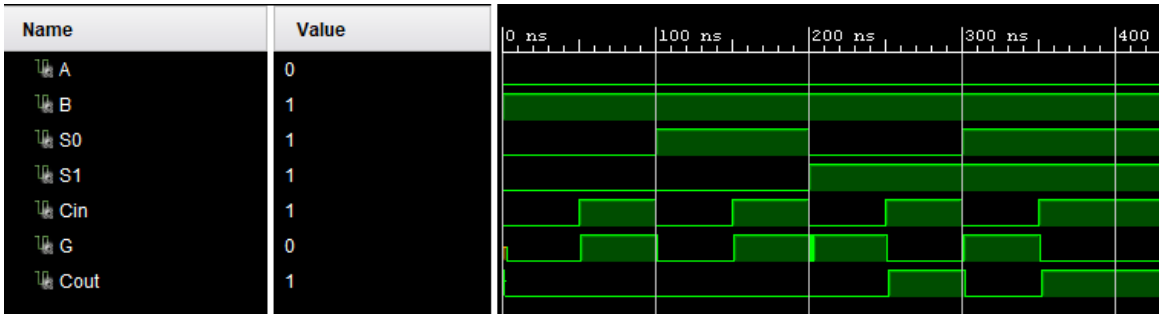
Shifter



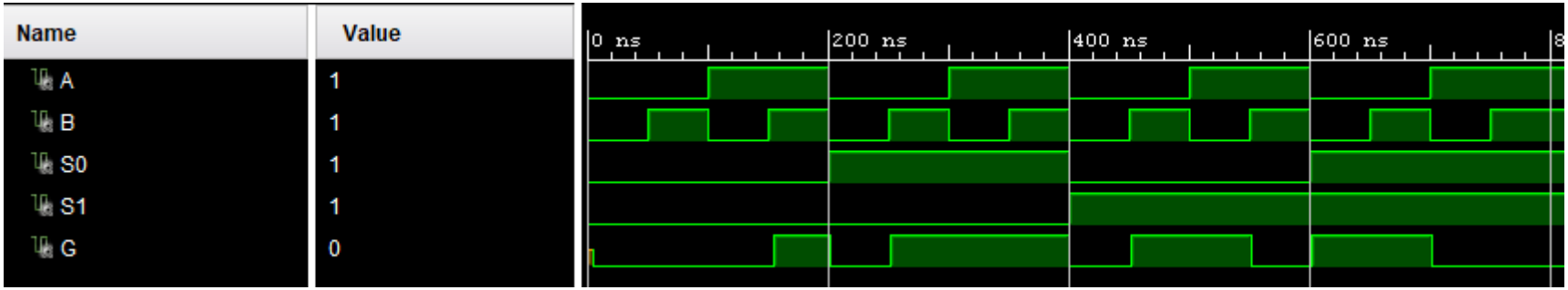
Full Adder



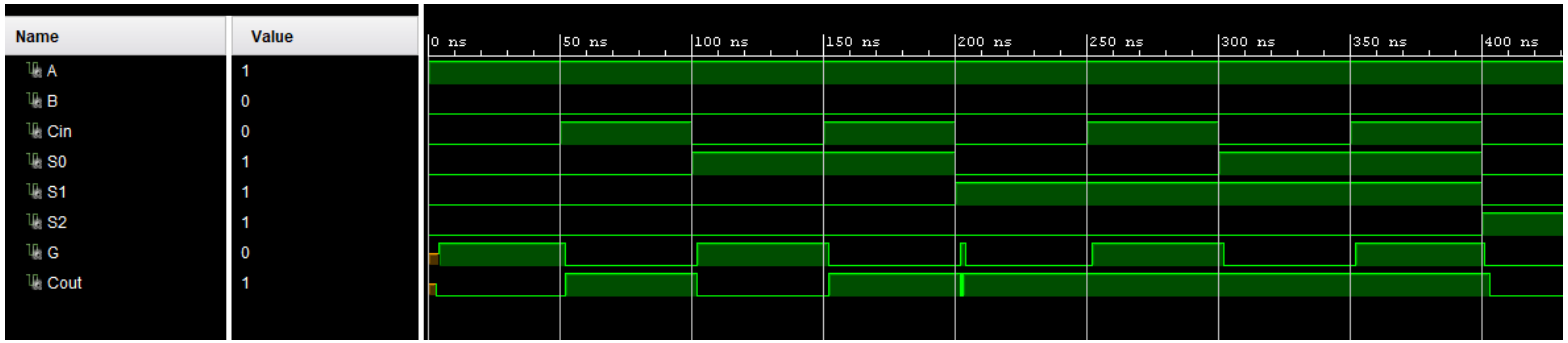
Arithmetic Bit Slice



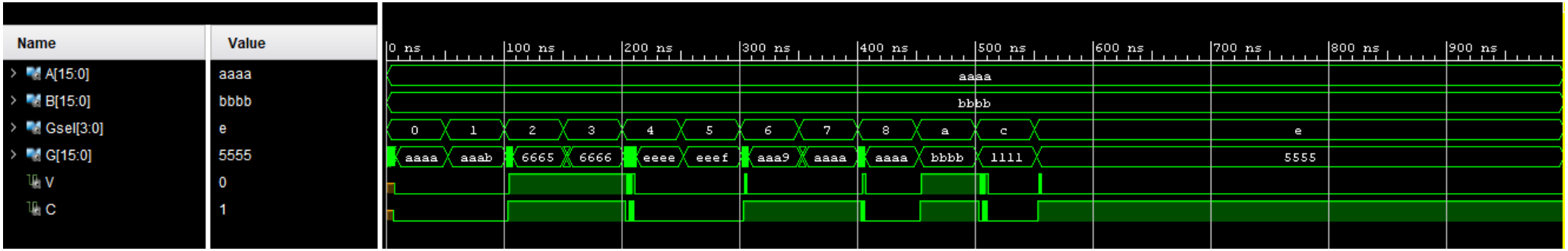
Logic Bit Slice



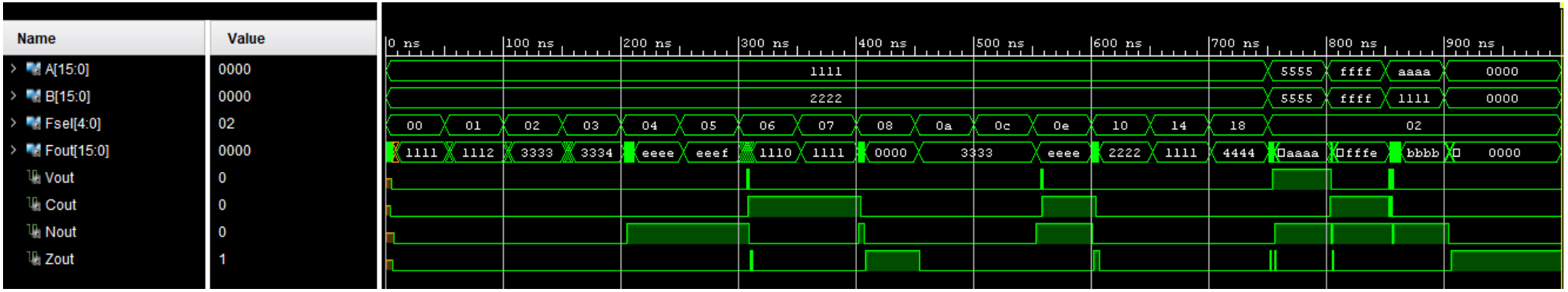
ALU Bit Slice



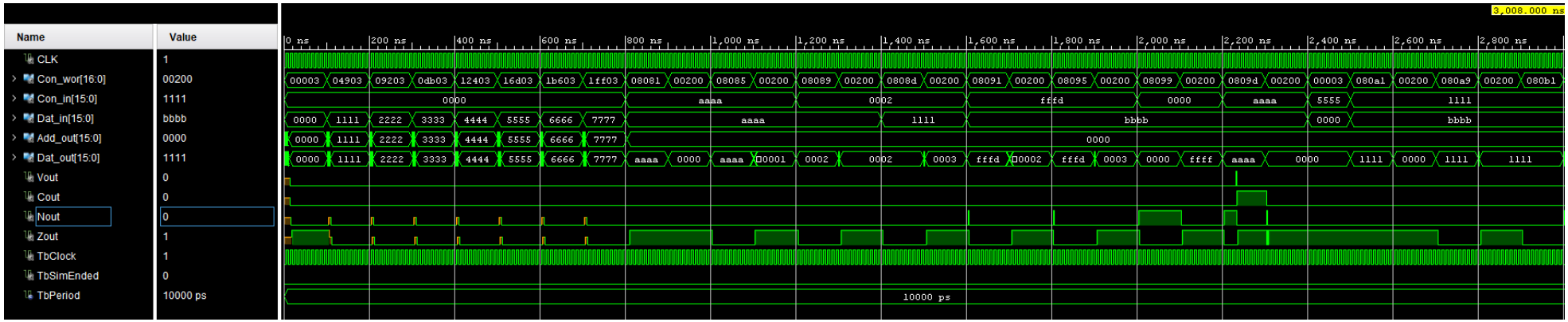
ALU



Functional Unit



Datapath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Value
CLK
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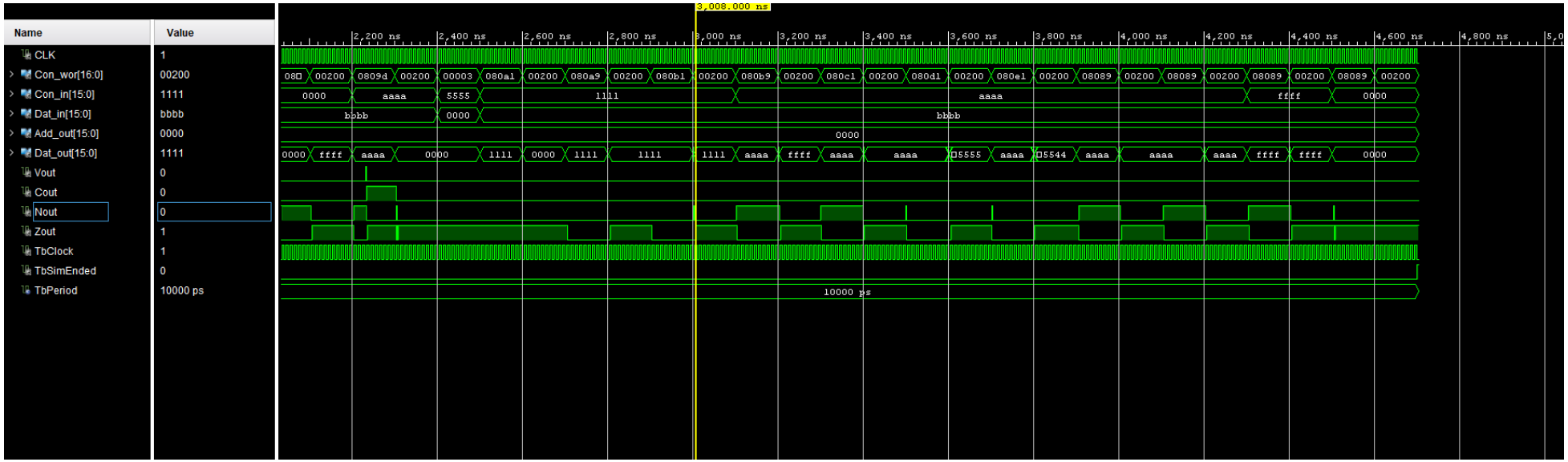
Con_in[15:0]
Dat_in[15:0]
Add_out[15:0]
Dat_out[15:0]
Vout
Cout
Nout
Zout
TbClock
TbSimEnded
TbPeriod
1
00200
1111
bbbb
0000
1111
0
0
0
1
1
0
10000 ps
3,008.000 ns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Vout
Cout
Nout
Zout
TbClock
TbSimEnded
TbPeriod
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1111
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0000
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0
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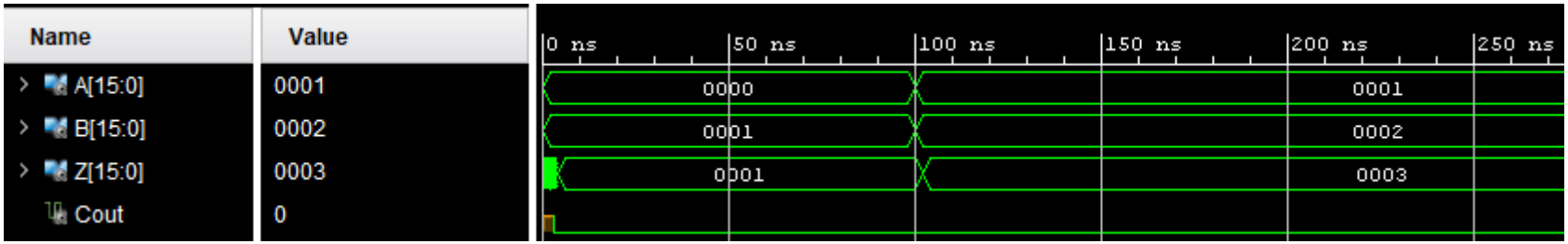
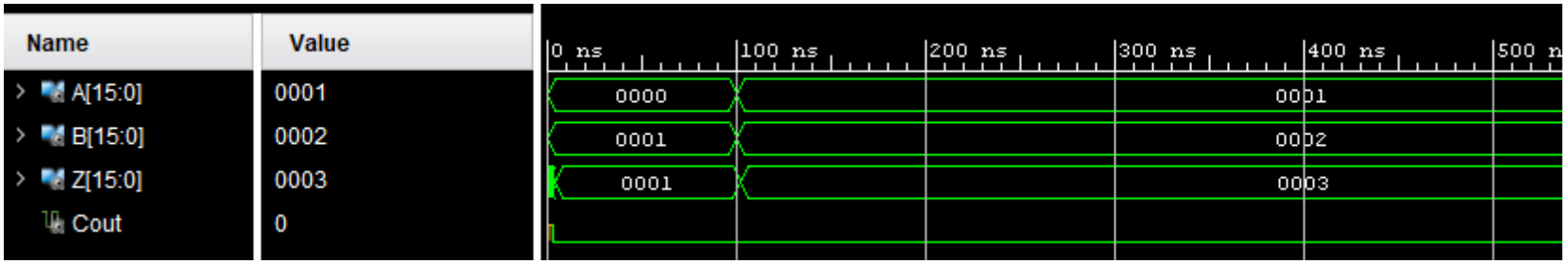
0
10000 ps
3,008.000 ns

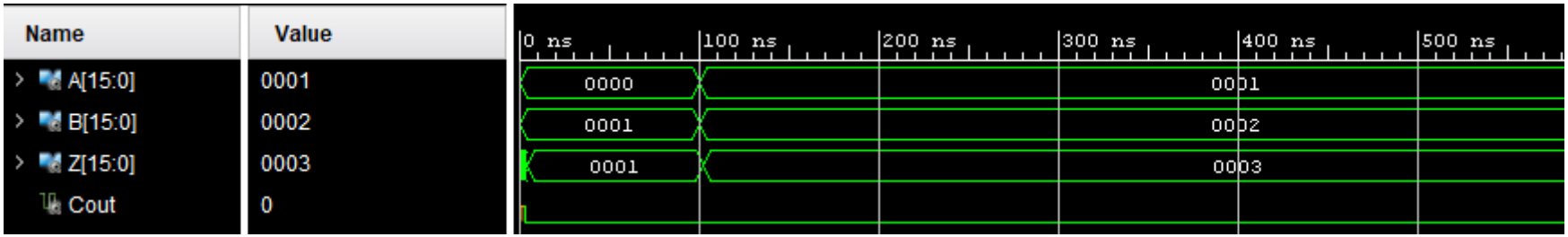
16 Bit Adder



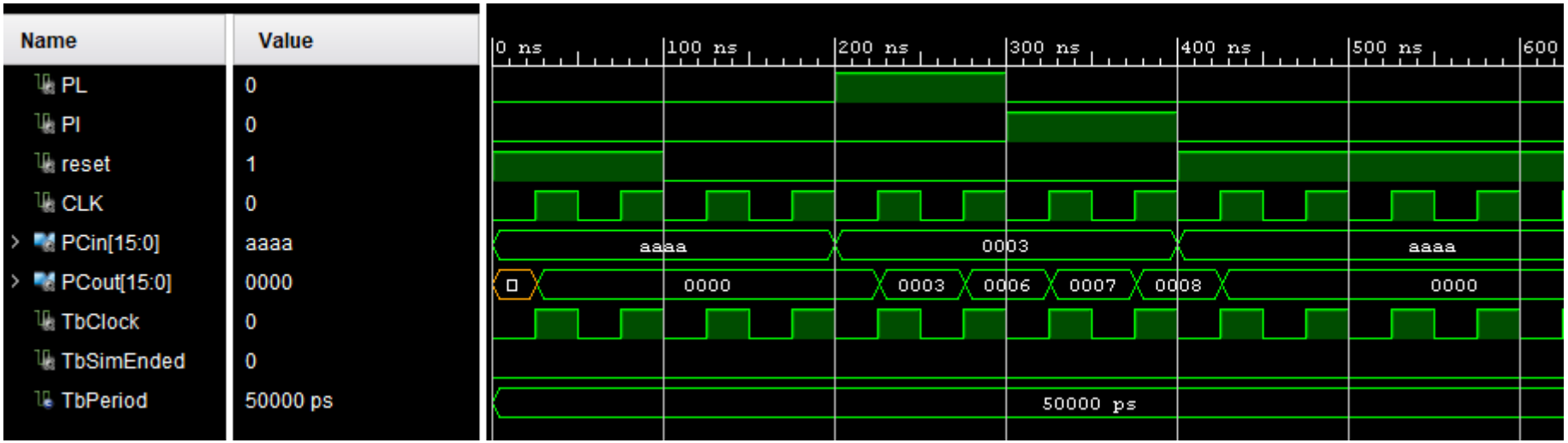
Control Address Register



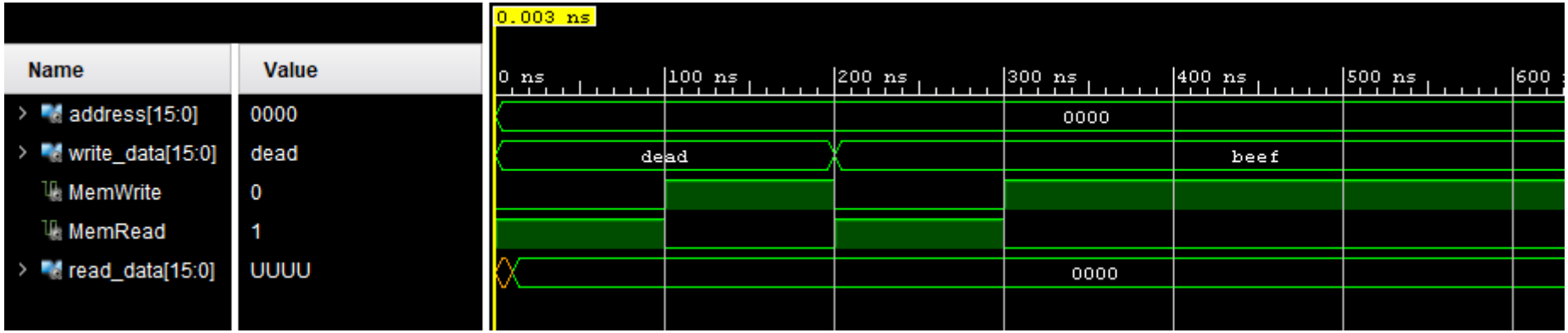
Instruction Register



Program Counter



Memory



Control Memory