2 Input Multiplexer

Name	Value	0 ns	50 ns	100 ns	150 ns 2
₩ In0	0				
₩a In1	1				
₩a s	1				
₩ Z	1				

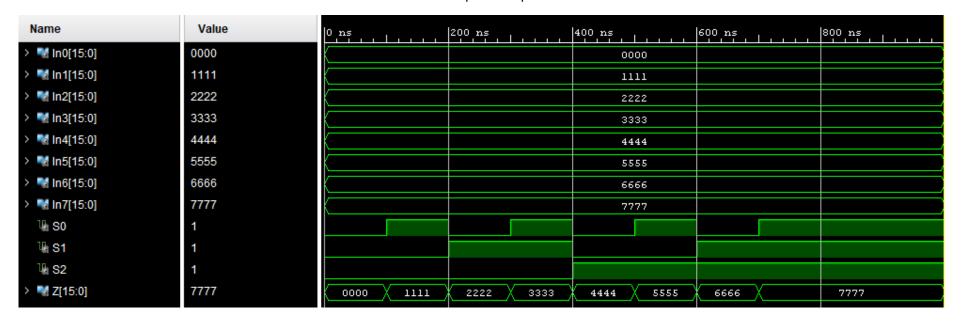
4 Input Multiplexer

Name	Value	0 ns	100 ns	200 ns	300 ns
⅓ In0	0				
¼ In1	1				
⅓ In2	0				
₩ In3	1				
₩ S0	1				
₩ S1	1				
₩z	1				

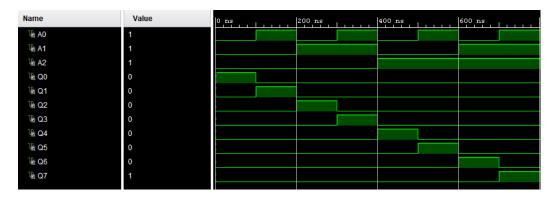
16 Bit 2 Input Multiplexer

Name	Value	0 ns	50 ns	100 ns	150 ns	200 ns	250 ns
> 🔣 In0[15:0]	0000				0000		
> 🔣 In1[15:0]	1111				1111		
₩ s	1						
> 🔣 Z[15:0]	1111	00	00	K		1111	

16 Bit 8 Input Multiplexer



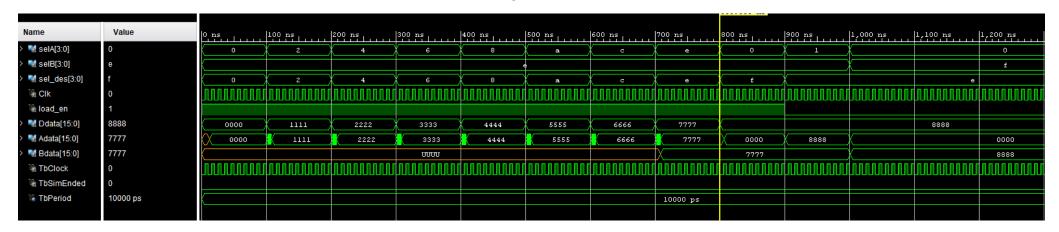
3 To 8 Decoder



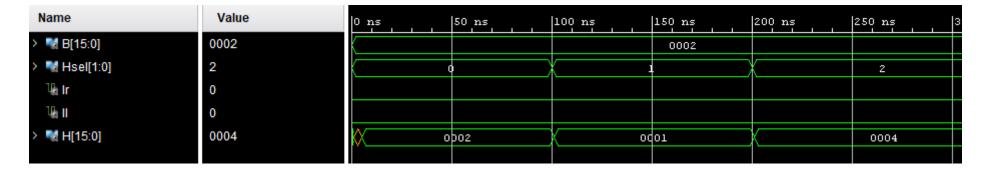
Register

Name	Value	0 ns	100 ns	200 ns	300 ns	400 ns	500 ns
> 🔣 D[15:0]	3333	00	00	1111	2222	K	3333
₩ load	1						
[™] Clk	0	\mathbf{M}					\mathcal{M}
> 🔣 Q[15:0]	3333	טטטט	0000	X 1	111	X	3333
₩ TbClock	0	10000000					\mathcal{M}
₩ TbSimEnded	0						
[™] TbPeriod	10000 ps				10000 ps		

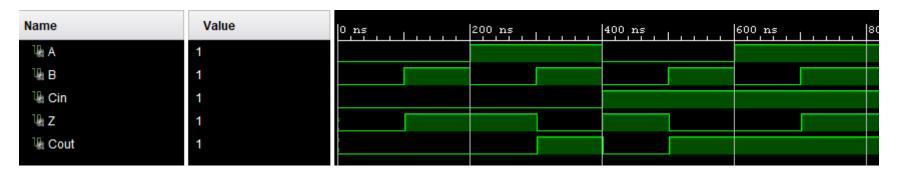
Register File



Shifter



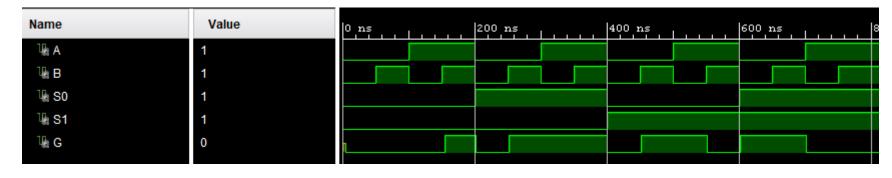
Full Adder



Arithmetic Bit Slice



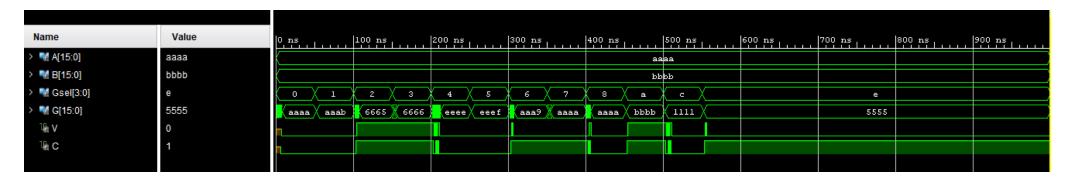
Logic Bit Slice



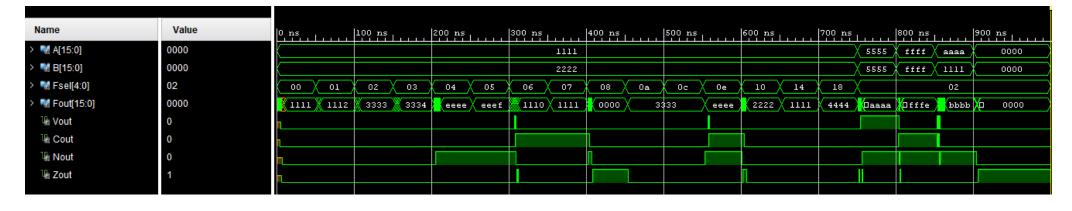
ALU Bit Slice

Name	Value	0 ns	50 ns	100 ns	150 ns	200 ns	250 ns	300 ns	350 ns	400 ns
¹la A	1									
Va B	0									
¹la Cin	0									
¹∄ S0	1									
Ū S1	1									
₩ S2	1									
₩ G	0					П				
₩ Cout	1			Í						

ALU

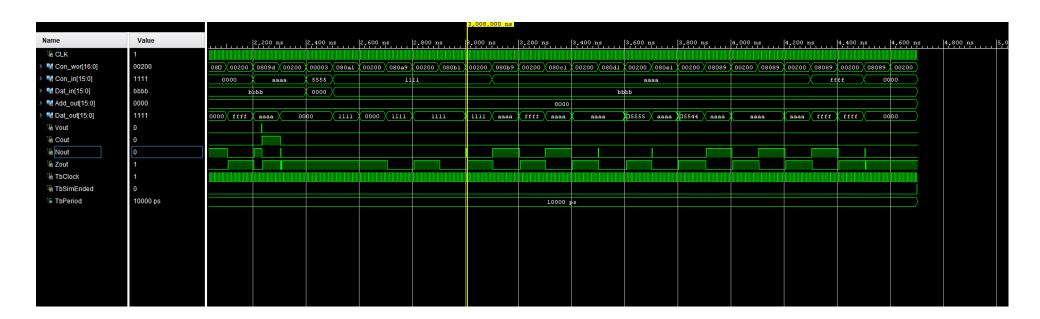


Functional Unit



Datapath

																											3,008.000
Name	Value	0 ns		200 ns		400 ns		600 ns		800 ns		1,000 ns	1,200 ns	1,	400 ns	1,600 ns	1	,800 ns	2,000	ns	2,200	ns	2,400	ns	2,600	ns	2,800 ns
₩ CLK	1																										
> 🔣 Con_wor[16:0]	00200	00003	04903	09203	0qP03	12403	16403	15603	1ff03	08081	00200	08085 00200	08089 002	00 0	8084 (00200)	08091 002	00 X	08095 00200	08099	00200	08094	00200	00003	080a	0020	080a9	00200 (080ы
> Con_in[15:0]	1111				00	00					as	aa	X	0002	:		fff	d	0	000	a	aaa	5555	χ		1111	
> 🦋 Dat_in[15:0]	bbbb	0000	1111	2222	3333	4444	5555	6666	7777	X		8888		$=$ $\!$	1111			bl	bbb				0000	χ		bbbb	
> 🔣 Add_out[15:0]	0000	0000	1111	2222	3333	4444	5555	6666	7777	X								0000									
> 🛂 Dat_out[15:0]	1111	0000	1111	2222	3333	4444	5555	6666	7777	aaaa	0000	aaaa X 00001	0002	0002	2 0003	fffd X0000	12	fffd 0003	0000	ffff	aaaa	χ ο	000	1111	0000	1111	1111
₩ Vout	0																										
™ Cout	0	I																									
™ Nout	0		П	1	ı	П	1		1																		
¼ Zout	1		1	li .																							
¼ TbClock	1		<u>Timili</u>	i i de la composición		1	imm.		İIIIII					ШΤ										$\Pi\Pi\Pi$			dononnonnon de la composición de la co
TbSimEnded	0																										
□ TbPeriod	10000 ps														10000 ps												



16 Bit Adder

Name	Value	0 ns	50 ns	100 ns	150 ns	200 ns	250 ns
> 🛂 A[15:0]	0001	00	00	K		0001	
> 🛂 B[15:0]	0002	00	01	*		0002	
> 🛂 Z[15:0]	0003	0	001	Χ		0003	
[™] Cout	0	1					

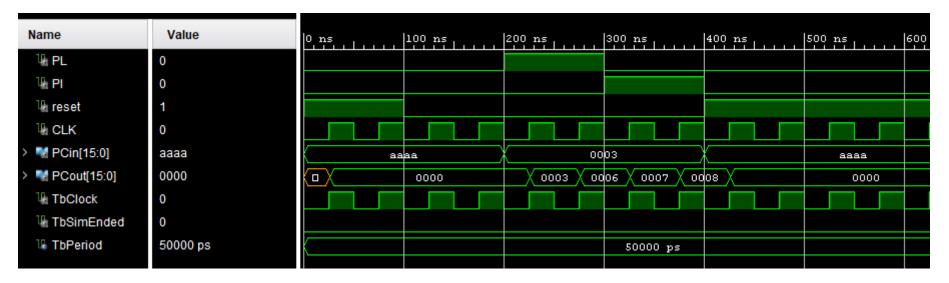
Control Address Register

Name	Value	0 ns	100 ns	200 ns	300 ns	400 ns	500 n
> 🔣 A[15:0]	0001	0000			00	01	
> M B[15:0]	0002	0001	k		00	02	
> 🔣 Z[15:0]	0003	0001	K		00	03	
¹₩ Cout	0						

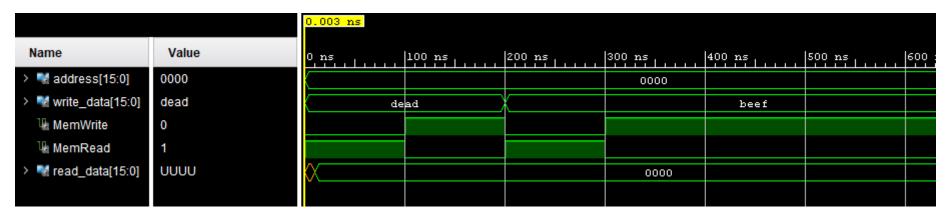
Instruction Register

Name	Value	0 ns	100 ns	200 ns	300 ns	400 ns	500 ns
> Nd A[15:0]	0001	0000			00	01	
> 🦬 B[15:0]	0002	0001			00	02	
> 🤻 Z[15:0]	0003	0001			00	03	
[™] Cout	0						

Program Counter



Memory



Control Memory

Name	Value
™ MW	0
Ue MM	0
₩ RW	0
¼ MD	0
■ FS[4:0]	00
₩ MB	0
₩ TB	0
[™] TA	0
₩ TD	0
₩ PL	0
₩ PI	0
¹la IL	0
₩ MC	0
MS[2:0]	0
▶ 🦬 NA[7:0]	00
N ■ N_CAR[7:0]	0d