Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	-	11	H3	17	PF1	I/O	FT	-	FSMC_A1 / I2C2_SCL / EVENTOUT	-
-	-	-	12	H2	18	PF2	I/O	FT	-	FSMC_A2 / I2C2_SMBA / EVENTOUT	-
-	-	-	13	J2	19	PF3	I/O	FT	(4)	FSMC_A3/EVENTOUT	ADC3_IN9
-	-	-	14	J3	20	PF4	I/O	FT	(4)	FSMC_A4/EVENTOUT	ADC3_IN14
-	-	-	15	K3	21	PF5	I/O	FT	(4)	FSMC_A5/EVENTOUT	ADC3_IN15
-	C9	10	16	G2	22	V_{SS}	S	-	-	-	-
-	B8	11	17	G3	23	V_{DD}	S	-	-	-	-
-	-	-	18	K2	24	PF6	I/O	FT	(4)	TIM10_CH1 / FSMC_NIORD/ EVENTOUT	ADC3_IN4
-	-	-	19	K1	25	PF7	I/O	FT	(4)	TIM11_CH1/FSMC_NREG/ EVENTOUT	ADC3_IN5
-	-	-	20	L3	26	PF8	I/O	FT	(4)	TIM13_CH1 / FSMC_NIOWR/ EVENTOUT	ADC3_IN6
-	-	-	21	L2	27	PF9	I/O	FT	(4)	TIM14_CH1 / FSMC_CD/ EVENTOUT	ADC3_IN7
-	-	-	22	L1	28	PF10	I/O	FT	(4)	FSMC_INTR/ EVENTOUT	ADC3_IN8
5	F10	12	23	G1	29	PH0/OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN(4)
6	F9	13	24	H1	30	PH1/OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT(4)
7	G10	14	25	J1	31	NRST	I/O	RST	-	-	-
8	E10	15	26	M2	32	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP/ EVENTOUT	ADC123_IN10
9	-	16	27	M3	33	PC1	I/O	FT	(4)	ETH_MDC/ EVENTOUT	ADC123_IN11
10	D10	17	28	M4	34	PC2	I/O	FT	(4)	SPI2_MISO / OTG_HS_ULPI_DIR / ETH_MII_TXD2 /I2S2ext_SD/ EVENTOUT	ADC123_IN12

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
11	E9	18	29	M5	35	PC3	I/O	FT	(4)	SPI2_MOSI / I2S2_SD / OTG_HS_ULPI_NXT / ETH_MII_TX_CLK/ EVENTOUT	ADC123_IN13
-	-	19	30	-	36	V_{DD}	S	-	-	-	-
12	H10	20	31	M1	37	V_{SSA}	S	-	-	-	-
-	-	-	-	N1	-	V_{REF-}	S	-	-	-	-
-	-	21	32	P1	38	V_{REF+}	S	-	-	-	-
13	G9	22	33	R1	39	V_{DDA}	S	-	-	-	-
14	C10	23	34	N3	40	PA0/WKUP (PA0)	I/O	FT	(5)	USART2_CTS/ UART4_TX/ ETH_MII_CRS / TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR/ EVENTOUT	ADC123_IN0/WKUP(4)
15	F8	24	35	N2	41	PA1	I/O	FT	(4)	USART2_RTS / UART4_RX/ ETH_RMII_REF_CLK / ETH_MII_RX_CLK / TIM5_CH2 / TIM2_CH2/ EVENTOUT	ADC123_IN1
16	J10	25	36	P2	42	PA2	I/O	FT	(4)	USART2_TX/TIM5_CH3 / TIM9_CH1 / TIM2_CH3 / ETH_MDIO/ EVENTOUT	ADC123_IN2
-	-	-	-	F4	43	PH2	I/O	FT	-	ETH_MII_CRS/EVENTOUT	-
-	-	-	-	G4	44	PH3	I/O	FT	-	ETH_MII_COL/EVENTOUT	-
-	-	-	-	H4	45	PH4	I/O	FT	-	I2C2_SCL / OTG_HS_ULPI_NXT/ EVENTOUT	-
-	-	-	-	J4	46	PH5	I/O	FT	-	I2C2_SDA/ EVENTOUT	-
17	H9	26	37	R2	47	PA3	I/O	FT	(4)	USART2_RX/TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / OTG_HS_ULPI_D0 / ETH_MII_COL/ EVENTOUT	ADC123_IN3
18	E5	27	38	-	-	V_{SS}	S	-	-	-	-

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
	D9			L4	48	BYPASS_REG	I	FT	-	-	-
19	E4	28	39	K4	49	V_{DD}	S	-	-	-	-
20	J9	29	40	N4	50	PA4	I/O	TTa	(4)	SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/ EVENTOUT	ADC12_IN4 /DAC_OUT1
21	G8	30	41	P4	51	PA5	I/O	TTa	(4)	SPI1_SCK/ OTG_HS_ULPI_CK / TIM2_CH1_ETR/ TIM8_CH1N/ EVENTOUT	ADC12_IN5/DAC_ OUT2
22	H8	31	42	P3	52	PA6	I/O	FT	(4)	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/ EVENTOUT	ADC12_IN6
23	J8	32	43	R3	53	PA7	I/O	FT	(4)	SPI1_MOSI/ TIM8_CH1N / TIM14_CH1/TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / ETH_RMII_CRS_DV/ EVENTOUT	ADC12_IN7
24	-	33	44	N5	54	PC4	I/O	FT	(4)	ETH_RMII_RX_D0 / ETH_MII_RX_D0/ EVENTOUT	ADC12_IN14
25	-	34	45	P5	55	PC5	I/O	FT	(4)	ETH_RMII_RX_D1 / ETH_MII_RX_D1/ EVENTOUT	ADC12_IN15
26	G7	35	46	R5	56	PB0	I/O	FT	(4)	TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N/ EVENTOUT	ADC12_IN8
27	H7	36	47	R4	57	PB1	I/O	FT	(4)	TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / TIM1_CH3N/ EVENTOUT	ADC12_IN9
28	J7	37	48	M6	58	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-