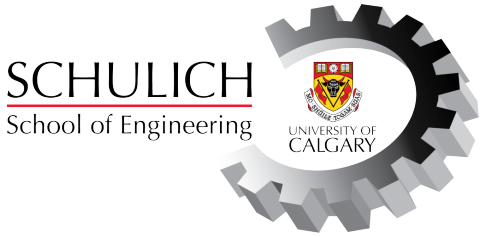


Department of Electrical and Computer Engineering

ENEL 453: Digital System Design

Fall 2017

Lab 5: Distance Measurer

1 Overview

In this lab project, you will design and implement a Distance Measuring system using the Sharp GP2Y0A41SK0F distance sensor. The distance sensor uses an infrared LED and outputs an analog voltage which you will read, transform into a distance measurement, and display the distance on a VGA monitor. You will use the FPGA and external components to design and implement an Analog-to-Digital Converter (ADC). You may use your code for the VGA Controller and PWM DAC, as well as any other of your code developed in past labs. You will also write a technical report and record a video presentation. The distance sensor will be obtained from our technicians.

This lab project is worth 40% of your final grade and is broken up as:

- Pre-lab: none
- In-lab simulation: required for design walkthrough
- In-lab demonstration and design walkthrough: 20%
- Technical Report: 10%
- Video Presentation: 10%

Lab sections B01 and B03 must present their demonstration during their last lab period, December 1, or earlier. Their technical report will be due at the end of the day December 1.

Lab sections B02 and B04 must present their demonstration during their last lab period, December 8, or earlier. Their technical report will be due at the end of the day December 8.

Late work will not be accepted unless accommodated for circumstances similar to accommodations given for deferral of final examinations: including debilitating illness, severe domestic affliction, religious conviction or absence due to a faculty-approved activity. ***Students are strongly encouraged to use their time effectively and complete the lab project in a timely manner.***

All team members can expect to answer questions regarding any aspect of the project ***and weak answers from any team member may result in grade reductions for the team***.

Note: To design this system, create a block diagram with sub-blocks, like in the previous labs, to help guide your design process. Design, build, and test incrementally and avoid attempting to design a complex system in one grand effort.

See the example circuit and explanation at the end of this document for a high-level overview of the basic requirements.

2 DELIVERABLES

The design project must include the following features: system reset, synchronous design, and debounced inputs as appropriate. Any deviations from this project handout will need to be approved in advance by both instructors, on the basis of whether it enhances student learning and follows the spirit of the project.

2.1 DEGREES OF COMPLETION

2.1.1 MINIMUM VIABLE PROJECT (MAXIMUM 15% FROM 40%)

In order to fulfill the Course Outline's requirement that "all course assignments must be completed to pass the course," the minimum requirements below must be met in order for the lab project to be considered completed.

Basic Technical Requirements (5%)

- A discrete ADC must be created with the FPGA and external components. An interface to an existing ADC is not acceptable. Use the "ADC and DAC" PDF on D2L for guidance and the Digital Ramp ADC (also known as a Ramp-Compare ADC) will probably be the easiest to implement.
- A PWM DAC (i.e. from Lab 4) must be used within the ADC.
- The analog voltage from the distance sensor must be converted to a distance in centimeters and presented on the 7-segment displays (as used in Lab 2), to three significant digits, e.g. 27.2 cm, and using the 7-segment display decimal point.
- The distance measured must range from 4.0 cm to 30.0 cm and the readout must be reasonably accurate. Recall that the distance sensor's analog output voltage is a non-linear function of distance (page 4 of sensor data sheet), so this must be taken into account.
- Continuous distance measurement, so varying the distance of an object from the sensor, will result in real-time changes in the distance presented on the 7-segment displays.

The grading will be as follows

- Pre-lab: none
- In-lab simulation: required for design walkthrough
- In-lab demonstration and design walkthrough: 5%
- Technical Report: 5%
- Video Presentation: 5%

Both the technical report and the video presentation will each be graded out of 10%, but they will be scaled down by 50% to reflect the lower technical achievement of the project. Example, a technical report that receives 8/10 according to the rubric will be scaled down to 4/10 for the minimum viable project.

Demonstration Rubric for Minimum Viable Project (5%)

Fails (0)	Demonstration of prototype does not show measurement of distance and reporting of reasonable result on 7-segment displays; OR PWM DAC is not used; OR a discrete ADC is not implemented and used; OR team is unable to explain their design during the design walkthrough and questions (this will be confirmed by a subsequent instructor meeting with the team during the demonstration lab period, as this will result in a failing grade for the course).
Below (1)	Poor design practice demonstrated, such as: no debouncing and synchronization of switch or pushbutton inputs; OR synchronous design violated; OR very few or no testbenches developed for testing; OR simulations to run the testbenches in demonstration do not work or do not reasonably test the design; OR poor mapping of nonlinear sensor input leading to poor distance measurement readings; OR full distance range of 4 - 30 cm is not measured; OR poor responses to design walkthrough and questions (all team members may be asked questions).
Meets (3)	All requirements for the distance measuring system (minimum viable project) have been met but there may be: minor omissions in testbenches; OR minor problems explaining design during walkthrough and questions; OR some clearly poor approaches for the system design despite having a working system.
Exceeds (5)	All requirements are met, the design is reasonable, a full suite of testbenches are presented, and the design walkthrough and answering of questions is well-done. There are no FPGA timing violations. The accuracy of the distance measuring system is better than +/- 1 cm, at any random distance within the measurement range.

2.1.2 COMPLETE PROJECT (40%)

In order to fully complete the project, following requirements must be met.

Basic Technical Requirements (10%)

- A discrete ADC must be created with the FPGA and external components. An interface to an existing ADC is not acceptable. Students are free to use whatever ADC architecture that interests them, whether it involves an internal DAC or not. Use the "ADC and DAC" PDF on D2L for guidance.
- The analog voltage from the distance sensor must be converted to a distance in centimeters and presented on the VGA monitor, to three significant digits, e.g. "27.2 cm" using a decimal point and units. No bouncing distance measurements on the VGA monitor, please (see note below).
- The distance measured must range from 4.0 cm to 30.0 cm and the readout must be reasonably accurate. Recall that the distance sensor's analog output voltage is a non-linear function of distance (page 4 of data sheet), so this must be taken into account.

Creative Technical Requirements (10%)

The creative requirements will be developed by the team, to extend the functionality of the design project. Grading will be at the discretion of the TA at the time of presentation and will reflect the degree of challenge and accomplishment. Sample creative directions may include some or all of (but not limited to) the following.

- Ability to switch between units, e.g. cm, mm, and inches.
- An alarm for detecting object within or outside an adjustable range.
- A technical deep-dive into ADC architectures and creation of a more design intensive and higher performance ADC. Examples: sample-and-hold; Flash, Delta-Sigma, or Successive Approximation ADCs; over-sampling and averaging to improve SNR. This is a good option for students particularly interested in circuit design. If you chose Delta-Sigma ADC, do not try to implement noise shaping and decimation, unless you want to do the equivalent of a master's degree with your project.
- A calibration system to ensure accuracy of the sensor (the graph on page 4 of the datasheet is the typical performance, individual sensor performance may vary).
- Ability to switch to measure distance between 0.0 to 4.0 cm (tricky).
- A self-test diagnostic mode or start-up state to ensure the distance measurer system is in a functional state. Example: one test may be to loop back a DAC output to the ADC input, and measure the DAC across a range of values and check that the expected ADC inputs are correct.
- A data log of distance measurements over time, on the VGA monitor, displayed, say, as a table.
- A low-pass filter to limit input frequencies to those consistent with the Nyquist sampling frequency of the ADC.

For the creative requirements, come up with logical and reasonable rationales for why you chose your requirements. For example, a bouncing distance measurement with changing rainbow colors on the VGA

monitor wouldn't make much sense for an engineering application, but perhaps can be justified for a marketing application.

The grading will be as follows

- Pre-lab: none
- In-lab simulation: required for design walkthrough
- In-lab demonstration and design walkthrough (basic requirements): 10%
- In-lab demonstration and design walkthrough (creative requirements): 10%
- Technical Report: 10%
- Video Presentation: 10%

Please be very careful to develop your creative technical requirements, so that you do not take on a challenge that ends up being too great. As EVDS professor Barry Wylant says that the "design challenge is to make sense of things before they exist," so you must make an assessment based on your confidence in your high-level design understanding of your creative technical requirements.

Demonstration Rubric for Basic Requirements (10%)

Fails (0)	Demonstration of prototype does not show measurement of distance and reporting of reasonable result on VGA monitor; OR a discrete ADC is not implemented and used; OR team is unable to explain their design during the design walkthrough and questions (this will be confirmed by a subsequent instructor meeting with the team during the demonstration lab period, as this will result in a failing grade for the course).
Below (3)	Poor design practice demonstrated, such as: no debouncing or no synchronization of switch or pushbutton inputs; OR synchronous design violated; OR very few or no testbenches developed for testing; OR simulations to run the testbenches in demonstration do not work or do not reasonably test the design; OR poor mapping of nonlinear sensor input leading to poor distance measurement readings; OR full distance range of 4 - 30 cm is not measured; OR poor responses to design walkthrough and questions.
Meets (7)	All requirements for the distance measuring system have been met but there may be: minor omissions in testbenches; OR minor problems explaining design during walkthrough and questions; OR some clearly poor approaches for the system design despite having a working system.
Exceeds (10)	All requirements are met, the design is reasonable, a full suite of testbenches are presented, and the design walkthrough and answering of questions is well-done. There are no FPGA timing violations. The accuracy of the distance measuring system is better than +/- 1 cm, at any random distance within the measurement range.

Demonstration Rubric for Creative Requirements (10%)

Fails (0)	Creative component not completed or too minimal to be awarded points; OR team is unable to explain their creative design component during the design walkthrough and questions.
Below (3)	Modest effort and accomplishment demonstrated (e.g. only additional functionality is ability to switch between distance units - cm, mm, inches) OR poor design practice demonstrated; OR poor responses to design walkthrough and questions.
Meets (7)	Significant effort and accomplishment is demonstrated (e.g. comparable to the effort to meet the Basic Requirements) but there may be: minor omissions in testbenches; OR minor problems explaining design during walkthrough and questions; OR some clearly poor approaches for the creative component.
Exceeds (10)	Significant effort and accomplishment is demonstrated (e.g. equal to or greater than the effort to meet the Basic Requirements), the design is reasonable, a full suite of testbenches are presented, and the design walkthrough and answering of questions is well-done. There are no FPGA timing violations.

2.1.3 Demonstration Format

Student teams will be graded by a 2-person TA grading team in an 8-minute time slot during the lab period. The sequence will be:

- Team demonstrates working system and identifies creative design features.
- TAs verify distance measurement accuracy of the system and functionality of system.
- Team gives design walkthrough of system: hardware, RTL Schematic, VDHL, and simulations. All team members must participate.
- TAs ask team questions about the design and any team member may be asked a question.
- TAs confer to assign grades according to the rubric.

The TAs will take notes during the presentation.

2.1.4 Technical Report and Presentation

The requirements and grading rubric will be provided in a separate document.

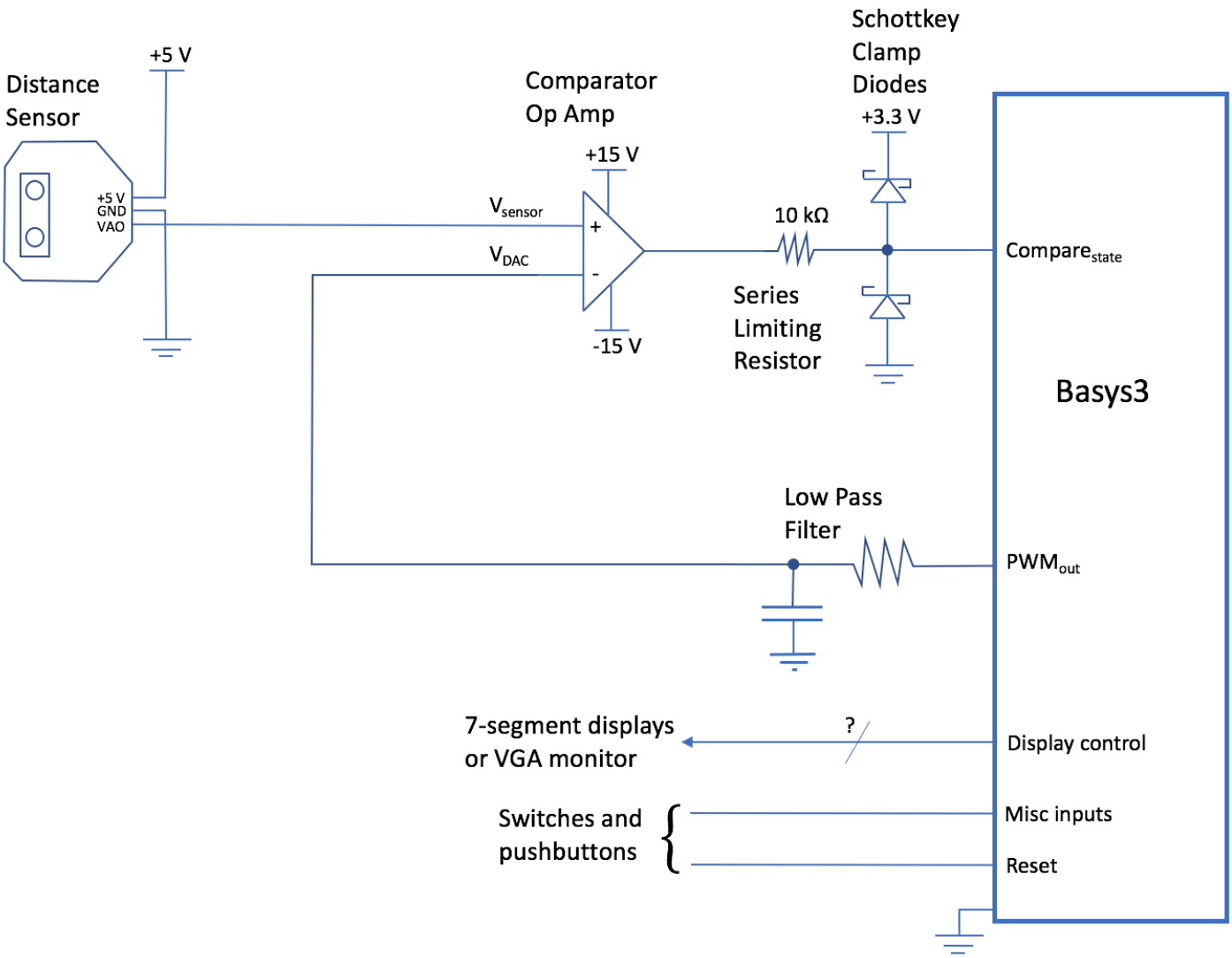
3 EXAMPLE HIGH-LEVEL OVERVIEW

The circuit below is an example to illustrate the basic operation of the distance measuring system using the Ramp-Compare ADC architecture. Please refer to the diagram on the following page.

1. PWM_{out} generates a PWM output which results in a sawtoothed 0V to 3.3V waveform (V_{DAC}), using a counter whose current count value is named *saw_count*.
2. The distance sensor produces an analog voltage (V_{sensor}) which is related to the distance of an object from the sensor.
3. The output of the comparator op amp is +15V when V_{sensor} is greater than V_{DAC}., e.g. when V_{DAC} is starting to ramp up. As V_{DAC} continues to ramp up, it will exceed the V_{sensor} value and the output of the comparator op amp will switch to -15V.
4. The output comparator op amp is connected to the FPGA using a protection circuit described later, and goes to the FPGA input $Compare_{state}$. When the signal to $Compare_{state}$ transitions from +15V to -15V, then the V_{sensor} and V_{DAC} will be approximately equal and *saw_count* will have a value that corresponds to the voltage value of V_{sensor}.
5. Once the FPGA detects the above high-to-low transition on $Compare_{state}$, it captures the value of *saw_count* and registers it. Then the FPGA maps the value of *saw_count* to a distance value (using perhaps a look-up table or by a calculation), and keeping account of the non-linear relationship of the V_{sensor} voltage-to-distance (according to page 4 of the distance sensor data sheet).
6. The FPGA outputs the distance value to the display, which can be the 7-segment displays or the VGA monitor.

Protection circuit: The circuit below is required to interface the comparator Op Amp to the Basys3 Pmod port. This circuit with the 10 kΩ series limiting resistor and two Schottkey clamping diodes will protect the Basys3 from overvoltage from the Op Amp's output (+15V to -15V), when creating the ADC.

- The op amp's output voltage swing is +/-15V, and will likely cause damage if put directly to the FPGA's input which is nominally tolerant of 0V to +3.3V.
- The Schottkey diodes clamp the voltage to safe values, in conjunction with the 10kΩ series limiting resistor. The Schottkey diodes have a forward voltage drop of 0.2V.
- If the op amp outputs +15V, then current flows through the series limiting resistor and into the top Schottkey diode. The voltage at $Compare_{state}$ will be 3.3V + 0.2V = 3.5V, which will be tolerable to the FPGA because some additional internal protection circuitry in the FPGA. The current through the resistor and top Schottkey diode will be (15V - 3.5V)/ 10kΩ = 1.15mA.
- If the op amp outputs -15V, then current flows through the series limiting resistor and from the bottom Schottkey diode. The voltage at $Compare_{state}$ will be 0V - 0.2V = -0.2V, which will be tolerable to the FPGA because some additional internal protection circuitry in the FPGA. The current through the resistor and bottom Schottkey diode will be (-15V - (-0.2V))/ 10kΩ = -1.48mA.


Distance Sensor
+5 V
+5 V
GND
VAO
Comparator Op Amp
+15 V
V_{sensor}
V_{DAC}
+
-
-15 V
Schottkey Clamp Diodes
+3.3 V
10 kΩ
Series Limiting Resistor
Compare$_{state}$
Basys3
Low Pass Filter
PWM$_{out}$
7-segment displays or VGA monitor
?
Display control
Switches and pushbuttons
Misc inputs
Reset