Subranging ADC requirements:

- 8 bit digital input/output to allow us to have enough digital readings to make sure we can have 3 significant digits for distances between 4 and 40 cm
- We believe this will require:
    - 34 op amps
    - 1 nmos transistor
    - 54 resistors
    - 12 digital inputs to Basys 3 board
    - 8 digital outputs from basys 3 board
- Here is our reasoning

Color code:

- **Blue: components**
- **Green: digital input outputs**
- **Yellow: questions**

Total Components:

- Op-amps
    - 35 if 2 used for sample and hold, 1 used for differential, 1 used for amplification, 1 used for R2R DAC and 15 used for each of the 2 4 bit flash ADC's
    - 34 if 2 used for sample and hold, 1 used for differential combined with amplifier, 1 used for R2R DAC and 15 used for each of the 2*4 bit flash ADC's
- Resistors:
    - 54
- Transistors:
    - 1 nmos if single nmos used for sample and hold
    - 1 nmos and 1 pmos if Cmos logic used for sample and hold

Total I/0 = 40, 16 or 20

- 8 digital outputs for R2R DAQ
- 32 digital inputs if encoding done inside FPGA: to many input/outputs
    - Must do encoding externally
- 8 digital inputs if encoding done on externally
    - Cant find 16-4 encoder on digikey
- 12 digital inputs since we cant find a 16-4 encoder, but can find a 8-3 encoder

Subranging overall:

- http://analoglib.net/2013-09-17/dingwall-jssc-85-an-8-mhz-cmos-subranging-8-bit-adc/
- https://www.physics.queensu.ca/~phys352/lect08.pdf
- 35 or 34 op-amps:
    - Q: what should op amp rail voltage values be

- Q: should we worry about the propagation delay of op amps
- Q: how will the FPGA know the total delay between FPGA reading 4 * MSB to reading 4 * LSB?
  - Aka: how do we match our most significant bits to our least significant bits

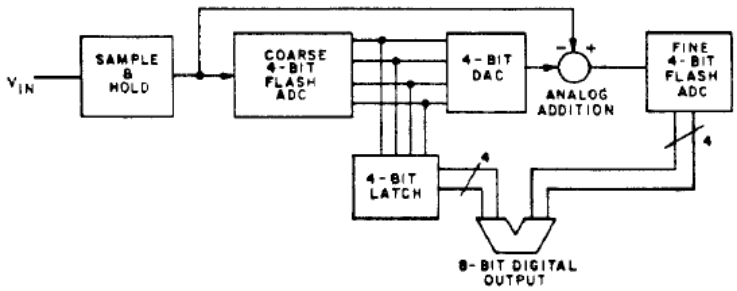
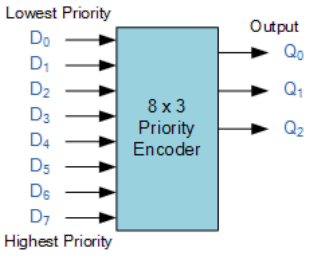


Fig. 1. Conventional 8-bit subranging ADC.

Encoder:

- http://www.electronics-tutorials.ws/combination/comb_4.html
- Encoding must be done off board in order to keep input output signals under 24
- 8-3 encoder digikey: https://www.digikey.ca/product-detail/en/texas-instruments/SN74HC148N/296-8233-5-ND/376979



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

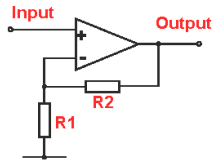
X = dont care

Non-inverting op amp:

- http://www.radio-electronics.com/info/circuits/opamp_basics/operational-amplifier-gain.php
- Not needed if we implement amplification into differential amplifier
- Need to amplify by 2^4 = 16
- 2 resistors
- 1 op amp
- Gain = vout/Vin = 1 + R2/R1
- R2 = 15 kOhm
- R1 = 1 kOhm

Non-Inverting op-amp gain

The circuit for the non-inverting op-amp is shown below. It offers a higher input impedance than the inverting op amp circuit.



Basic non-inverting operational amplifier circuit

The gain of the non-inverting circuit for the operational amplifier is easy to determine. The calculation hinges around the fact that the voltage at both inputs is the same. This arises from the fact that the gain of the amplifier is exceedingly high. If the output of the circuit remains within the supply rails of the amplifier, then the output voltage divided by the gain means that there is virtually no difference between the two inputs.

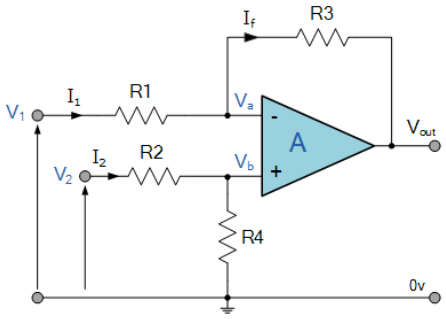
As the input to the op-amp draws no current this means that the current flowing in the resistors R1 and R2 is the same. The voltage at the inverting input is formed from a potential divider consisting of R1 and R2, and as the voltage at both inputs is the same, the voltage at the inverting input must be the same as that at the non-inverting input. This means that Vin = Vout x R1 / (R1 + R2). Hence the op amp gain equation for the voltage gain of the circuit Av can be taken as:

$$\frac{V_{out}}{V_{in}} = A_V = 1 + \frac{R_2}{R_1}$$

Differential Amplifier:

- http://www.electronics-tutorials.ws/opamp/opamp_5.html
- 4 resistors
- 1 op amp
- Can potentially amplify by 2^4 = 16
- If R1 = R2 and R3 = R4 then
    - Vout = R3/R1(V2-V1)
- Therefore, if R3 = R4 = 16 kOhm, and R1 = R2 = 1 kOhm, there would be no need for a non inverting op amp circuit!

Differential Amplifier



Sample and hold circuit:

- http://www.d.umn.edu/~htang/ECE5211_doc_files/ECE5211_files/Chapter11.pdf
- Q: how long would we need to hold it

- 2 op-amps
    - 1: input to keep vin stable and not load bearing
    - 2: output to better drive voltage signal to encoder
- Nmos transistor
- Or Cmos logic

11.2 sample and hold basics

The simplest implementation of a S&H circuit is shown below.

The voltage V' would ideally stay constant in the hold mode by having a value equal to V_{in} at the instance of clock going low. But there are two error sources due to switch:

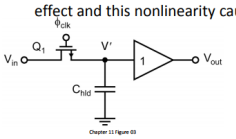
1. The channel charge go to both junctions to causes negative glitches. If source impedance of V_{in} is small, then the glitch is small and last a short duration.
2. The channel charge go to V' causes a negative voltage that is long lasting.

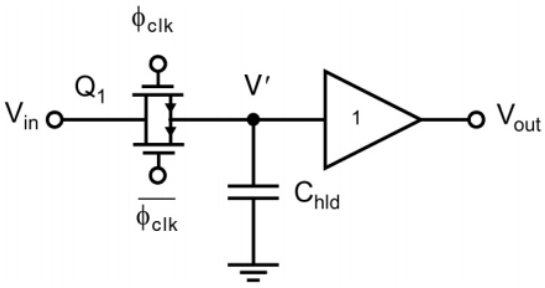
$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{ox}WLV_{eff\text{-}1}}{2} \qquad V_{eff\text{-}1} = V_{GS1} - V_{tn} = V_{DD} - V_{in} - V_{tn}$$

Here V_{in} is the input voltage at the moment Q1 turns off.

$$\Delta V' = \frac{\Delta Q_{C\text{-}hld}}{C_{hld}} = -\frac{C_{ox}WLV_{eff\text{-}1}}{2C_{hld}} = -\frac{C_{ox}WL(V_{DD} - V_{tn} - V_{in})}{2C_{hld}}$$

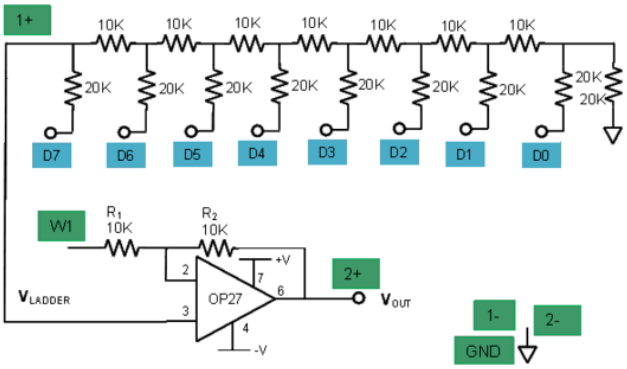
This error is linearly related to V_{in}, therefore causes a linear error (called gain error), but this error is also related to V_{tn}, which is nonlinearly related to V_{in} due to body effect and this nonlinearity causes harmonics.





R2r:

- https://wiki.analog.com/university/courses/electronics/electronics-lab-14
- 1 op amp
- 8 output signals from FPGA
- 9 * 20 kOhm resistors
- 9 * 1 kOhm resistors



Flash adc (2 of these):

- https://www.allaboutcircuits.com/textbook/digital/chpt-13/flash-adc/
- Vref = 3.1 since input input max is 3.05
- 16 - 1 op amps and resistors will allow us to have a 4 bit input
- 2*15 op amps
- 2*15 resistors;

- Q: can this be any resistance value? Would bigger be better?

- 2*16 input voltages to FPGA if we do encoding inside fpga
- 2*4 input voltages to FPGA if we do encoding externally
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