ROBERT RIORDAN

Electronic Engineer with a ME in Electronic and Computer Engineering

DIGITAL LOGIC DESIGN ENGINEER

Intel *July 2021 - March 2024*

- Worked on the digital design of a PCIe interface controller for Intel's IPU products.
- Maintained and updated top level RTL interface and partition level connectivity, using Synopsys coreTools and Intel's tools for SystemVerilog generation.
- Created Python scripts to flag discrepancies between RTL and architecture specification.
- Created a Python script to automatically insert feed-throughs into the design.
- Learned to use new tools and languages on the jobs, such as TCL, UPF, coreTools, CDC, and Jasper.
- Integrated 3rd party IPs into the project, such as thermal and voltage sensors, and controllers.
- Integrated tools into release flow for automated code validation and quality assurance.
- Worked with a large multi-disciplinary team developing Intel's IPU products.
- Worked on Intel's IPU project from the initial architecture stage, through to final RTL delivery.

ANALOG AND MIXED SIGNAL INTERN

Xilinx *January 2020 - August 2020*

- Worked with both digital design and verification teams to create Xilinx's RF SoCs.
- Designed and implemented a digital Cascaded Integrator-Comb filter in Verilog.
- Verified the Cascaded Integrator-Comb filter using MatLab and SystemVerilog.
- Created verification sequences for a complex multiplier.
- Created Python scripts to verify the implementation of team members testbenches.

RESEARCH ENGINEER INTERN

Insight Centre for Data Analytics *June 2019 - September 2019*

- Modeled crowd flow dynamics using 3D motion capture technology.
- Designed and developed Python scripts to convert 3D motion capture data into CSV format.
- Developed algorithms to measure stride length and inter-person distance in MatLab.
- Implemented a linear regression model to predict these dynamic features.
- Analysed accelerometry data in swimmers using MatLab to identify useful features.

EDUCATION

University College Dublin *September 2019 - May 2021*
ME Electronic and Computer Engineering Second Class Honours, Grade 1
Thesis: Multigroup Multicast Cell-free Massive MIMO
I developed novel equations to model and load balance power consumption in a multigroup multicast cell-free massive MIMO network and created a MatLab simulation to compare my solutions with the contemporary solutions.

University College Dublin *September 2016 - May 2019*
BSc Engineering Science, Major in Electronic Engineering Second Class Honours, Grade 1

PROJECTS

I program confidently in Python, MatLab, and SystemVerilog, using both Windows and Linux operating systems, and I have experience with many other languages such as C/C++ and Java. Some examples include

Verilog:	Designed and implemented a basic calculator to run on a FPGA.
PCB Design:	Designed and built an 8-bit computer.
C:	Programmed an arduino to validate each module in the 8-bit computer.
RobotC:	Built and programmed a line following robot.
Java:	Replicated the board game *Forbidden Island* in the terminal.
Python:	Designed and programmed a Rubik's Cube simulator in the terminal.
Python:	Created a program to validate if a juggling pattern is possible.
Micropython:	Created a pomodoro timer with a rp2040 and designed and 3d printed a housing for the device.
MatLab:	Modeled a three body solar system of the Sun, Earth, and Moon.

SKILLS AND INTERESTS

- I enjoy learning many new skills including juggling, unicycling, solving Rubik's Cube, and diabolo.
- I held the positions of auditor, treasurer, and secretary for the UCD Juggling and Circus Society while in UCD.
- I organised many workshops, regular training sessions, national competitions and conventions, and society trips, while on the UCD Juggling and Circus Society committee.
- I am an avid rock climber and sailor, and worked as a sailing instructor throughout my time in college, prior to becoming an engineer.
- I have competed in several regional, national, and inter-varsity sailing events.

References available upon request.