SE350 Lab1 Tutorial

Introduction to MCB1700 and Keil IDE

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P1 Requirements : API

- Memory Management: a memory pool which has fixed size of memory block and fixed number of memory blocks.
  - void * request_memory_block ()
  - int release_memory_block (void * MemoryBlock)
- Processor Management
  - int release_processor ()
- Process Priority Management
  - int set_process_priority (int process_ID, int priority)
  - int get_process_priority (int process_ID)

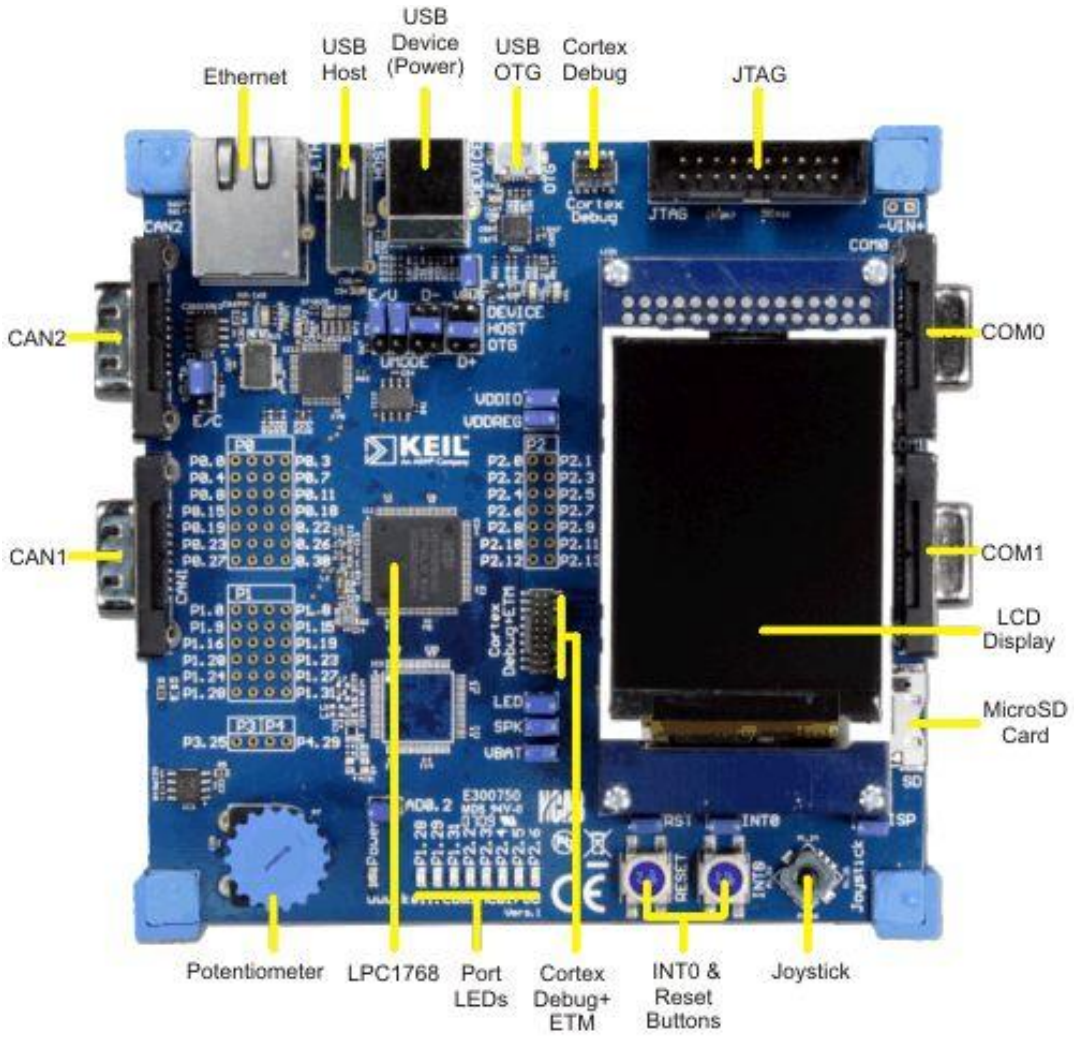
P1 Requirements: Processes

- Null Process
  - A system process which does nothing in an infinite loop. PID=0.
- Test Processes
  - Up to six test processes with PIDs = 1,2, …, 6
  - User level processes, only calls the user APIs
- Initialization
  - Memory, system processes and user processes

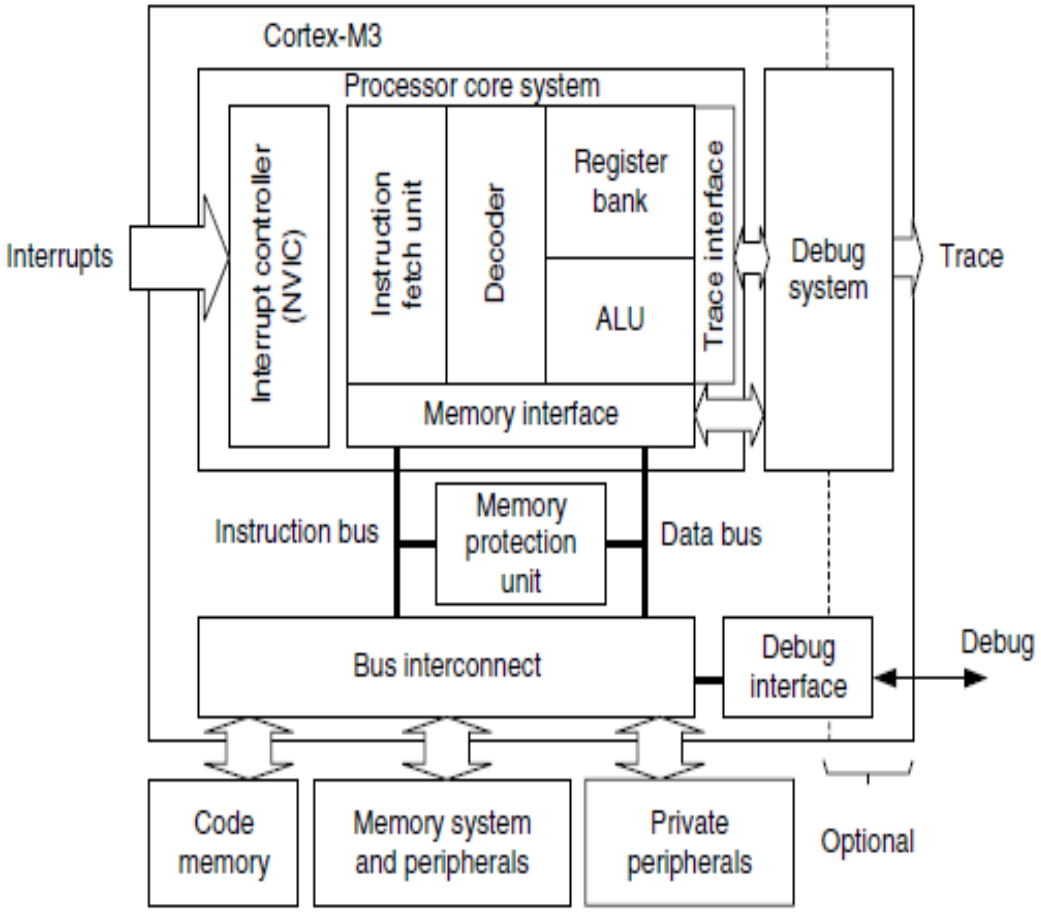
All processes never terminate!
No new process created on the fly.

Keil MCB 1700 Board

- Cortex-M3 Processor
- NXP LPC1768 MCU
- Up to 100 MHZ cpu
- One SystemTick Timer
- Four Timers
- Four UARTs
- Many other cool stuff…



Cortex-M3 Overview



(Image Courtesy of [1])

- 32-bit microprocessor
  - 32-bit data path
  - 32-bit register bank
  - 32-bit memory interface
- Harvard Architecture
  - Separate data and memory bus
  - instruction and data buses share the same memory space (a unified memory system)

Cortex-M3 Registers

- General Purpose Registers (R0-R15)
  - Low registers (R0-R7)
    - 16-bit Thumb instructions and 32-bit Thumb-2 instructions
  - High registers (R9-R12)
    - All Thumb-2 instructions
  - Stack Pointer (R13)
    - **MSP:** Privileged, default after reset, os kernel, exception handler
    - **PSP:** Uer-level (i.e. unprivileged) base-level application
  - Link Register (R14)
  - Program Counter (R15)
- Special Registers
  - Program Status registers (PSRs)
  - Interrupt Mask registers (PRIMASK, FAULTMASK, and BASEPRI)
  - Control register (CONTROL)

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Low registers: R0-R7
16-bit Thumb instructions
32-bit Thumb-2 instructions
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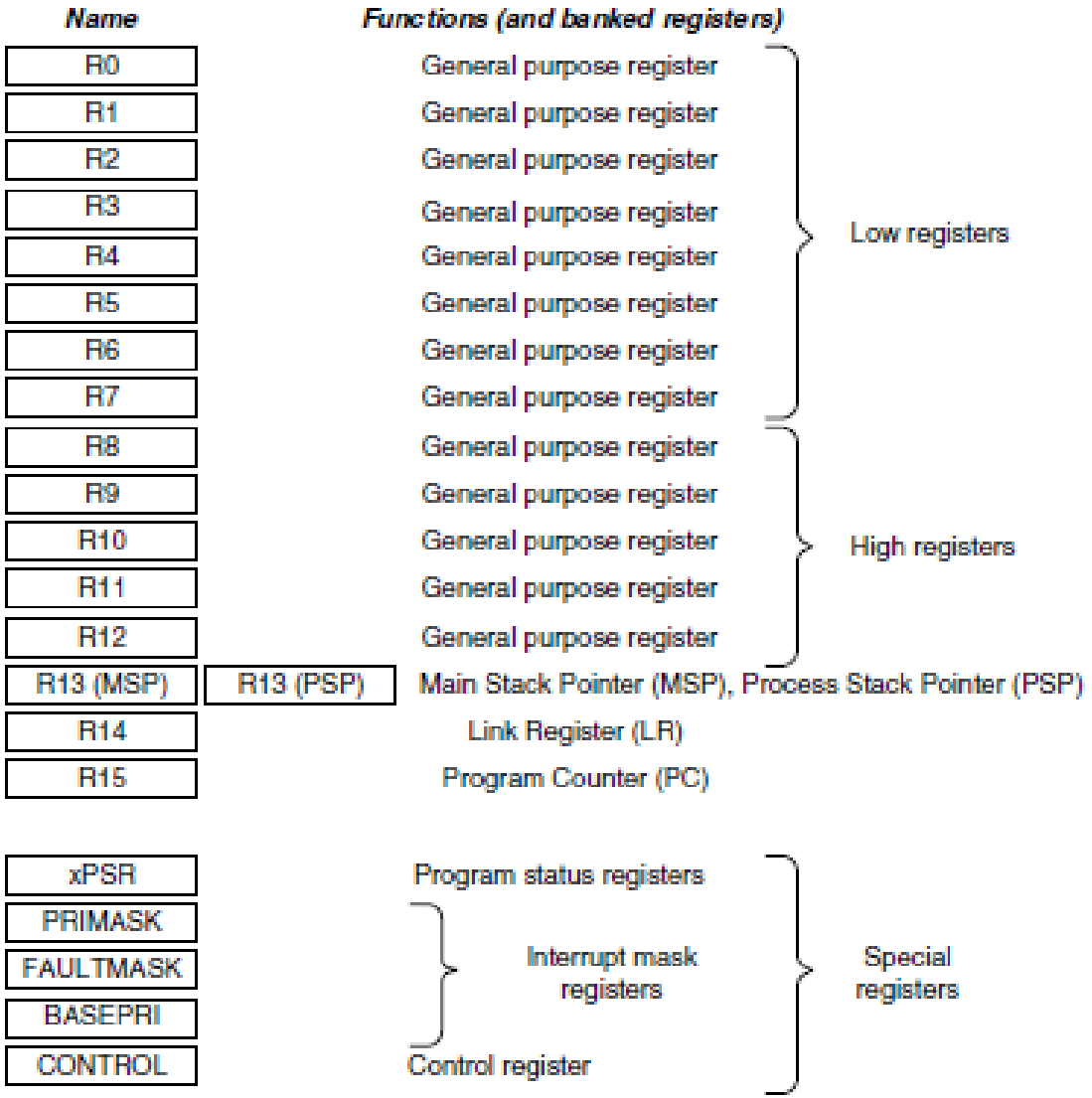
MSP: default after reset
os kernel, exception handler
Privileged
PSP: base-level application
unprivileged, user-level



(Image Courtesy of [1])

Cortex-M3 Memory Map

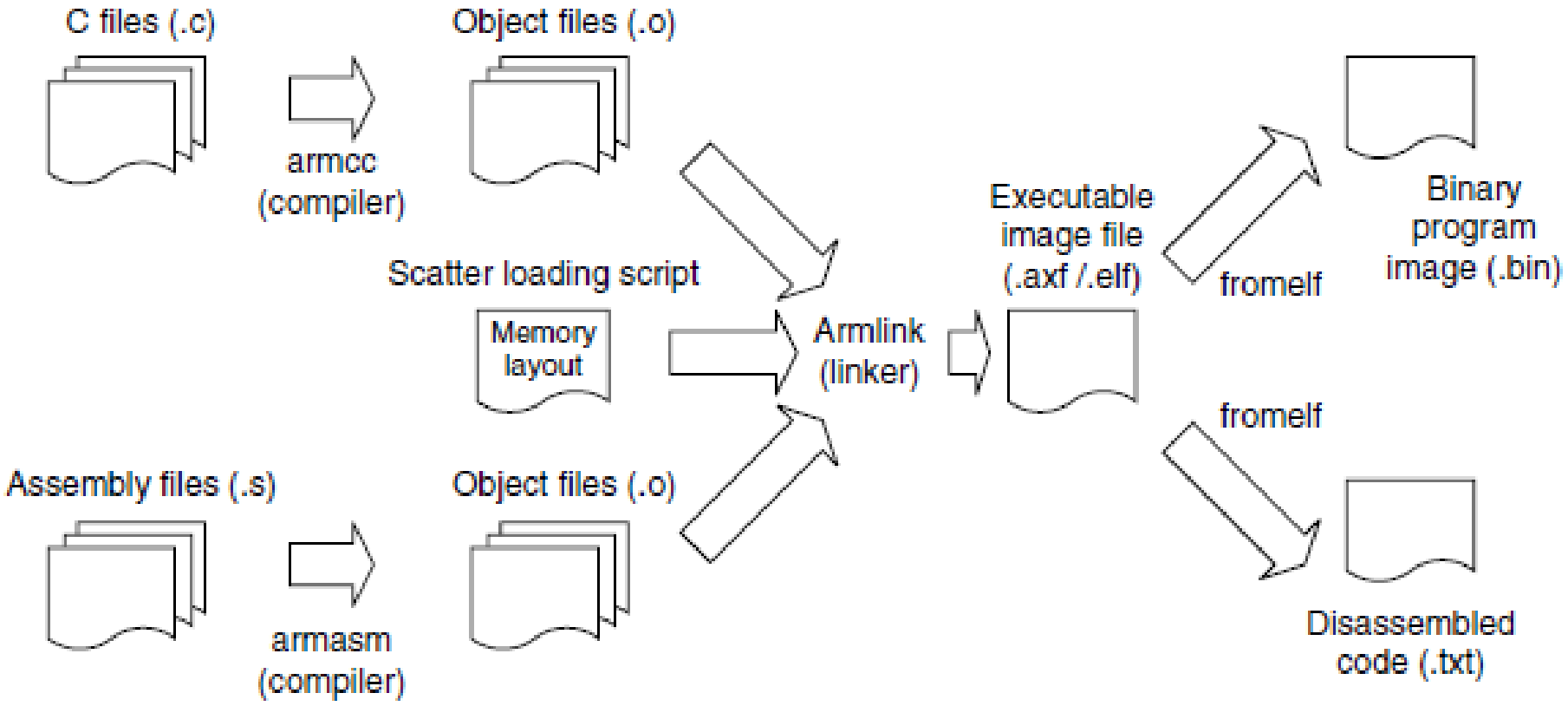
0xFFFF FFFF 0xE000 0000	0.5G	System level	Private peripherals including NVIC, MPU and debug components	★
0xA000 0000	1.0G	External device	Mainly used as external peripherals	
0x6000 0000	1.0G	External RAM	Mainly used as external memory	
0x4000 0000	0.5G	Peripherals	Mainly used as peripherals	
0x2000 0000	0.5G	SRAM	Mainly used as static RAM	★
0x0000 0000	0.5G	Code	Mainly used fro program code. Exception vector table after reset	★

(Table Courtesy of [1])

LPC1768 Memory Map

0x2008 4000		
0x2007 C000	32 KB	AHB SRAM (2 blocks of 16 KB)
0x1FFF 2000		Reserved
0x1FFF 0000	8 KB	Boot ROM
0x1000 8000		Reserved
0x1000 0000	32 KB	Local SRAM
0x0008 0000		Reserved
0x0000 0000	512 KB	On-chip flash

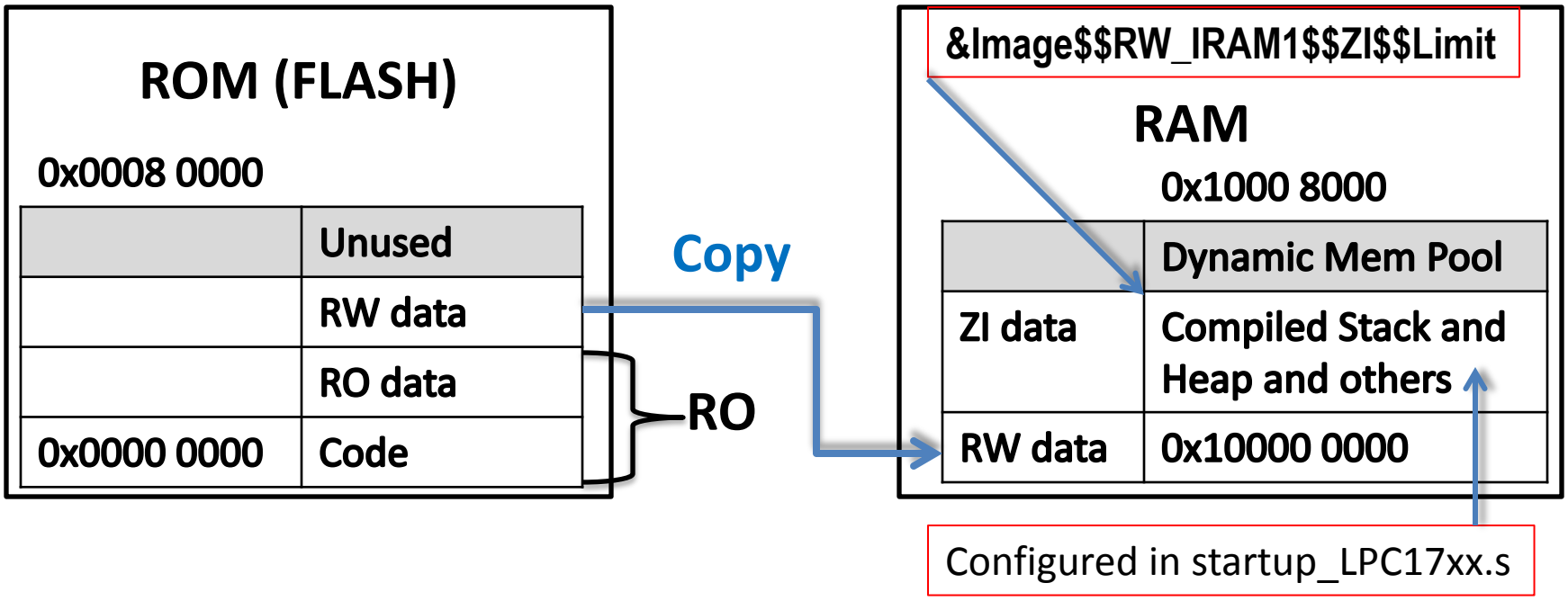
Example Flow Using ARM Development Tools



(Image Courtesy of [1])

Image memory layout

- A simple image consists of:
  - read-only (RO) section (Code + RO-data)
  - a read-write (RW) section (RW-data)
  - a zero-initialized (ZI) section (ZI-data)



End Address of the Image

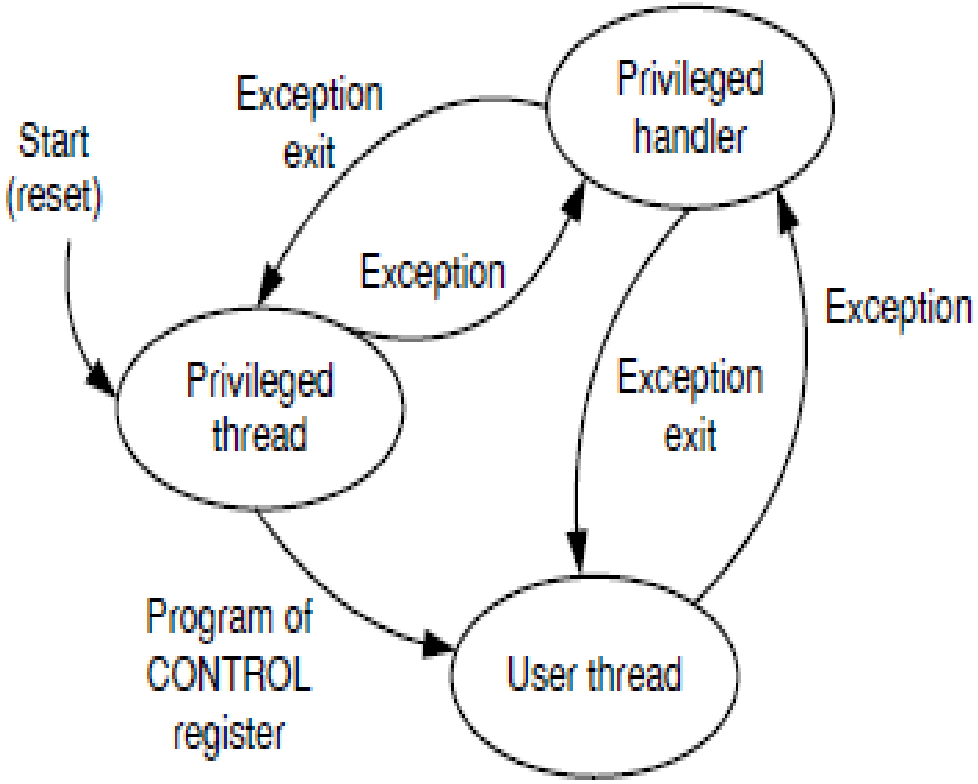
- Linker defined symbol Image$$RW_IRAM1$$ZI$$Limit

```
extern unsigned int Image$$RW_IRAM1$$ZI$$Limit;

unsigned int free_mem =
    (unsigned int) &Image$$RW_IRAM1$$ZI$$Limit;
```

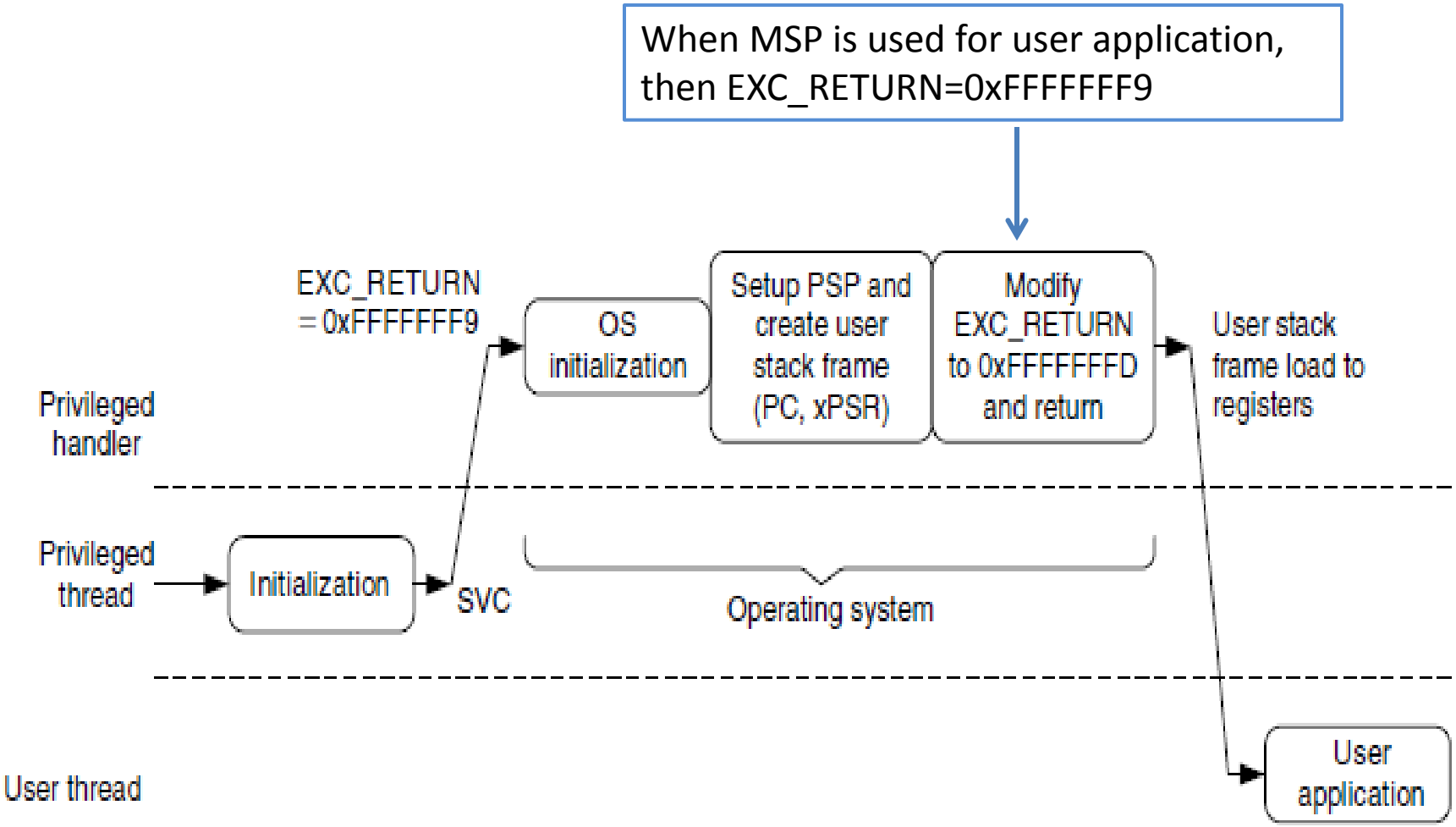
Operation Modes

- Two modes
  - Thread mode
  - Handler mode
- Two privilege levels
  - Privileged level
  - User level



(Image Courtesy of [1])

OS Initialization Mode Switch



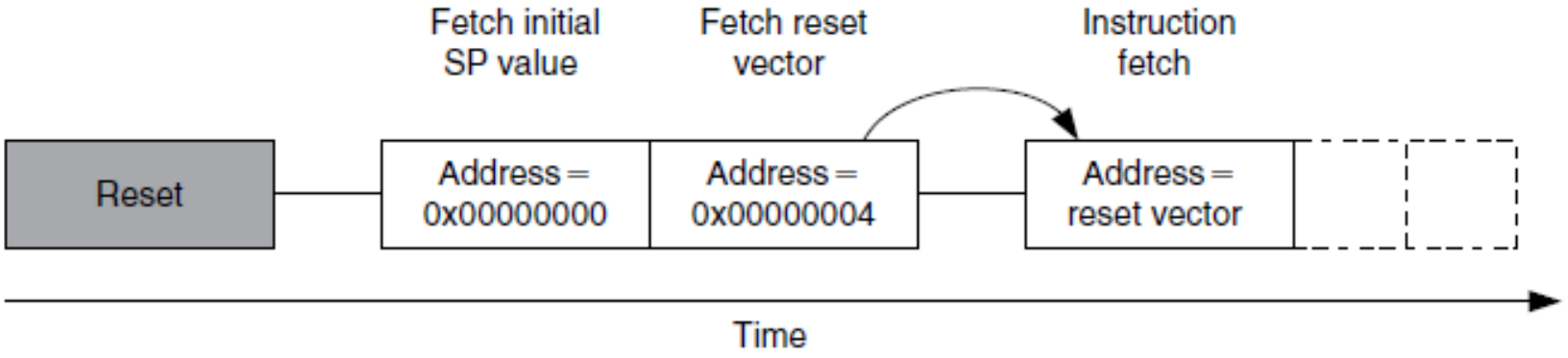
(Image Courtesy of [1])

Exceptions (1)

- NVIC (Nested Vectored Interrupt Controller)
  - System Exceptions
    - Exception Numbers 1 -15
    - SVC call exception number is 11
  - External Interrupts
    - Exception Numbers 16-50
    - Timer0-3 IRQ numbers are 17-20
    - UART0-3 IRQ numbers are 21-24
- Vector table is at 0x0 after reset.
- 32 programmable priorities
- Each vector table entry contains the exception handler's address (i.e. entry point)

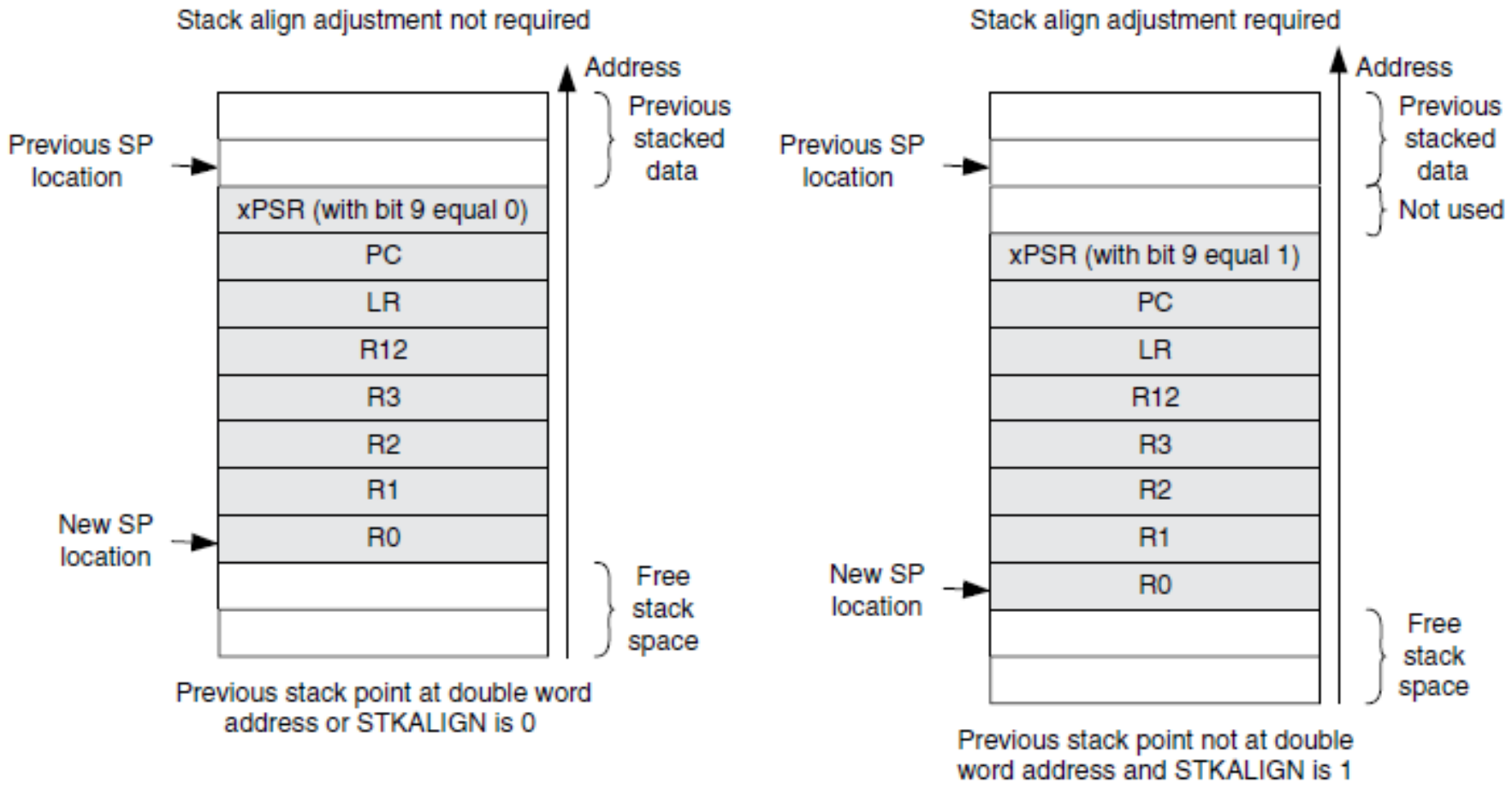
Exceptions (2)

Address	Exception Number	Value (Word Size)
0x0000 0000	-	MSP initial value
0x0000 0004	1	Reset vector (program counter initial value)
0x0000 0008	2	NMI handler starting address
0x0000 000C	3	Hard fault handler starting address
…	…	Other handler starting address



(Image Courtesy of [1])

Exception Stack Frame



(Image Courtesy of [1])

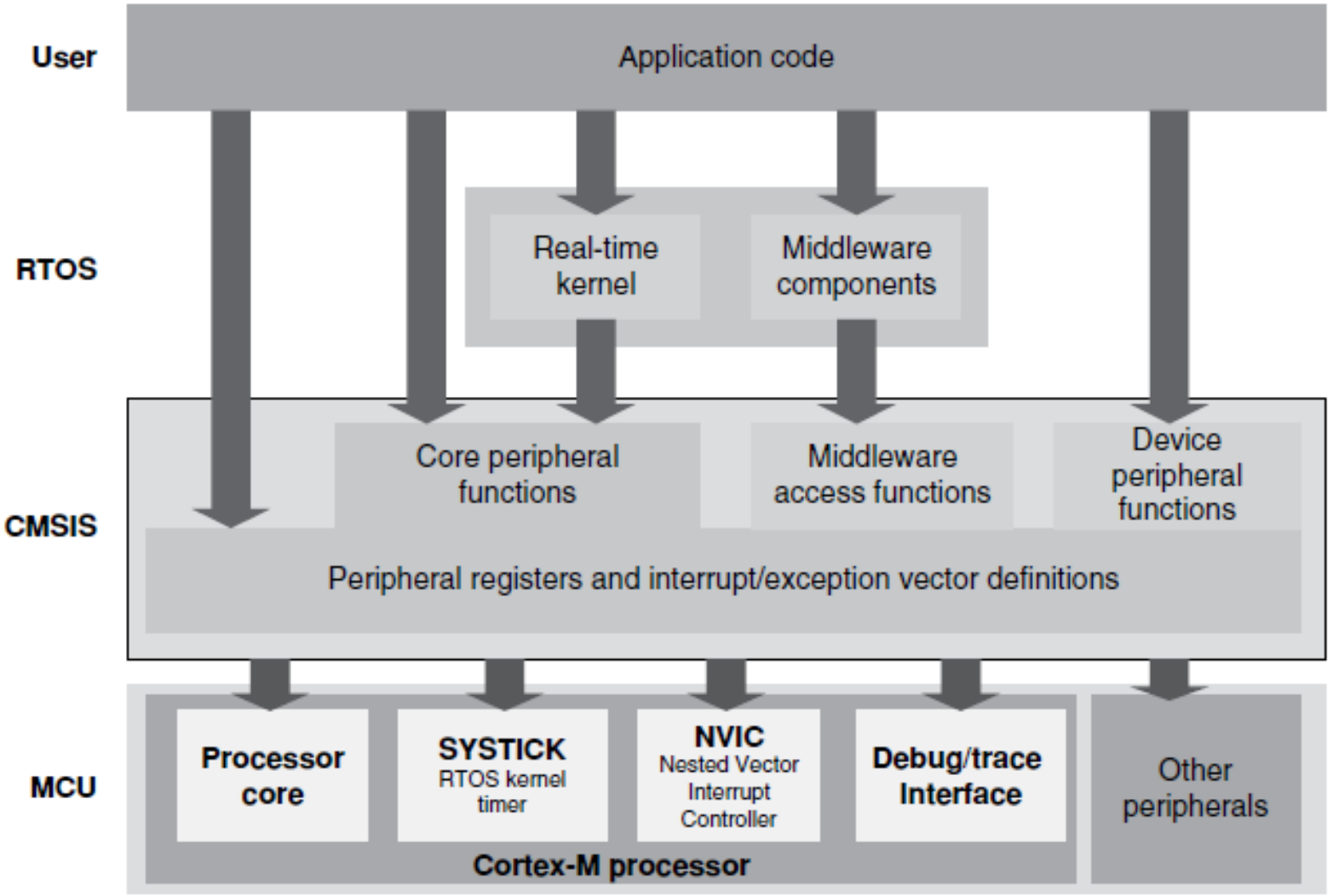
AAPCS (ARM Architecture Procedure Call Standard)

- R0-R3 , R12
  - Input parameters Px of a function. R0=P1, R1=P2, R2=P3 and R3=P4
  - R0 is used for return value of a function
- R12, SP, LR and PC
  - R12 is the Intra-Procedure-call scratch register.
- R4-R11
  - Must be preserved by the called function. C compiler generates push and pop assembly instructions to save and restore them automatically.

Cortex Microcontroller Software Interface Standard (CMSIS)

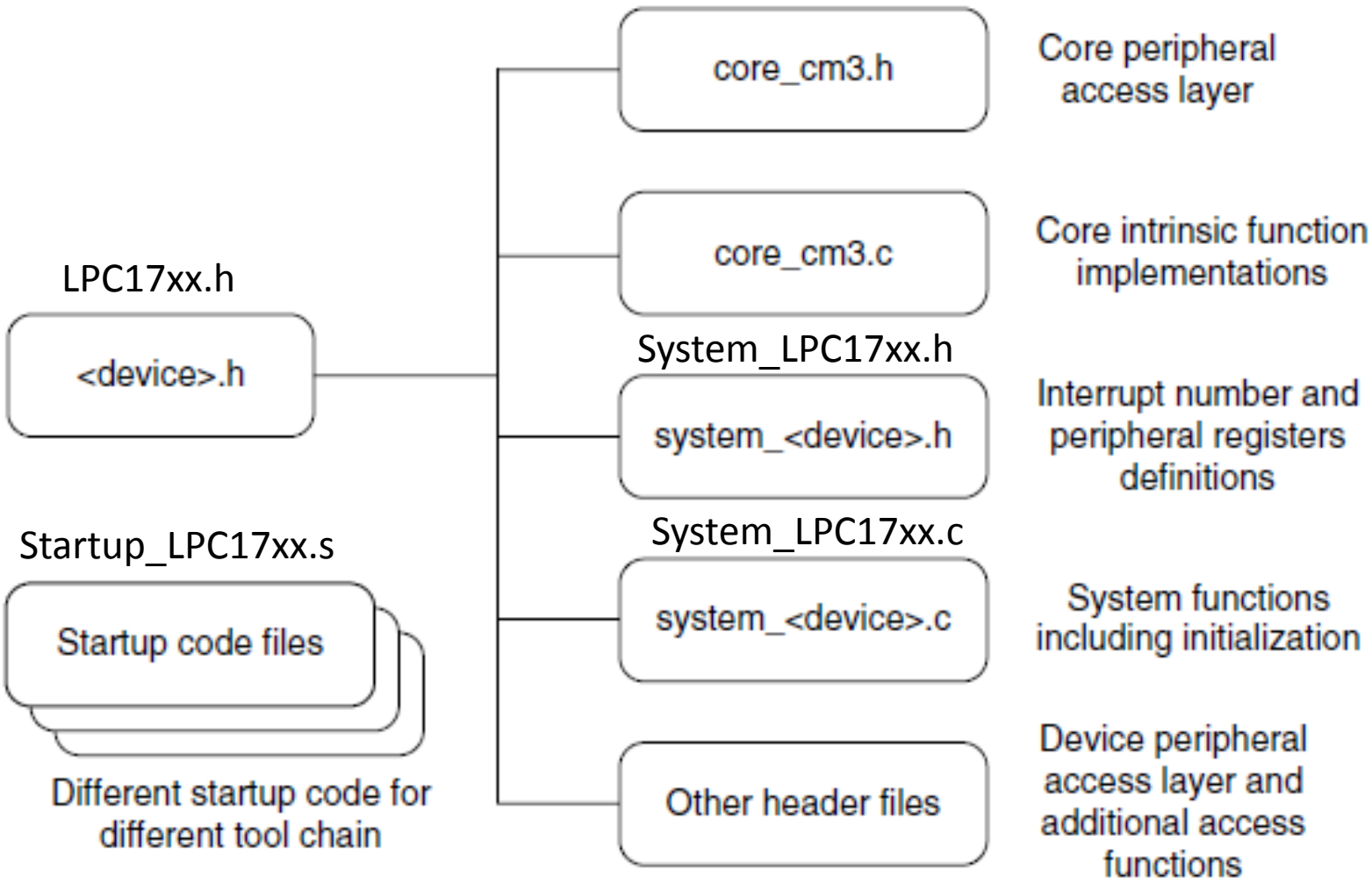
- Hardware Abstraction Layer (HAL) for Cortex-M processor registers
  - NVIC, MPU
- Standardized system exception names
  - Example: void SVC_Handler(), void UART0_IRQHandler()
- Standardized method of header file organization
- Common method for system initialization
  - SystemInit()
- Standardized intrinsic functions
  - Example: void __disable_irq(void), void __enable_irq(void)
- *Common access functions for communication*
- Standardized way for embedded software to determine system clock frequency
  - *SystemFrequency* variable is defined in device driver code

CMSIS Structure



(Image Courtesy of [1])

CMSIS Files



(Image Courtesy of [1])

External Interrupt Programming

- `IRQn` is defined in <device.h> file (i.e. LPC17xx.h)
- A set of functions
  - `void NVIC_EnableIRQ(IRQn_Type IRQn)`
  - `void NVIC_DisableIRQ(IRQn_Type IRQn)`
  - `void NVIC_SetPriority(IRQn_Type IRQn, int32_t priority)`
  - `uint32_t NVIC_GetPriority(IRQn_Type IRQn)`
  - `void NVIC_SetPendingIRQ(IRQn_Type IRQn)`
  - `void NVIC_ClearPendingIRQ(IRQn_Type IRQn)`
  - `IRQn_Type NVIC_GetPendingIRQ(IRQn_Type IRQn)`

CMSIS Example

```
#include "vendor_device.h"  // For example,
  // lm3s_cmsis.h for LuminaryMicro devices
  // LPC17xx.h for NXP devices
  // stm32f10x.h for ST devices

void main(void) {
  SystemInit();
  …
  NVIC_SetPriority(UART1_IRQn, 0x0);
  NVIC_EnableIRQ(UART1_IRQn);
  …
}
void UART1_IRQHandler {
 ...
}

void SysTick_Handler(void) {
…
}
```

Common name for system initialization code (from CMSIS v1.30, this function is called from startup code)

NVIC setup by core access functions

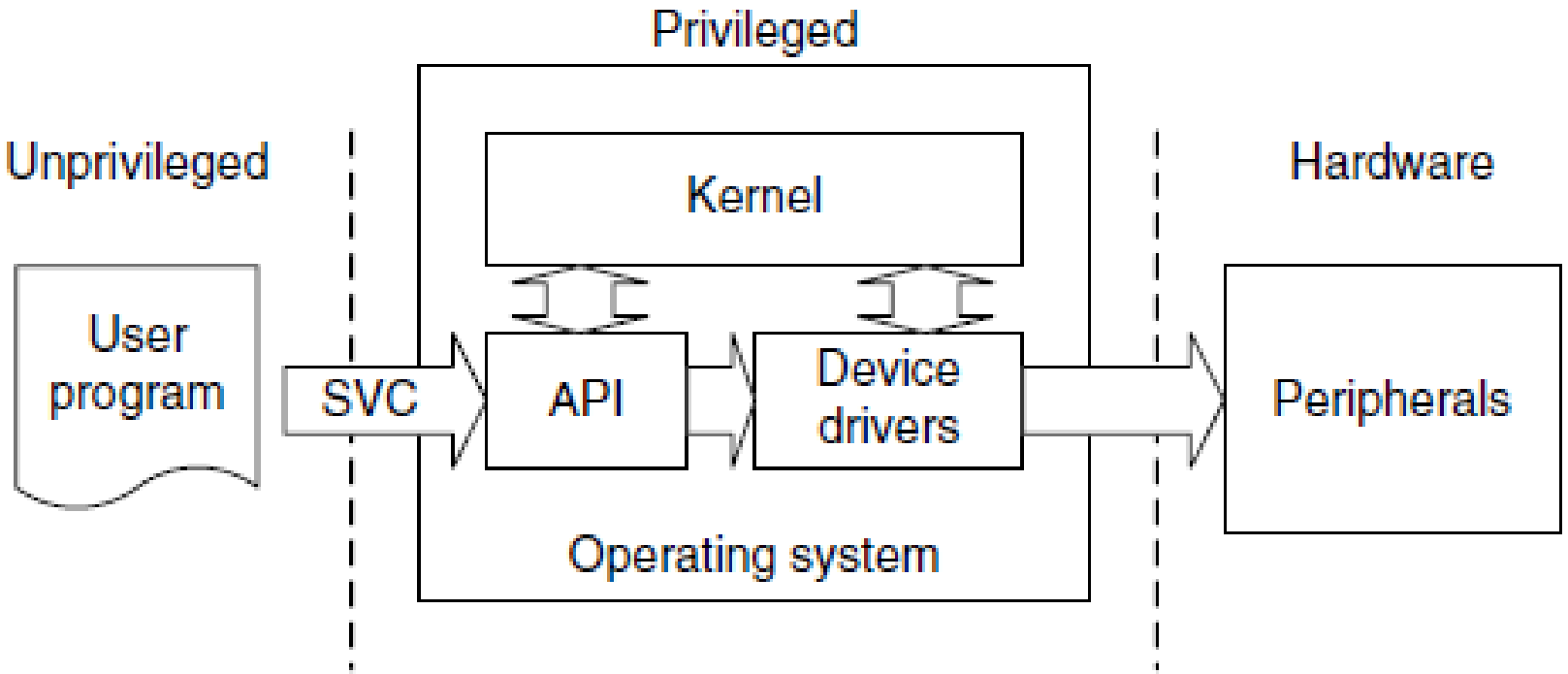
Interrupt numbers defined in system_<device>.h

Peripheral interrupt names are device specific, define in device specific startup code

System exception handler names are common to all Cortex microcontrollers

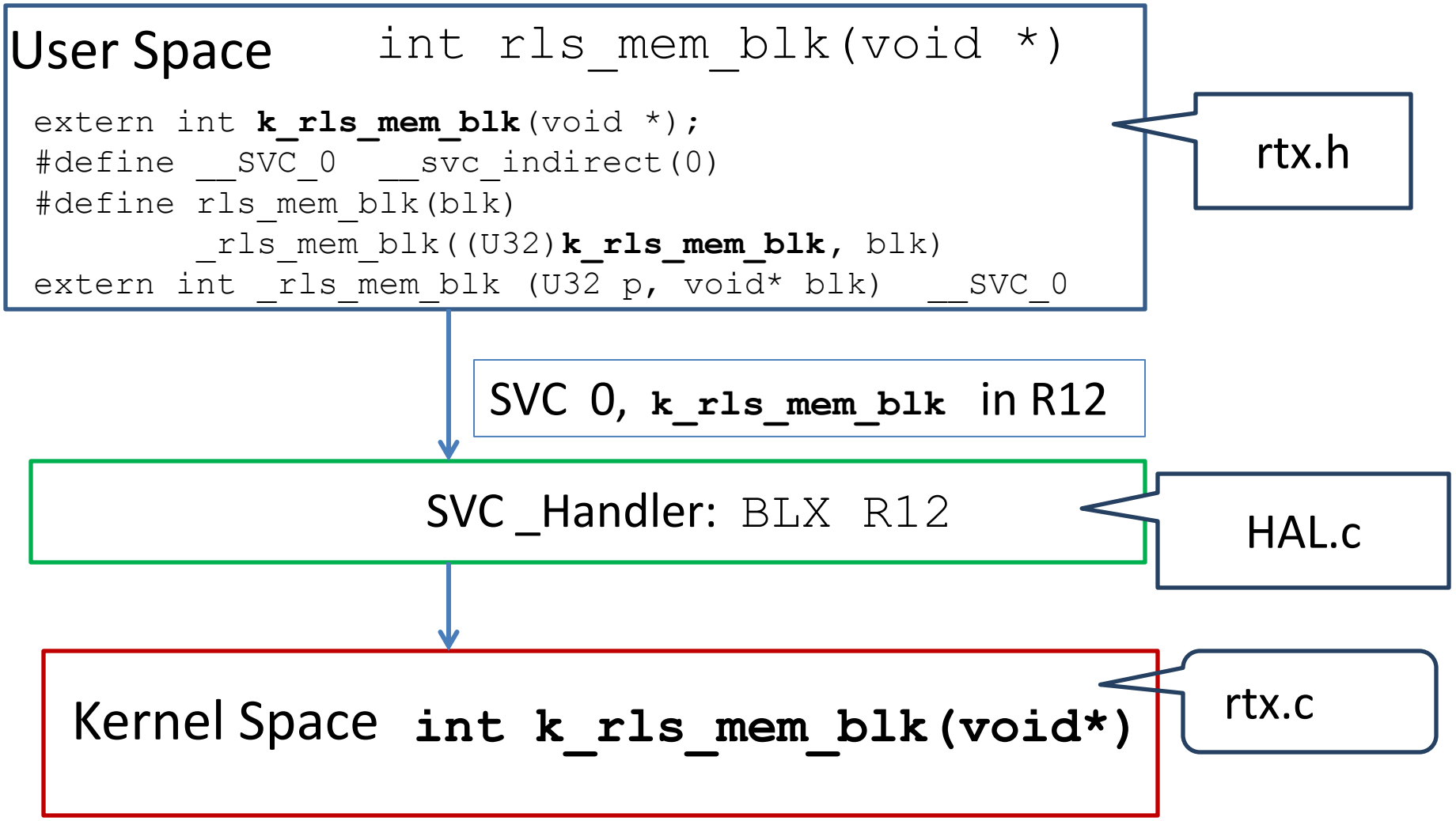
(Image Courtesy of [1])

SVC as a Gateway for OS Functions



(Image Courtesy of [1])

System calls through SVC in C



Hints

- Start with compile time memory pool and then change it later to dynamic memory pool.
- Start with just one ready queue and two simple user processes in your system to implement the context switching between the two processes.
- Once you get two processes working properly under context switching, add more ready queues to different priority levels and add user test process one by one to re-fine your context switching logic.

References

1. Yiu, Joseph, *The Definite Guide to the ARM Cortex-M3*, 2009
2. *RealView® Compilation Tools Version 4.0 Developer Guide*
3. *ARM Software Development Toolkit Version 2.50 Reference Guide*
4. *LPC17xx User's Manual*

Keil IDE Demo