***Tema lab 4***

Pb MUX 8x1

LIBRARY IEEE;

USE IEEE.std\_logic\_1164.all;

ENTITY MUX IS

PORT

(J: IN std\_logic\_vector(0 to 7);

S: IN std\_logic\_vector(0 to 2);

O: OUT std\_logic);

END MUX;

ARCHITECTURE ARCH OF MUX IS

COMPONENT MUX\_2x1 IS

PORT

(J: IN std\_logic\_vector(0 to 1);

S: IN std\_logic;

Y: OUT std\_logic);

END COMPONENT;

COMPONENT MUX\_4x1 IS

PORT

(I: IN std\_logic\_vector(0 to 3);

S: IN std\_logic\_vector(0 to 1);

Y: OUT std\_logic);

END COMPONENT;

SIGNAL L: std\_logic\_vector(0 to 1);

BEGIN

MUX4x1\_1: MUX\_4x1 PORT MAP(J(0 to 3), S(0 to 1), L(0));

MUX4x1\_2: MUX\_4x1 PORT MAP(J(4 to 7), S(0 to 1), L(1));

MUX2x1: MUX\_2x1 PORT MAP(L(0 to 1), S(2), O);

END ARCH;

LIBRARY IEEE;

USE IEEE.std\_logic\_1164.all;

ENTITY MUX\_4x1 IS

PORT

(I: IN std\_logic\_vector(0 to 3);

S: IN std\_logic\_vector(0 to 1);

Y: OUT std\_logic);

END MUX\_4x1;

ARCHITECTURE ARCH\_4 OF MUX\_4x1 IS

BEGIN

Y<=(NOT S(0) AND NOT S(1) AND I(0)) OR (NOT S(0) AND S(1) AND I(1)) OR (S(0) AND NOT S(1) AND I(2)) OR (S(0) AND S(1) AND I(3));

END ARCH\_4;

LIBRARY IEEE;

USE IEEE.std\_logic\_1164.all;

ENTITY MUX\_2x1 IS

PORT

(J: IN std\_logic\_vector(0 to 1);

S: IN std\_logic;

Y: OUT std\_logic);

END MUX\_2x1;

ARCHITECTURE ARCH\_2 OF MUX\_2x1 IS

BEGIN

Y<=(NOT S and J(0)) OR (S AND J(1));

END ARCH\_2;

