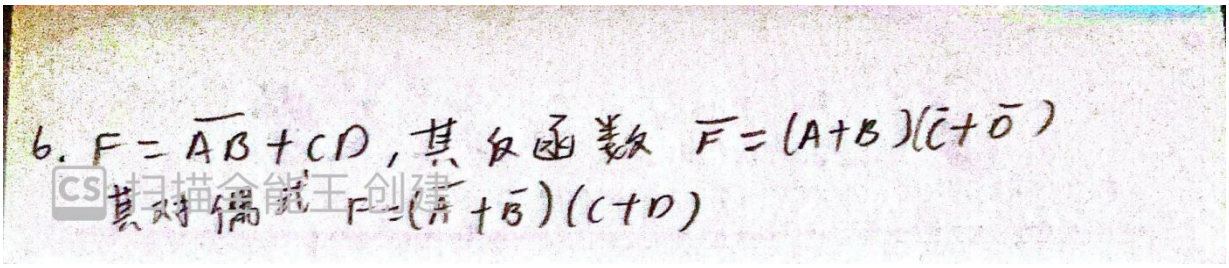
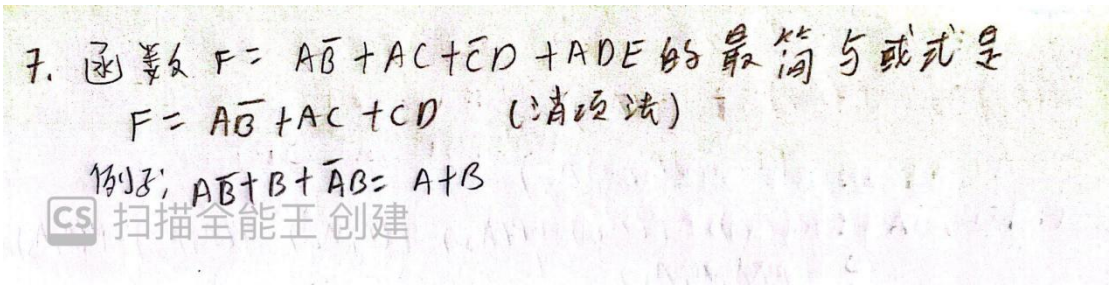
计算机组成作业 1
71066001-陈伟杰

第一大题
1.导通，截止
2.关态，低电平，开态，高电平
3.3.0v，0.35v
4.ECL-TTL-CMOS（从快到慢），CMOS-TTL-ECL（抗干扰能力强弱），CMOS-TTL-ECL（静态功耗低和高）
5.0 和 1
6.



7.



8.存储电路，反馈电路，输入信号决定
9.编码
10.译码器，n 个输入，2n 输出
11.1110111111

第二题

1.第 4 个，大于 0.5v 小于 0.5v

2.第 3 个

3.第二个 答案是或逻辑

4.第 4 个

5.第 1 个 答案是 1

6.第 2 个 答案是 011

7.第 1 个 答案是互为反函数

8.第 3 个 答案是构成电路的逻辑元件存在传输延迟

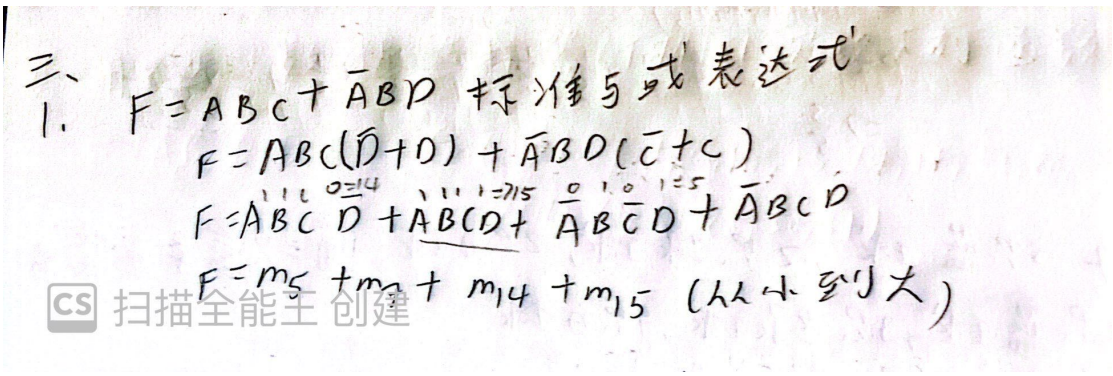
9.第 3 个 答案是数据选择器

10.第 2 个 答案是半加

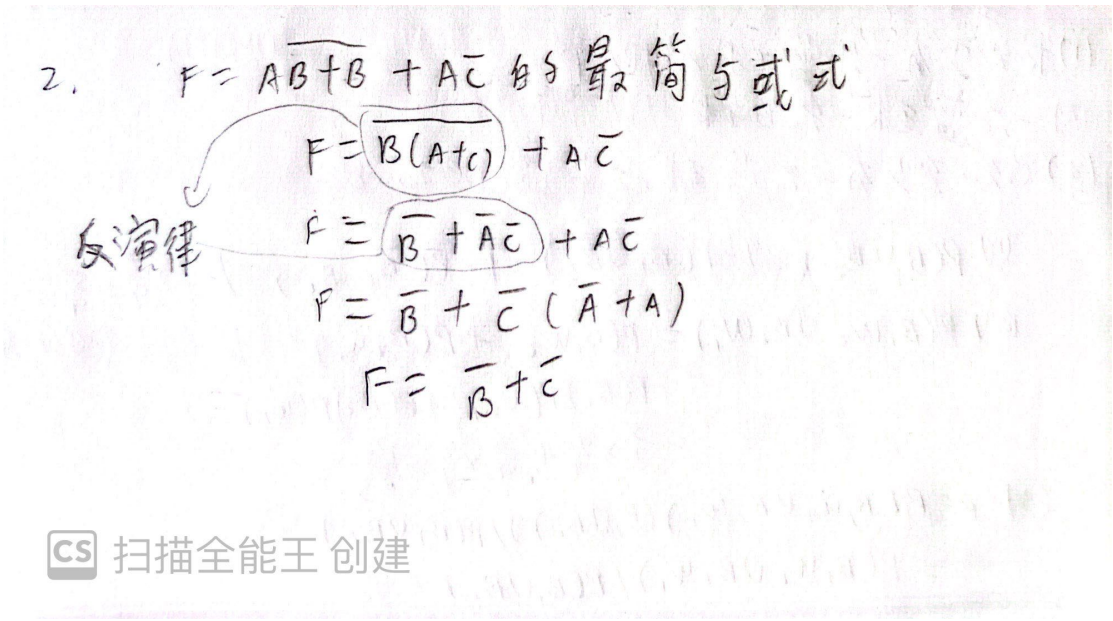
11.第 4 个 数值比较器

第三题

1.



2.



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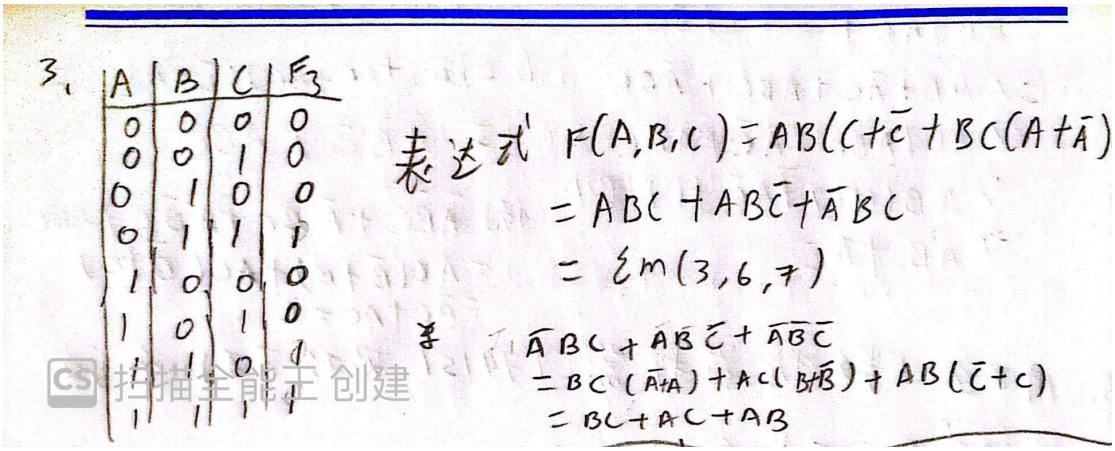
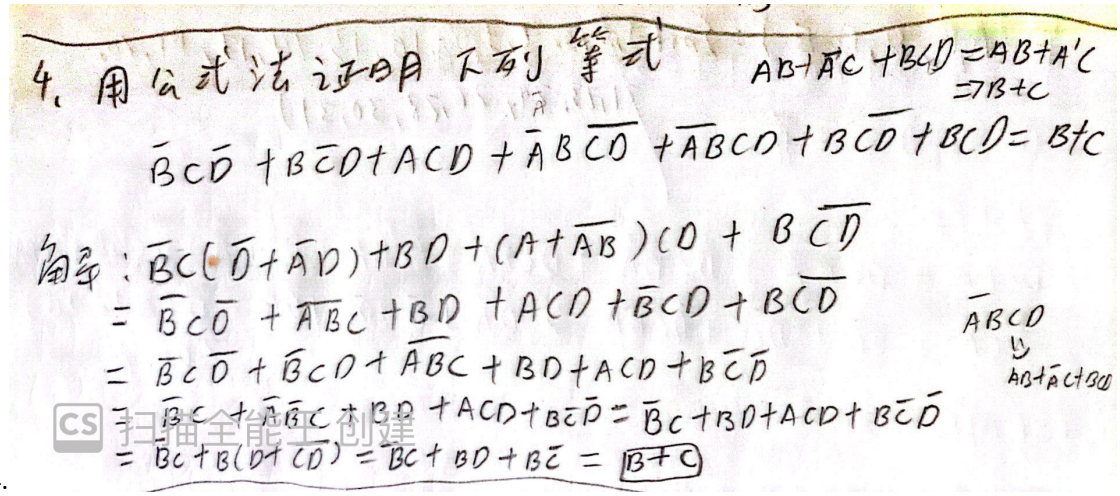



```
module top_module(
    input A,B,C;
    output out
);
    assign out =B&C+A&C+A&B;
endmodule
```

4.



5.

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5. 用8选1数据选择器CT74151实现下列函数

$F(A,B,C,D,E)=\sum m(1,2,3,4,7,8,10,13,14,17,19,20,21,23,24,26,28,30,31)$

A	B	C	D	E	F
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	0
1	1	1	1	1	1

令 $A_2A_1A_0=ABC$

$D_0=D\bar{E}$

$D_1=D\oplus E$

$D_2=\bar{E}$

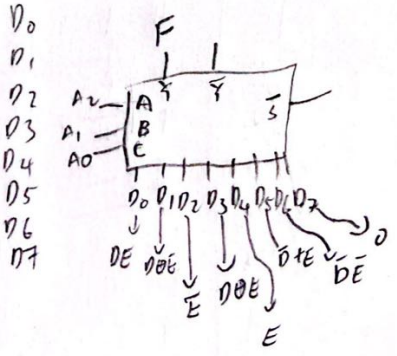
$D_3=D\oplus E$

$D_4=E$

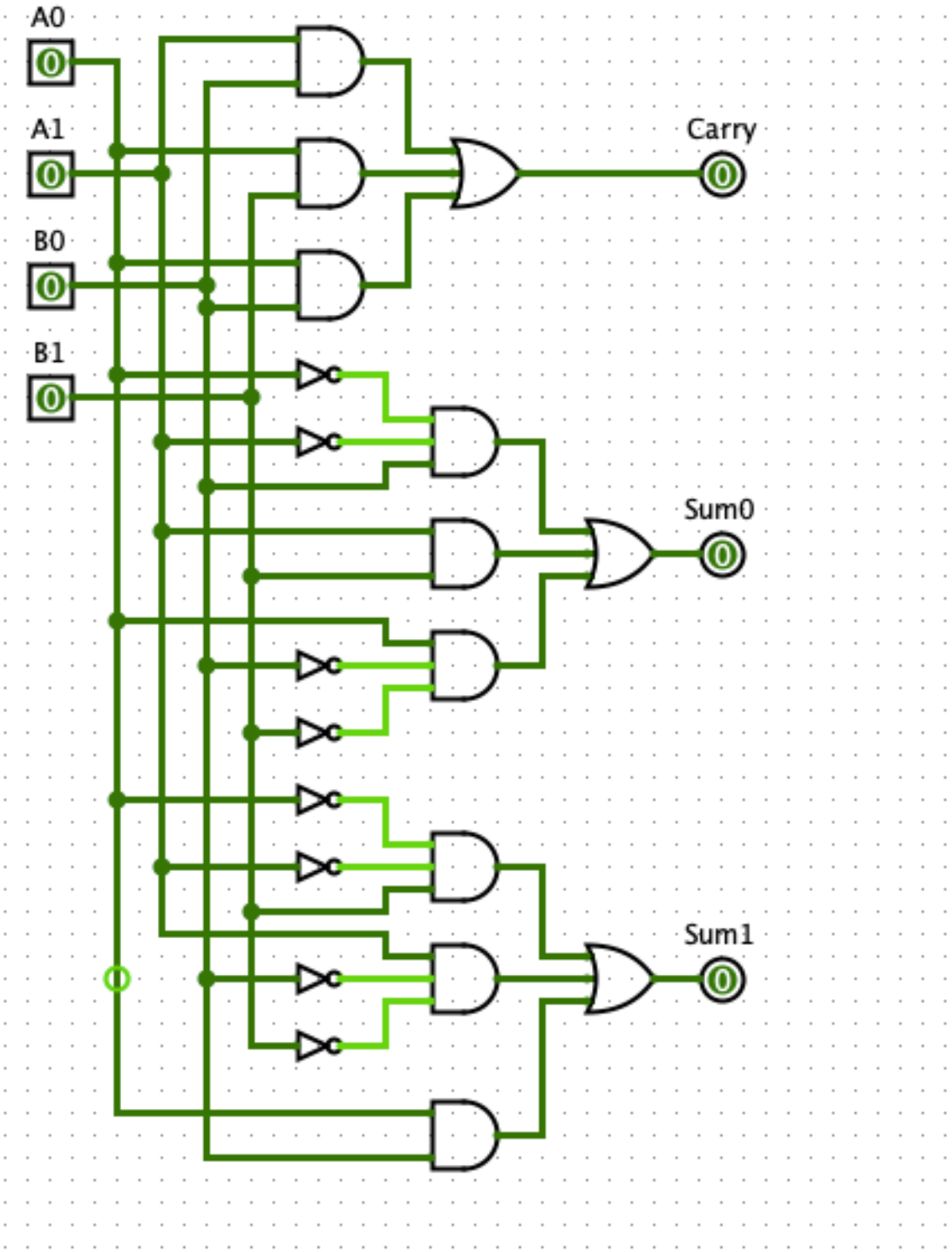
$D_5=\bar{D}+E$

$D_6=\bar{D}\bar{E}$

$D_7=0$



6.(1)



(下面这张图是 2)

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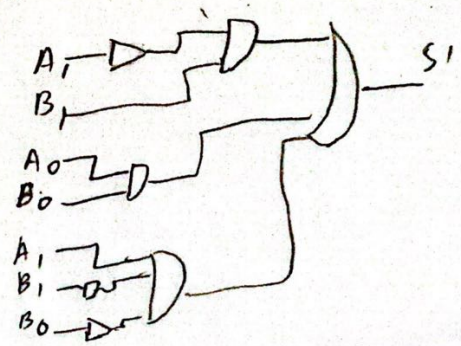
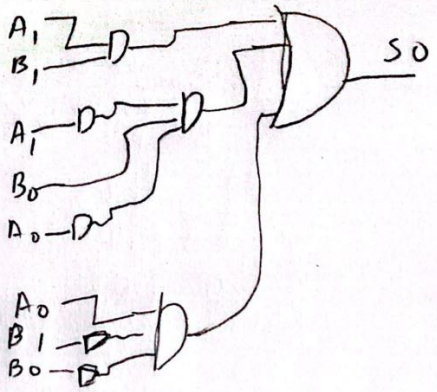
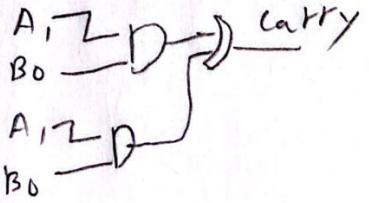
6. 三进制全加器真值表

A	B	C	sum	carry
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	1	0	1	0
0	1	1	2	0
0	1	2	0	1
0	2	0	2	0
0	2	1	0	1
0	2	2	1	1
1	0	0	1	0
1	0	1	2	0
1	0	2	0	1
1	1	0	2	0
1	1	1	0	1
1	1	2	1	1
1	2	0	0	1
1	2	1	1	1
1	2	2	2	1
2	0	0	2	0
2	0	1	0	1
2	0	2	1	1
2	1	0	0	1
2	1	1	1	1
2	1	2	2	1
2	2	0	1	1
2	2	1	2	1
2	2	2	0	2





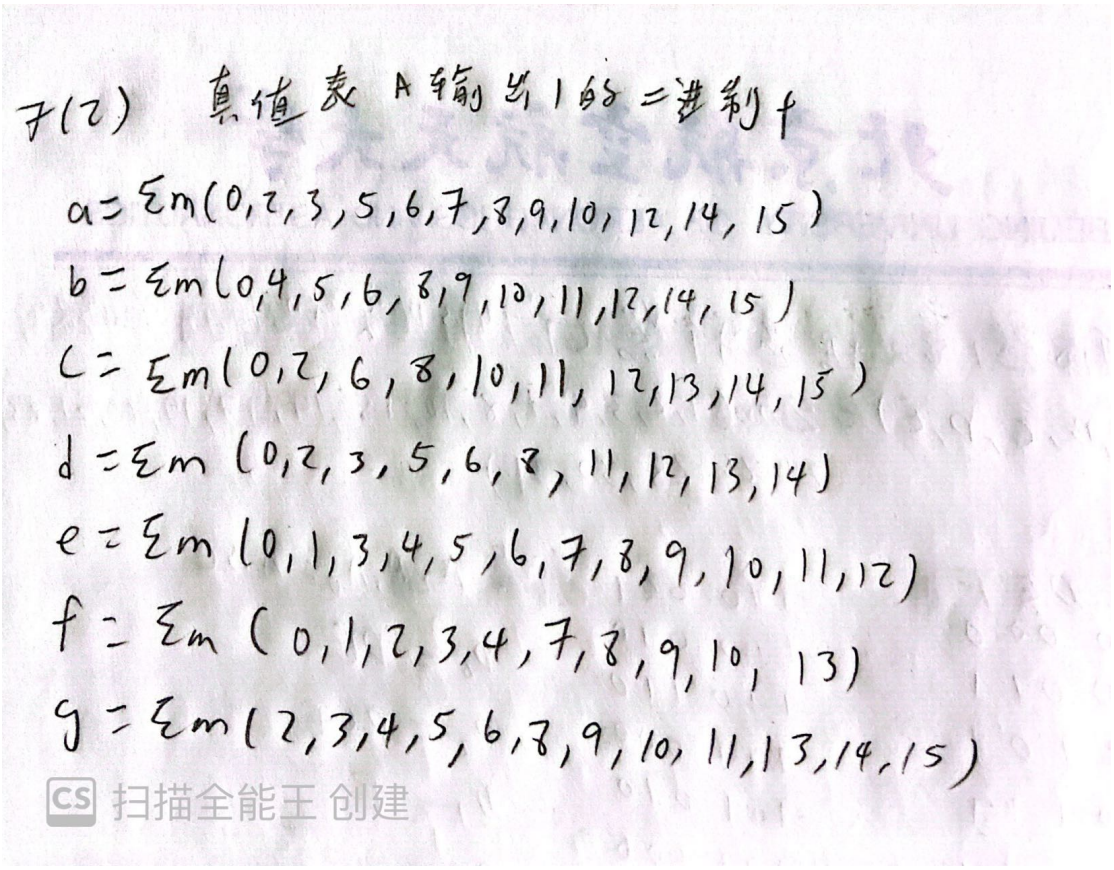


7.

7. 请给出7段数码管控制电路的输入输出信号真值表

11)

输入				输出							字形
D	C	B	A	Fa	Fb	Fc	Fd	Fe	Ff	Fg	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	0	0	0	1	1	0	1
0	0	1	0	1	0	1	1	0	1	1	2
0	0	1	1	1	0	0	1	1	1	1	3
0	1	0	0	0	1	0	0	1	1	1	4
0	1	0	1	1	1	0	1	1	0	1	5
0	1	1	0	1	1	1	1	1	0	1	6
0	1	1	1	1	0	0	0	1	1	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	0	0	1	1	1	9
1	0	1	0	1	1	1	0	1	1	1	A
1	0	1	1	0	1	1	1	1	0	1	B
1	1	0	0	1	1	1	1	0	0	0	C
1	1	0	1	0	0	1	1	1	1	1	D
1	1	1	0	1	1	1	1	0	0	1	E
1	1	1	1	1	1	1	0	0	0	1	F




```
module seg_dec(num,a_g);//71066001-陈伟杰的第七题 (3)
input[3:0] num;
output[6:0] a_g;//a_g 代表着abcdefg
reg[6:0] a_g;
always@(num)
begin
    case(num)
    4'd0:begin a_g<=7'b1111110;//这些都是我根据真值表所输出的数 比如这个是0
    4'd1:begin a_g<=7'b0000110;//1
    4'd2:begin a_g<=7'b1011011;//2
    4'd3:begin a_g<=7'b1001111;//3
    4'd4:begin a_g<=7'b0100111;//4
    4'd5:begin a_g<=7'b1101101;//5
    4'd6:begin a_g<=7'b1111101;//6
    4'd7:begin a_g<=7'b1000110;//7
    4'd8:begin a_g<=7'b1111111;//8
    4'd9:begin a_g<=7'b1100111;//9
    4'da:begin a_g<=7'b1110111;//A
    4'db:begin a_g<=7'b0111101;//B
    4'dc:begin a_g<=7'b1111000;//C
    4'dd:begin a_g<=7'b0011111;//D
    4'de:begin a_g<=7'b1111001;//E
    4'df:begin a_g<=7'b1110001;//F
    endcase
end
endmodule
```