INTERFACE PCBA HIGH LEVEL DESIGN SPECIFICATION

PM1 Pachymeter Automated System Level Test Platform

Prepared for:

Occuity Ltd

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1 TABLE OF CONTENTS

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CHANGE HISTORY

Version	Author	Date of Change	Description
0.1	James Bridson	29-Oct-2021	Initial version.
0.2	James Bridson	10-Nov-2021	Revision for Occuity and LeoTel joint review.
0.3	James Bridson	18-Nov-2021	Updated following first review.
0.4	James Bridson	22-Dec-2021	Incorporated comments from final LeoTel & Occuity review.
0.5	James Bridson	07-Mar-2022	Updated following PCBA B1 integration.

DOCUMENT REFERENCES

Ref.	Document Id	Title	Author	Issue	Date
1	P1-SOF-SIS-01	Software Interface Specification	Occuity	2	21-Jun-2021
2	P1-SOF-ASV-01	Automated System- and Subsystem-Level Software Verification – Proposal	Occuity	Draft 1	18-Jun-2021
3	LSSL/20210723/01	Development Proposal	LSSL	1.1	23-Sep-2021

APPLICABLE STANDARDS

Term	Description
ISO 13485	Medical devices – quality management systems – Requirements for regulatory purposes
IEC 62304	Medical device software – software lifecycle processes
ISO 14971	Medical devices – Application of risk management to medical devices
ISO/IEC 12207	Systems and software engineering – Software life cycle processes

GLOSSARY & ACRONYMS

Term	Description
AI	Analogue Input
AO	Analogue Output
APFI	Analogue Programmable Function Interface
CC	Constant Current
COTS	Commercial Off-The-Shelf
DI	Digital Input
DIO	Digital Input / Output
DNC	Do Not Connect
DNF	Do Not Fit
DO	Digital Output
DUT	Device Under Test
FFC	Flexible Flat Cable
FPC	Flexible Printed Circuit
GPIO	General Purpose Input / Output
IEC	International Electrotechnical Commission
ISO	International Organization for Standardization
LDA PCB	Laser Driver and Amplifier Printed Circuit Board
LSC PESS	Linear Scanner Controller Programmable Electronic Sub-System
OTS	Off-The-Shelf
Pachymeter	A scientific instrument used to measure the thickness of the cornea using laser, light waves or ultrasound.
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PDA PESS	Pachymeter Data Acquisition Programmable Electronic Sub-System
PE PESS	Pachymeter Environmental Programmable Electronic Sub-System
PFI	Programmable Function Interface
PI PESS	Pachymeter Interface Programmable Electronic Sub-System
TBC	To Be Confirmed
UUT	Unit Under Test
WP*n*	Work Package *n*

2 INTRODUCTION

This specification documents the high-level design for the Occuity PM1 Pachymeter Automated System Level Test Platform interface printed circuit board assembly (PCBA). The PCBA will act as an interface between the PM1 Pachymeter under test and the test platform providing connectivity of the input/output test signals and any associated signal conditioning where required. The PCBA will also provide some general purpose digital input/output, for future control/monitoring needs, and pass-thru of other useful signals e.g. to the LCD.

2.1 PURPOSE

This document is primarily intended to be used:

- As a means of communication between Occuity Ltd and LeoTel Software Systems Limited (LSSL) to clarify the high-level design of the PM1 Pachymeter Automated System Level Test Platform Interface PCBA, and to ensure that both parties have the same understanding of the design; and
- By hardware and software engineers during the PM1 Pachymeter Automated System Level Test Platform project, in particular when constructing the test platform.

2.2 SCOPE

This document covers the hardware signals, interfaces, interconnections and any signal conditioning required on the PM1 Pachymeter Automated System Level Test Platform Interface PCBA in order to meet the requirements documented in reference [3].

2.3 DOCUMENT OVERVIEW

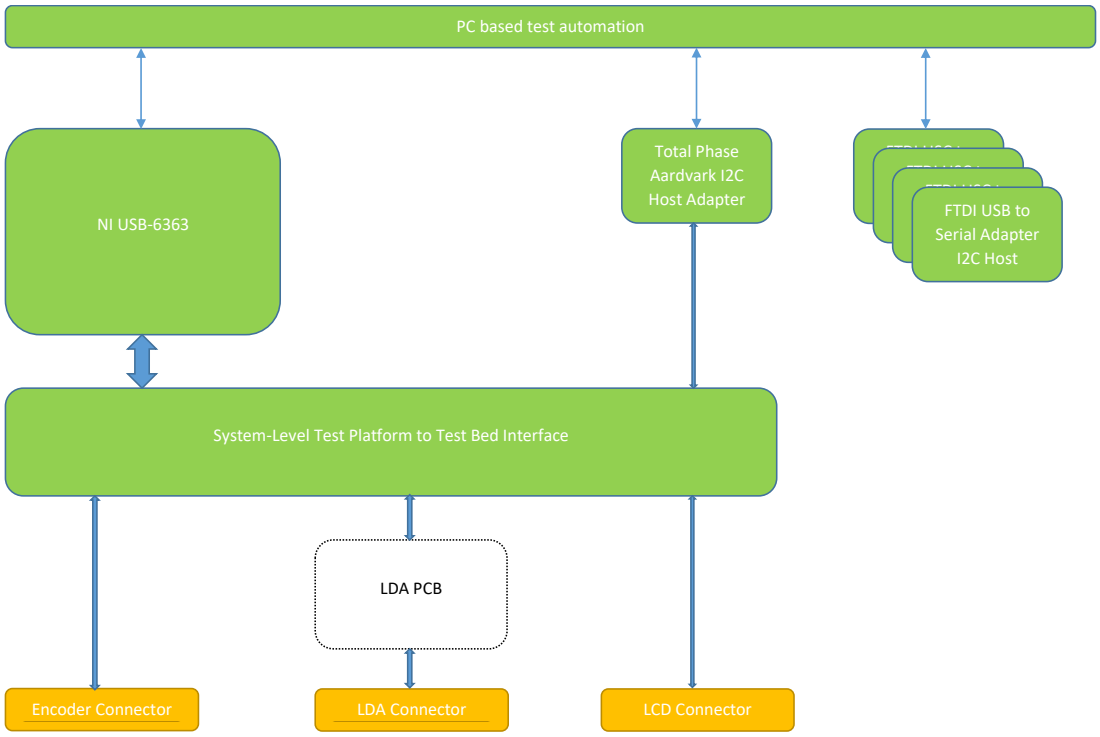
The remainder of this document is organised into sections as follows:

Section 3 documents the Interface PCBA High Level Design

3 INTERFACE PCBA SOLUTION

3.1 OVERVIEW

The logical components in the PM1 Pachymeter Automated System Level Test Platform are summarised in the following diagram:

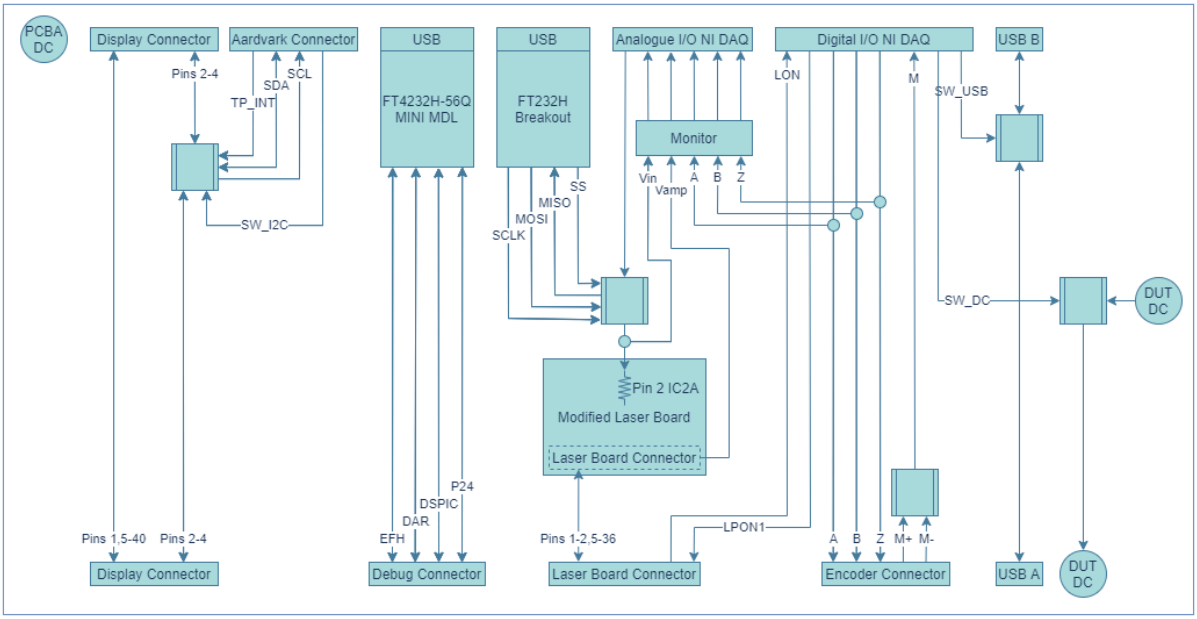


This document covers the hardware signals, interfaces, interconnections and any signal conditioning required on the block labelled 'System-Level Test Platform to Test Bed Interface' in order to provide a convenient interface between the PM1 Pachymeter Automated System Level Test Platform and the PM1 Pachymeter under test.

3.2 HIGH LEVEL DESIGN

3.2.1 OVERVIEW

The following block diagram illustrates the connectivity that will be provided by the Interface PCBA between the PM1 Pachymeter Automated System Level Test Platform and the PM1 Pachymeter device under test (DUT).



3.2.2 CONNECTOR PINOUTS

3.2.2.1 PM1 PACHYMETER TO INTERFACE PCBA

3.2.2.1.1 Display Connector

The PM1 Pachymeter main board display connector (X1) will connect to the interface PCBA via an FFC terminated at a MOLEX 54104-4033 FFC-to-board 0.50mm 40 circuit connector.

The FFC carries the LCD display and touch panel signals between the PM1 Pachymeter main board and the interface PCBA.

Pin	Signal	Level	Direction	Notes
X1-1	~TP_RESET	0V/+3V3	Output	TP Reset (active low)
X1-2	TP_INT	0V/+3V3	Input	TP Interrupt (active high)
X1-3	SDA3	0V/+3V3	Open Drain	I2C Serial Data
X1-4	SCL3	0V/+3V3	Open Drain	I2C Serial Clock
X1-5	+3V3	+3V3	Power	Power
X1-6	GND	GND	Ground	Signal Ground
X1-7	N/C			N/C
X1-8	N/C			N/C
X1-9 to X1-19	GD3 to GD15	0V/+3V3	Output	LCD Data
X1-20	GND	GND	Ground	Signal Ground
X1-21 to X1-25	GD19 to GD23	0V/+3V3	Output	LCD Data
X1-26	GND	GND	Ground	Signal Ground

Pin	Signal	Level	Direction	Notes
X1-27 to X1-36	DISPLAY_*	0V/+3V3	Output	LCD Control
X1-37	+3V3	+3V3	Power	LCD Power
X1-38	GND	GND	Ground	Signal Ground
X1-39	LCD_BACKLIGHT	20mA (CC)	Power	LCD Backlight Anode
X1-40	GND	GND	Ground	LCD Backlight Cathode

The interface PCBA will support a pass-through facility to a display assembly via an FFC terminated at a MOLEX 54104-4033 FFC-to-board 0.50mm 40 circuit connector.

The FFC carries the pass-through LCD display and touch panel signals between the PM1 Pachymeter main board and the interface PCBA.

Pin	Signal	Level	Direction	Pass-Through	Notes
1	~RST	0V/+3V3	Output	Direct	TP Reset
2	IRQ	0V/+3V3	Input	Switched	TP Interrupt
3	SDA	0V/+3V3	Open Drain	Switched	I2C Serial Data
4	SCL	0V/+3V3	Open Drain	Switched	I2C Serial Clock
5	+3V3	+3V3	Power	Direct	Power
6	GND	GND	Ground	Direct	Signal Ground
7	N/C			Direct	N/C
8	N/C			Direct	N/C
9 to 19	GD3 to GD15	0V/+3V3	Output	Direct	LCD Data
20	GND	GND	Ground	Direct	Signal Ground
21 to 25	GD19 to GD23	0V/+3V3	Output	Direct	LCD Data
26	GND	GND	Ground	Direct	Signal Ground
27 to 36	DISPLAY_*	0V/+3V3	Output	Direct	LCD Control
37	+3V3	+3V3	Power	Direct	LCD Power
38	GND	GND	Ground	Direct	Signal Ground
39	LCD_BACKLIGHT	20mA (CC)	Power	Direct	LCD Backlight Anode
40	GND	GND	Ground	Direct	LCD Backlight Cathode

3.2.2.1.2 Debug Connector

The PM1 Pachymeter main board debug connector (X6) will connect to the interface PCBA via a PicoBlade Male-to-PicoBlade Male Off-the-Shelf (OTS) Cable Assembly terminated at a MOLEX 53398-0971 PicoBlade PCB Header 1.25mm 9 circuit connector.

The cable assembly carries the microprocessor serial debug signals between the PM1 Pachymeter main board and the interface PCBA.

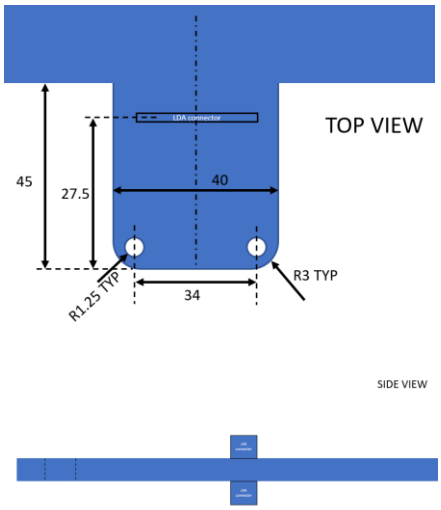
Pin	Signal	Level	Direction	Notes
X6-1	GND	GND	Ground	Signal Ground
X6-2	EFH_DBG_RX	0V/+3V3	Input	Serial Receive
X6-3	EFH_DBG_TX	0V/+3V3	Output	Serial Transmit
X6-4	DAR_DBG_RX	0V/+3V3	Input	Serial Receive
X6-5	DAR_DBG_TX	0V/+3V3	Output	Serial Transmit
X6-6	DSPIC_DBG_RX	0V/+3V3	Input	Serial Receive
X6-7	DSPIC_DBG_TX	0V/+3V3	Output	Serial Transmit
X6-8	P24_DBG_RX	0V/+3V3	Input	Serial Receive
X6-9	P24_DBG_TX	0V/+3V3	Output	Serial Transmit

3.2.2.1.3 Laser Board Connector

The PM1 Pachymeter main board laser connector (J1) will connect to the Interface PCBA via one of two SAMTEC CLM-118-02-F-D low profile dual wipe 1.00mm board-to-board connectors on either side of the Interface PCBA.

Pin	Signal	Level	Direction	Pass-Through	Notes
J1-1 to J1-2	-	-	-	Direct	
J1-3	LON	0V/+3V3	Output	Direct	Laser on also connected to an NI digital input.
J1-4	LPON1	0V/+5V	Input	N/C	Laser on check connected to an NI digital output.
J1-5 to J1-9, J1-11 to J1-12, J1-16, J1-20, J1-24, J1-28 to J1-32	-	-	-	Direct	
J1-10, J1-13 to J1-15, J1-17 to J1-19, J1-21 to J1-23, J1-25 to J1-27, J1-33 to J1-36	GND	GND	Ground	Direct	Common Analogue and Signal Ground

These board-to-board connectors carries the laser board assembly signals between the PM1 Pachymeter main board and the Interface PCBA and will be mounted according to the following layout and dimensions:



A modified PM1 Pachymeter laser board will be mounted on the Interface PCBA via a SAMTEC FTMH-118-03-F-DV surface mount micro terminal strip board-to-board connector.

The modification will allow an analogue signal to be fed in to pin 2 IC2A via a 5.1M resistor.

3.2.2.1.4 Encoder Connector

The PM1 Pachymeter main board encoder connector (X7) will connect to the Interface PCBA via an FFC terminated at a MOLEX 54550-1033 FFC-to-board 0.50mm 10 circuit connector.

Pin	Signal	Level	Direction	Notes
X7-1	+5V5	+5V5	Power	Power
X7-2	GND	GND	Ground	Ground

Pin	Signal	Level	Direction	Notes
X7-3	M+	0V/+5V5	Output	Analogue H-Bridge Drive Output
X7-4	M-	0V/+5V5	Output	Analogue H-Bridge Drive Output
X7-5	A	0V/+5V	Input	Encoder A Channel
X7-6	B	0V/+5V	Input	Encoder B Channel
X7-7	~A	0V/+5V	Input	N/C on encoder board
X7-8	~B	0V/+5V	Input	N/C on encoder board
X7-9	Z	0V/+5V	Input	Encoder Z Channel
X7-10	LS	0V/+5V	Open Drain	Pull-up on the encoder board (S1 DNF)

This FFC carries the M+/M- analogue H-bridge drive and A, B & Z encoder signals between the PM1 Pachymeter main board and the Interface PCBA.

3.2.2.1.5 USB Pass-Through Connector

The PM1 Pachymeter main board USB connector (CN2) (or development board micro USB CN2 connector) will connect to the Interface PCBA via a standard USB-A connector (and a suitable cable). The interface board will facilitate pass through (via a switch) to a micro-USB-B connector that will connect to a PC using a suitable USB cable (e.g. micro-USB-B to USB-A or micro-USB-B to USB-C). The switch should facilitate switching both power and data on and off.

Pin	Signal	Level	Direction	Notes
1	VCC	+5V	Power	USB A Power
2	D-	0V/+5V	Ground	USB A Data -
3	D+	0V/+5V	Output	USB A Data +
4	GND	GND	Ground	USB A Ground

3.2.2.1.6 DUT Power Connector

A 2 way screw terminal connector will be provided to carry a switched 7.5VDC unregulated supply between the Interface PCBA and the PM1 Pachymeter development board. This allows connection of a DC barrel plug terminated cable or other suitable powering connector.

Screw Terminal	Signal	Level	Direction	Notes
1	0/+7V5	0/+7V5	Power	Power
2	GND	GND	Ground	Ground

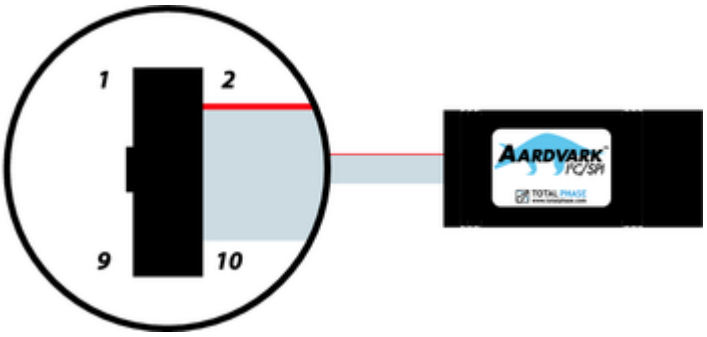
3.2.2.2 Test Platform to Interface PCBA

3.2.2.2.1 Interface PCBA Power Connector

The Interface PCBA will be powered from a 7.5VDC external power supply connected via a barrel connector from a wall-wart supply. This will be used to derive any other voltages needed on board.

Pin	Signal	Level	Direction	Notes
1	0/+7.5V	0/+7.5V	Power	Power
2	GND	GND	Ground	Ground

3.2.2.2.2 Total Phase Aardvark Connector



The Total Phase Aardvark I2C/SPI Host adapter connects to the Windows PC controlling the automatic test activity via a USB 1.1 Full-Speed (12 Mbit/s) interface.

The host adapter has a standard 10-wire 1.25 mm (0.050”) pitch cable terminated with a standard IDC 2.54 mm (0.100”) pitch IDC type connector.

The I/O signals used by the PM1 Pachymeter Automated System Level Test Platform will be connected through to the Interface PCBA via a standard IDC 2.54 mm (0.100”) pitch IDC type connectors and keyed boxed header.

Pin	Signal	Level	Direction	Notes
1	SCL	0V/+3V3	Open Drain	I2C Serial Clock with 2K2 pull-up resistor
2	GND	0V	Ground	Signal Ground
3	SDA	0V/+3V3	Open Drain	I2C Serial Data with 2K2 pull-up resistor
4	N/C			DNC
5	GPIO5	0V/+3V3	Output	Touch Panel IRQ (active low)
6	N/C			DNC
7	GPIO7	0V/+3V3	Output	Touch Panel Switching Control
8	GPIO8	0V/+3V3		Spare
9	GPIO9	0V/+3V3		Spare
10	GND	0V		Signal Ground

3.2.2.2.3 USB FT4232H Mini Module

The Interface PCBA will utilise an FTDI FT4232H mini module to provide a USB connection from a test PC to the microprocessor debug ports.

3.2.2.2.4 USB FT232H Breakout

The Interface PCBA will utilise an Adafruit FT232H breakout board to provide a USB connection from a test PC to drive SPI and GPIO interfaces for control of the input circuitry to pin 2 IC2A on the modified laser board (photodiode simulation).

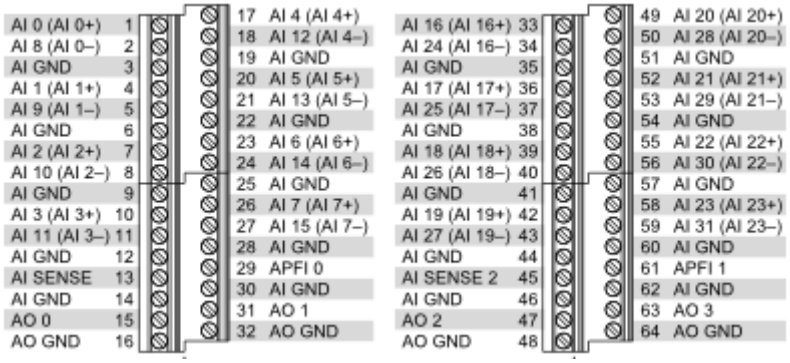
3.2.2.2.5 NI USB-6363

The NI USB-6363 connects to the Windows PC controlling the automatic test activity via a USB 2.0 Hi-Speed (480 Mbit/s) interface.

The NI USB-6363 has 128 screw terminals for termination of I/O connections. The screw terminals are designed to accept wiring from 0.2047 mm^2 to 1.3087 mm^2 (16 AWG to 24 AWG).

3.2.2.2.5.1 Analogue

The NI USB-6363 can provide up to 32 single ended or 16 differential AI channels and up to 4 AO channels.



3.2.2.2.5.1.1 Analogue Output

AO channel 0 will be connected through to the Interface PCBA via coax cable onto a 2 way screw terminal connector for onward processing on the Interface PCBA.

Screw Terminal	Signal	Level	Direction	Notes
15	AO 0	+/-5V	Output	Modified Laser Board - Photodiode Simulation
16	AO GND	AO GND	Ground	

Channel 0 will be used to interface to the modified laser board to drive the photodiode simulation.

3.2.2.2.5.1.2 Analog Input

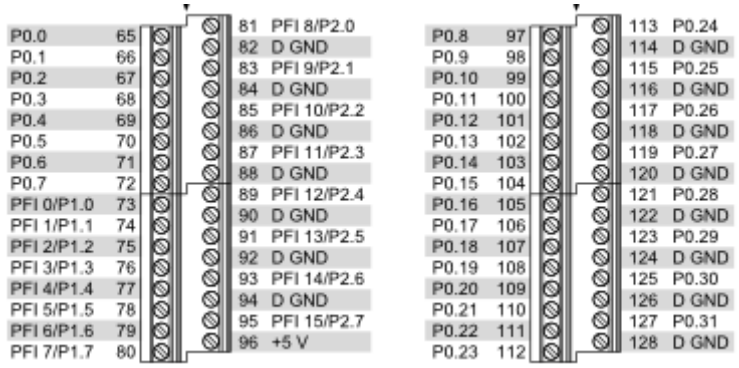
AI channel 0 through 7 configured as differential channels will be connected through to the Interface PCBA via shielded cable onto a 16 way 2.54mm pitch shrouded post header.

These channels will be used for monitoring purposes during integration and testing of the automated test platform. All monitoring lines shall be routed with jumper links located close to the source of the signal to allow removing any impact of the sensing line on the signals.

Pin	Signal	Level	Direction	Notes
1	AI 0+	+/-100mV to +/-10V	Input	Injected Signal (before 5.1M resistor)
2	AI 0-	GND		
3	AI 1+	+/-100mV to +/-10V	Input	Laser Board Vamp
4	AI 1-	GND		
5	AI 2+	+/-100mV to +/-10V	Input	Encoder M+
6	AI 2-	GND		
7	AI 3+	+/-100mV to +/-10V	Input	Encoder M-
8	AI 3-	GND		
9	AI 4+	+/-100mV to +/-10V	Input	Encoder A
10	AI 4-	GND		
11	AI 5+	+/-100mV to +/-10V	Input	Encoder B
12	AI 5-	GND		
13	AI 6+	+/-100mV to +/-10V	Input	Encoder Z
14	AI 6-	GND		
15	AI 7+	+/-100mV to +/-10V	Input	Spare (routed to spare IDC header)
16	AI 7-	GND		

3.2.2.2.5.2 Digital

The NI USB-6363 can provide up to 48 DIO pins 16 of which are programmable PFI lines that can be used not only as normal static digital input/output pins but also as timing input/output signals for AI/AO/DI/DO or counter/timer functions.



3.2.2.2.5.2.1 Digital Input/Output

DIO pins P0.0 - P0.3, P1.0 – P1.3 and P2.0 – P2.3 will be connected through to the Interface PCBA via a ribbon cable onto a 24 way 2.54mm pitch shrouded post header.

Pin	Signal	Level	Direction	Notes
1	P0.0	0V/+5V	Output	Encoder Board Connector – Encoder A Channel
2	D GND	GND		Signal Ground
3	P0.1	0V/+5V	Output	Encoder Board Connector – Encoder B Channel
4	D GND	GND		Signal Ground
5	P0.2	0V/+5V	Output	Encoder Board Connector – Encoder Z Channel
6	D GND	GND		Signal Ground
7	P0.3	0V/+5V	Output	Spare
8	D GND	GND		Signal Ground
9	P1.0	0V/+5V	Output	Laser Board Connector - LPON1
10	D GND	GND		Signal Ground
11	P1.1	0V/+5V	Output	DUT DC Power Switching Control
12	D GND	GND		Signal Ground
13	P1.2	0V/+5V	Output	USB Pass-Through Switching Control
14	D GND	GND		Signal Ground
15	P1.3	0V/+5V	Output	Spare (routed to spare IDC header)
16	D GND	D GND		Signal Ground
17	P0.4	0V/+5V	Input	Laser Board Connector - LON
18	D GND	D GND		Signal Ground
19	P0.5	0V/+5V	Input	Encoder Board Connector – H-Bridge Drive (M)
20	D GND	D GND		Signal Ground
21	P0.6	0V/+5V	Input	Spare (routed to spare IDC header)
22	D GND	D GND		Signal Ground
23	P0.7	0V/+5V	Input	Spare (routed to spare IDC header)
24	D GND	D GND		Signal Ground

3.2.2.2.6 DUT USB Pass-Through

The Interface PCBA will have a USB Micro-B connection for connection to a PC. All USB signals will be switchable under DIO software control so as to connect or disconnect through to the pass-through USB A connector that may be connected to the DUT via a USB A to USB C cable.

3.2.2.2.7 DUT Power Connector

The Interface PCBA will accept input from a +7.5VDC external power supply connected via a barrel connector from a wall-wart supply. This will be used to supply the switched screw terminal power output to the PM1 Pachymeter development board.

Pin	Signal	Level	Direction	Notes
1	0/+7.5V	0/+7.5V	Power	Power
2	GND	GND	Ground	Ground

3.2.3 Signal Routing and Conditioning

3.2.3.1 Display Connector

3.2.3.1.1 Touch Panel Simulation

The TP_INT, SDA3 and SCL3 touch panel signals will be switchable under DIO software control via the Total Phase Aardvark SPI/I2C Host Adapter configured to run in I2C and GPIO mode.

When automated testing is inactive these signals will be connected to the pass-through display connector on the Interface PCBA allowing normal LCD and touch screen behaviour.

When automated testing is active:

- TP_INT will be connected to a Total Phase Aardvark I2C/SPI Host Adapter GPIO pin allowing software control of the interrupt signal being fed to the PM1 Pachymeter main board. Both signals are +3V3 compatible so no further signal conditioning is required.
- SDA3 and SCL3 will be connected to the Total Phase Aardvark I2C/SPI Host Adapter allowing simulation of the I2C slave operation of the I2C touch controller. The host adapter and the PIC driving the display are +3V3 compatible and pull-up resistors for the I2C signals are provided within the host adapter so no further signal conditioning on the I2C clock and data signals is required.

3.2.3.1.2 Display Pass-Through

All signals coming from the PM1 Pachymeter main board display connector (X1), other than TP_INT, SDA3 and SCL3 will be connected directly to another MOLEX 54104-4033 FFC-to-board 0.50mm 40 circuit connector for pass-through connection to a display assembly via an FFC.

TP_INT, SDA3 and SCL3 touch panel signals will be switchable under software control between pass-through (default) and touch simulation modes.

3.2.3.2 Debug Connector

The four microprocessor serial debug connections will be connected to the digital inputs on the FT4232H mini module. The connections will be routed via 0R resistors.

3.2.3.3 Laser Board Connector

3.2.3.3.1 LON / LPON Simulation

The PM1 Pachymeter main board LON laser on command signal will be routed to a NI USB-6363 DI/PFI pin to allow software detection of the laser on command from the main board. It will also be routed to the modified laser board connector. The LON signal is 0V/+3V3 and is sufficient to drive the NI USB-6363 DI to a logic high.

An NI USB-6363 DO pin will be routed to the PM1 Pachymeter main board LPON1 laser on check signal to allow the simulation to confirm that the laser is on. The PIC32MZ102 is +5V input tolerant so this level does not need conversion but the connection will be carried via a simple voltage divider fitted with 0R and DNF resistors.

The actual LPON1 signal coming from the modified laser board connector remains not connected/unused.

All other pins on the laser board connectors are routed straight through.

3.2.3.3.2 Analogue Input Signal Simulation

The photodiode connection requires suitable level conversion / amplification and a software adjustable bias to be managed under software control. The control will be affected from the PC via the USB to SPI/GPIO breakout board.

The conditioned signal will be carried via a coaxial connection to the 5.1M resistor connected to pin 2 of IC2A on the modified laser board.

3.2.3.4 Encoder Connector

3.2.3.4.1 Detection of Analogue H-Bridge Drive Activity

The M+ and M- Analogue H-Bridge drive signals will be connected through a summing amplifier through a low pass RC filter and fed into a comparator along with an adjustable threshold set by a manual potentiometer. The output from the comparator will then be used to directly drive a NI USB-6363 DI/PFI pin. This will allow detection of, and triggering on, Analogue H-Bridge drive activity during automated testing.

3.2.3.4.2 Playback of Encoder Signals

The encoder A, B and Z channel signals will each be driven from a NI USB-6363 DO pin. These pins will be allocated sequentially in the P0 block supporting high speed synchronised digital waveform output. This will allow synchronised playback of encoder signals during automated testing.

As the NI USB-6363 is only enable to drive the waveform digital output at 1MHz channel B will be delayed by a 500ns delay line in order to ensure that both A and B do not both change on the same cycle as that will lead to undefined behaviour.