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Implement a clock-synchronous VHDL entity with a serial data input and an enable input signal to activate the entity.

The entity receives 16 bits as serial input, from the least significant bit (b0) to the most significant bit (b15), and transfer these 16 bits to a parallel, 8-bits output in 2 consecutive bytes with the format:

`[b15, … , b8]` followed by `[b7, …, b0]`.

Dati seriali = Serial data
abilitatione = enable
Uscita = Output