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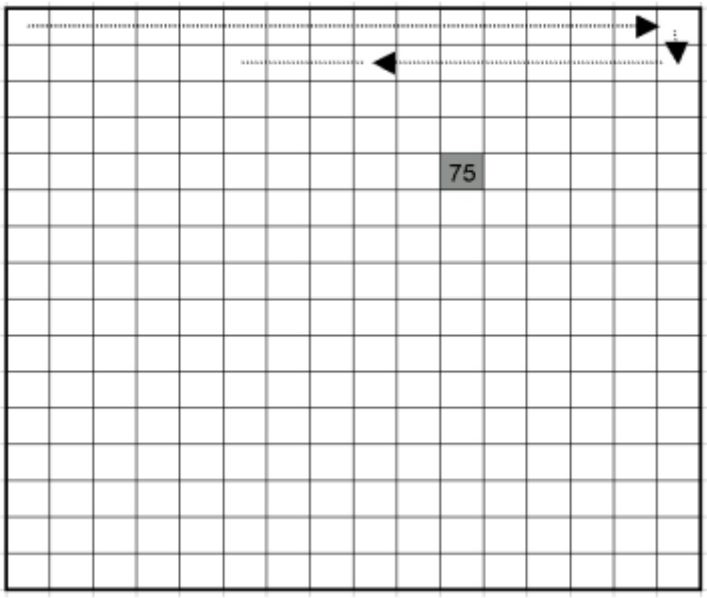
Create a clock-synchronous VHDL entity with two 4-bits inputs (**DATAX**, **DATAY**) and one serial output (**OUTPIXEL**).

The entity must pilot a 16x16 display as showed in the picture:



After receiving a pair of values at the inputs, the output must scan through the display, one pixel per clock cycle, starting from the top left pixel and proceed as shown in the picture. The output must be equal to 1 only at the position specified by the input signals.

Avoid the accumulation of data inside the entity.

When the entity is not enabled, the output must be set to high impedance.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity disdri is
      Port ( clk : in std_logic;
            en : in std_logic;
            datax : in std_logic_vector(3 downto 0);
            datay : in std_logic_vector(3 downto 0);
            outpixel : out std_logic);
end disdri;

architecture Behavioral of disdri is
signal cont: INTEGER :=0;
signal pixone: std_logic_vector(7 downto 0);
signal regx : std_logic_vector(3 downto 0);
signal regy : std_logic_vector(3 downto 0);

begin

p1:process(clk)
begin
if en='1' then
      if rising_edge(clk) then
            if cont=0 then
                  regx<=datax;
                  regy<=datay;
                  outpixel<='0';
                  cont<= cont +1;
            elsif cont >0 and cont <255 then
                  cont<= cont +1;
                  if cont=conv_integer(pixone) then
                        outpixel<='1';
                  else outpixel<='0';
                  end if;
            elsif cont=255 then
                  cont<=0;
            end if;
      end if;
elsif en='0' then
      outpixel<='Z';
end if;
end process;

p2:process(clk)
begin
      if rising_edge(clk) then
            if (regy and "0001") = "0000" then
                  pixone <= regy & regx;
            else
                  pixone <= regy & not(regx);
            end if;
      end if;
end process;
end Behavioral;
```