Applications of PSCAD® / EMTDC™

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Chapter 1:

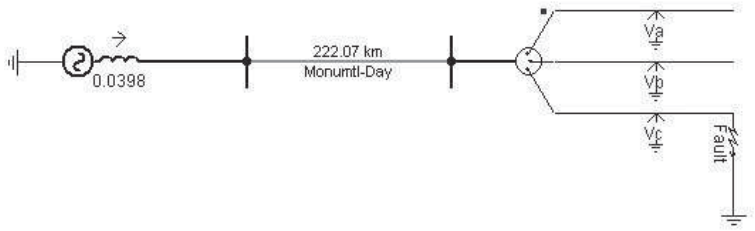
Introduction

This Workbook is designed to guide the user of PSCAD/EMTDC through its use and application. PSCAD/EMTDC (also referred to as PSCAD) is a simulator of ac power systems, low voltage power electronics systems, high voltage DC transmission (HVDC), flexible AC transmission systems (FACTS), distribution systems, and complex controllers.

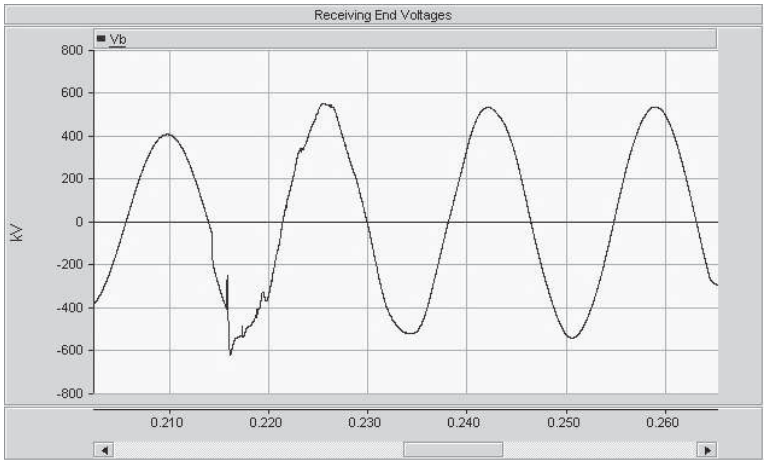
WHERE PSCAD CAN BE USED

PSCAD can represent electric circuits in detail not available with conventional network simulation software. For example, transformer saturation can be represented accurately on PSCAD and only superficially, if at all, on Phasor based simulators like power system stability programs.

A simple classical example of the use of PSCAD is demonstrated in the following example. A 222 km, 500 kV transmission line is open circuited at its far end, and it's C phase at that end is faulted. The voltage of B phase is plotted:



It is obvious from this example that the instantaneous solution algorithm of PSCAD and the precision achievable with it opens up great opportunities for investigation and study.



PSCAD is used by engineers, researchers and students from utilities, manufacturers, consultants, research and academic institutes. It is used in planning, designing, developing new concepts, testing ideas, understanding what happened when equipment failed, commissioning, preparation of specification and tender documents, teaching and research. The following are some of the studies that can be conducted with PSCAD:

- Insulation coordination of AC and DC equipment.
- Traditional power system studies, including TOV, TRV, faults, reclosure, and ferroresonance.
- Relay testing (waveforms) and detailed analysis of the CT/VT/CCVT responses and their impact on operation. Waveforms generated by PSCAD can be saved using PSCAD RTP/Comtrade recorder. Then, by using RTP Playback system, these waveforms can be used to test physical protection and control equipment.
- Designing power electronic systems and controls including FACTS devices, active filters, low voltage series and shunt compensation devices.
- Incorporate the capabilities of MATLAB/Simulink directly into PSCAD/EMTDC.
- Subsynchronous oscillations, their damping and resonance.
- Effects of DC currents and geomagnetically induced currents on power systems, inrush effects and ferroresonance.
- Distribution system design, including transient overvoltages, with custom power controllers and distributed generation.
- Power quality analysis and improvement, including hamonic impedance scans, motor starting sags and swells, non-linear loads, such as arc furnaces and associated flicker measurement.
- Design of modern transportation systems (ships, rail, automotive) using power electronics.
- Design, control coordination and system integration of wind farms, diesel systems, and energy storage.
- Variable speed drives, their design and control.
- Industrial systems.
- Intelligent multiple-run optimization techniques can be applied to both control systems and electrical parameters.

Applications of PSCAD/EMTDC

Case examples have been prepared for this Applications of PSCAD/EMTDC workbook and most examples can be used with the 15 node Student Edition of PSCAD.

The material is prepared to help launch the electric power engineer into useful and essential studies of power systems and controls. An understanding of the full power of PSCAD can only come with familiarity and use.

PSCAD/EMTDC is under continual development by a team of engineers and computer scientists at the Centre. Development direction is guided by the Technical Review Committee and the needs of the many users around the world.

Chapter 2:

Traditional Transient Studies

Traditionally, the greatest use of electromagnetic transients programs has been in the study of switching surges in AC networks (PSCAD/EMTDC enables the scope of transients studies to be broadened to include detailed control systems and power electronics).

SOURCES

When transients are being studied, the whole network usually does not need to be modeled as it does in transient stability studies (where the transients are much slower and can reach further into the network). Care is required in selecting the sources representing the short circuit impedance and where the source is located.

Thevenin Voltage Sources

The simplest Thevenin source representing the AC system and its short circuit impedance at the selected busbar is a series R – L. This can be found accurately for fundamental frequency, particularly if the short circuit capacity is known through a separate study. There are two main types of Thevenin sources in the Sources page of the Master Library. Sources can be internally or externally controlled in terms of source voltage magnitude, frequency and phase.

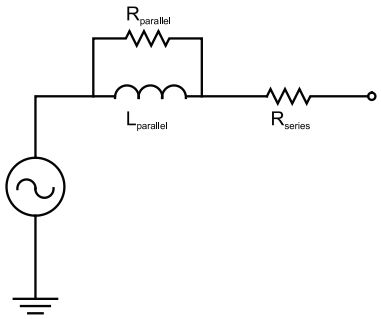
The first source type is the "Three Phase Voltage Source" component and the "Single Phase Voltage Source" component. To recognize that there is frequency dependency in the short circuit impedance, simple impedance fitting through the low order harmonics is possible with the series R-R//L impedance configuration. Zero sequence definition is possible.

Various sources are available in the Sources page of the Master Library. Externally, controllable current and voltage sources provide special interface capabilities between controls and the network.

Load Flow Set-up with a Source

When including more than one source or generator in an AC network model, it is important to ensure the load flow is correct. Now, the load flow solution of the same network will provide the voltage magnitude, phase and power and reactive power generated or absorbed at the terminals of the Thevenin sources.

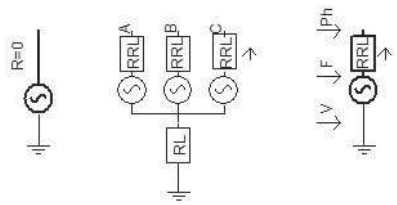
The voltage behind the Thevenin impedance or that at the bus may be specified. If the voltage at the bus is specified, the desired P and Q levels of the source are also required. The model will compute the internal voltage behind the Thevenin impedance.



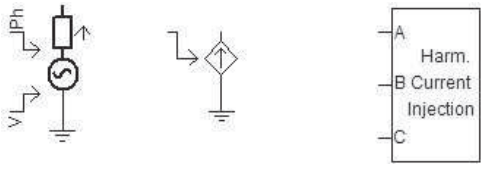
R-R//L configuration of Thevenin source impedance, selected to provide the same impedance angle at fundamental frequency and one low order harmonic (2nd, 3rd of 4th).

Sources representing network equivalents and their short circuit contributions should include resistive damping to reflect the effect of loads and losses in the network.

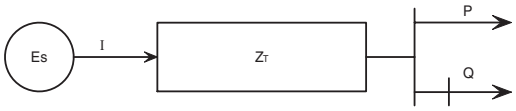
This is realized in single and three phase source components in the Sources page of the Master Library:



Ideal source realizable (R=0.0) through Simple Three Phase Source component. Provides chatter removal, but has no separate zero sequence impedance definition.



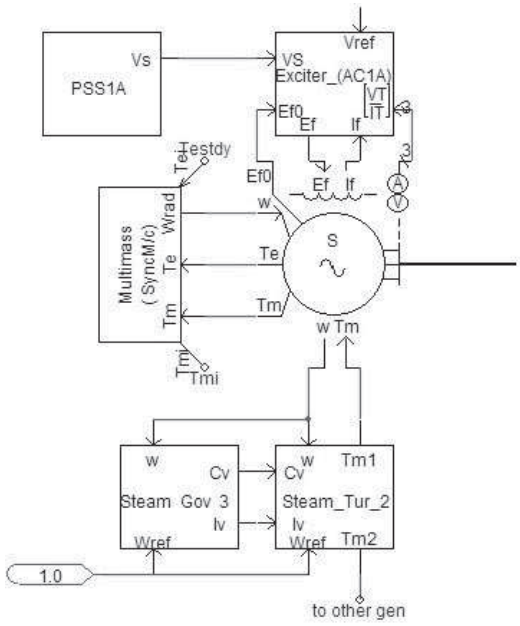
Special sources including a harmonic current injection source for measuring harmonic impedance among other things.



$$I = P - \frac{jQ}{V_T}$$

$$E_S = V_T + I * Z_T$$

Calculation necessary for each fixed network source when the terminal voltage VT magnitude and phase is known from the load flow, as well as the power P and reactive power Q that the source generates, and knowing short circuit impedance ZT.



Example connection of synchronous generator with an IEEE Exciter (Type AC1A), a stabilizer, a combined cycle turbine and governor, and a shaft torsional model. It is not always necessary to model all these functions. A library of IEEE standard exciters and power systems stabilizers is available in the Machines page of the Master Library.

The reference on the IEEE standard exciters is:
"IEEE Recommended Practice for Excitation System Models for Power System Stability Studies" IEEE Std 421.5-1992.

Setting the Load Flow with a Generator

When one or more synchronous generators are to be connected into the network, the load flow process is a little easier (even if the generator set-up is more complex). Each generator can start the case during initialization (beginning at TIME = 0.0) with a three phase fundamental frequency voltage source (with no impedance) connected at its terminals. Its magnitude and phase is fixed as designated within the machine's data input sheets.

The general method of initialization and start-up, which is suggested be normally used, is based on entering firstly the terminal voltage magnitude and phase. The start-up sequence is:

1. At time=0, machine is a fixed source at its terminals, whose voltage magnitude and phase is as entered by the user, which might correspond to the values obtained from a load flow program solution of the network.
2. The network solution progresses from the start-up with the voltage source firmly fixed so that the network can reach its steady state condition. To ensure that the steady state condition of the network is reached smoothly, the source voltage magnitude may ramp to its specified value over a time interval entered by the user.
3. When the steady state of the network has been reached, the user may choose to convert from the voltage sources representing each machine to an actual machine model, rotating at a fixed speed of 1 pu. At the time of transition from source to machine model, IEEE exciter and stabilizer models (if used with the machine model) can be initialized so that the transition from source to machine is seamless.
4. If for some reason, parts of the system still need to reach the steady state, the machine in its constant speed state with the excitation system active can be run until the user is satisfied. At this point in time, the rotor can be 'unlocked' on all machines. When this transition occurs, any IEEE governor/turbine system, including any torsional multi-mass model of the turbines, shaft and generator, can be instantly initialized (if proper initialization procedures have been followed) and the whole system will now run free and in steady state. Mechanical torque input to the machine can be derived from the governor/turbine combination, if desired. If for some reason a perturbation is evident or the system is not settling down to a steady state condition, investigate whether initialization procedures have been followed correctly or whether the system is dynamically stable. For example, excitation systems may not be adequately designed and may contribute to electromechanical instability (this can be quickly verified by replacing the exciters driven input to the machine by a fixed constant value). When systems with many synchronous machines are being modeled, it is always a good idea to be satisfied the system is

dynamically stable when run on a power system stability program.

5. At the point in time when the machines are running free and the excitation and governor systems are stable, a 'snapshot' can be taken. Faults and disturbances can be applied to the system with start-up commencing from the snapshot.

There are ten examples of synchronous generator connections in the tutorial available with PSCAD under PSCAD\examples\tutorial\machines.

MULTIPLE RUN

Having the ability in PSCAD/EMTDC to repeatedly run a case is a valuable resource to search for best performance of controls, maximum switching transient overvoltages, and changing the type and application of disturbances.

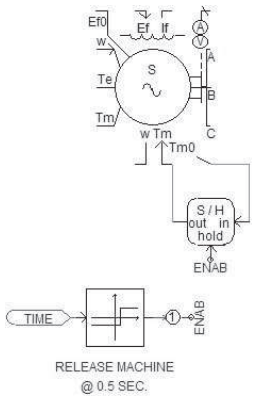
Multiple Runs can be accomplished by two methods:

1. Using the Multiple Run component with the following features:
   - Up to six variables can be modified with different values for each successive run.
   - Operate in either sequential or random mode.
   - Support for real and integer variable types
   - Up to six input variables can be recorded for each run.
   - Automatic processing of input variables (min, max, |max|, Integral Square Error).
   - Statistical summary of the recorded data.

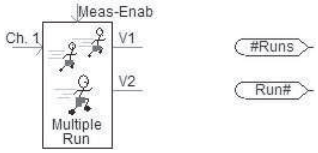
2. Manually defining the multiple run variables with these limited features:
   - Set the number of runs in the Case Properties from the Project Tree.
   - Variables for the current run number and the number of runs can be used in conjunction with any other components to create multiple run variables. Control blocks or logic functions can then use the current run number and the total number of runs as input to compute the variables being modified for each run.

If the Multiple Run component is used, it will automatically set the number of runs depending on the selected variation method. More than one Multiple Run component can be placed in the same circuit, but only one of them can be enabled during a particular run. For Multiple Run components that are disabled, parameter values should be entered in the "Real" (or "Integer") fields of the first data sheet.

If a Multiple Run component is used, the multiple run setting in Case Properties from the Project Tree must be left set at 0 runs.



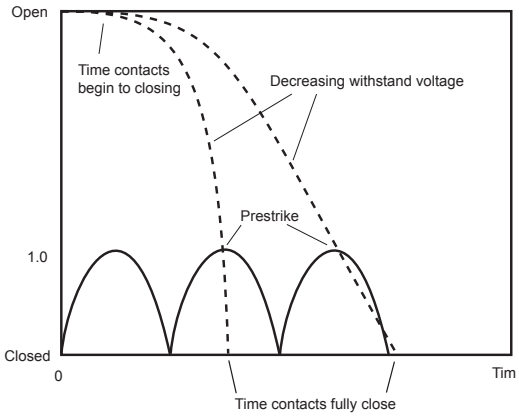
A useful component for initializing generation equipment is Sample and Hold (S/H). Any output from generation equipment ending in 0 (eg. Tm0) is an initializing function. The S/H component will sample and hold its input as an output at the time the "hold" input signal changes from integer 0 to integer 1 (as "ENAB" does in this case when a governor is not required).



Multiple Run components in the I/O_Devices page of the Master Library.

Selecting the number of signals output for the Multiple Run component. Sequential or Random mode may be selected. Note that the multiple run feature can be disabled if only a single run is required.

Data sheet for Multiple Run component defining the recording channels information.



Pre-strike effect in closing circuit breakers with a finite closing time.

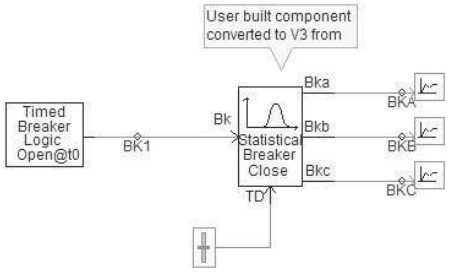
Speed of operation of a 230 kV, SF6 circuit breaker was found to vary with temperature, SF6 pressure, hydraulic energy and dc voltage according to a test undertaken by the Manitoba HVDC Research Centre as follows:

Variations in closing speed: 8-10%

Variations in opening speed: 5-6%

One supplier provided the following circuit breaker closing times:

110 kV	30 +/- 10 msec.
220 kV	65 +/- 8 msec.
220 kV	80 +/- 5 msec.
500 kV	80 +/- 5 msec.



User defined component for modeling circuit breaker pre-strike along with a Multiple Run component to generate a random time over a one cycle spread for the contacts to commence closing.

The Breaker Pre-strike component has a built-in statistical function that computes the individual pole closing time from the standard deviation of closing time.

Breaker Pre-strick component. Input Bk is to initiate three phase circuit breaker closing or opening (0 to close, 1 to open), TD is the delay time (msec) before the contacts actually commence to close after initiated by signal to Bk. Output signals Bka, Bkb and Bkc are the actual circuit breaker contact make or break indicators.

ENERGIZING TRANSIENTS

The traditional method of representing a circuit breaker for energizing transmission lines, transformers, capacitor banks, etc. in transient studies is to assume that the contacts can close on any part of the cycle. In reality, there is a closing time between when the contacts start to close and when they finally make. Somewhere in between, an arc may strike across the contacts as they close. This is known as "pre-strike."

Breaker Pre-Strike

The vertical axis in the figure is a measure of the withstand voltage across the circuit breaker contacts. In the open position, the withstand voltage of the circuit breaker will be a per unit value of rated voltage. The time varying value of voltage across the open contacts is depicted as an absolute function of the alternating voltage across the contacts. As the contacts close, the withstand voltage reduces as the separation distance between the contacts reduces. When the voltage across the contacts exceeds the reducing withstand voltage of the insulating medium between them, pre-strike occurs.

As a result of the pre-strike, there will be a greater tendency for effective closing to occur with rising or maximum voltage across the contacts. For slow contact closing, there will even be a shadow effect where it will not be possible for effective closing to occur over a portion of the cycle.

A user-defined component has been developed to model the pre-strike effect of circuit breaker closing. The closing time is specified in msec. However, each phase may close with a slightly different speed, and so a standard deviation is specified in the component. During a multiple run, each phase of the circuit breaker closes based on the mean closing time and the variation on this defined by the standard deviation.

To ensure there is a random initiation of the circuit breaker closing, the Breaker Pre-strike component has an input designated TD that is a time delay (in msecs) before the poles actually commence to close after the Timed Breaker Logic component (or other signal) has initiated closing. By randomly changing TD with the Multiple Run component over a period of one cycle (0 - 20 msec if a 50 Hz system or 0 - 16.667 msec if a 60 Hz system) during successive runs, line energizing studies can be accomplished. A probability distribution of maximum line energization overvoltages can be obtained as impacted by breaker pre-strike and the random closing period over one cycle.

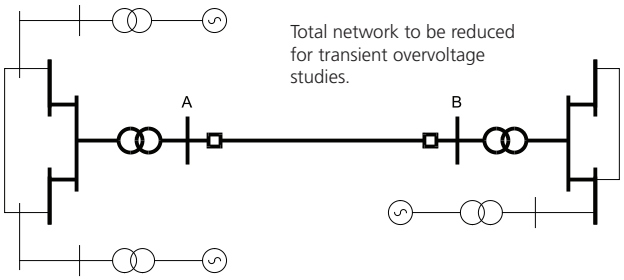
The record of maximum line energization overvoltages for each randomly switched closing is preserved in a multiple run output file designated in the Multiple Run component properties sheet Edit Parameters Recording Data Config Base Output File Name. This multiple run output file must have an ".out" extension, and will record all the output channels of the Multiple Run component for each run in one file. The output is statistically processed

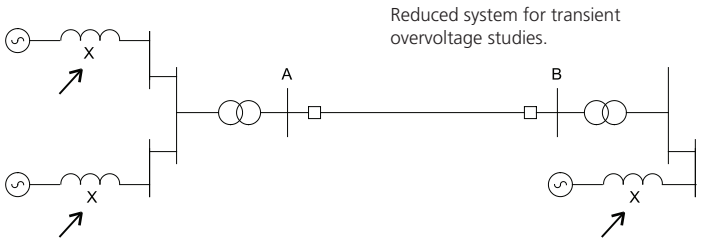
for a probability distribution of maximum line overvoltages for use in transmission line design.

SWITCHING SURGE DATA REQUIREMENTS

AC insulation coordination studies will investigate surge arrester ratings and insulation levels for substation equipment. The studies will provide a check for, and the coordination of, the Basic Impulse Levels (BIL) of existing and new AC substation equipment. For substations with voltages up to 110 kV and 220 kV, lightning will have the major impact on surge arrester selection. For substation equipment at 345 kV and higher, transient overvoltages from switching surges may have greater impact on surge arrester selection and substation equipment insulation levels.

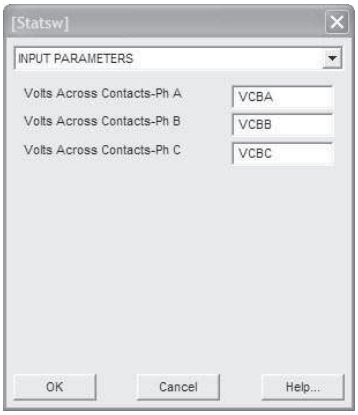
System Equivalents for Switching Surge TOV Studies
A reduced network diagram must be developed which should include detailed transmission line and transformer data for at least two busbars away from the substation busbars under study (for the network representation beyond the two busbars, a three phase equivalent source with positive and zero sequence impedances can be applied at the second busbar removed from the busbar under study which serves as an interface busbar). The value of the source impedances will be based on the short circuit impedances.





The network example shown below is to have the portion in thicker lines modeled in detail in PSCAD/EMTDC for study of the transmission line between Station A and Station B. The network portion shown by thin lines is to be reduced to short circuit equivalents X1, X2 and X3, as also shown below.

The short circuit impedances X1, X2 and X3 shown in this example should be more than just a simple inductance. At the



Data sheet for Circuit Breaker Pre-Strike component defining essential input parameters for multiple run analysis of energization.

Note: Contact withstand strength should exceed the peak transient recovery voltage for the circuit breaker. Based on IEC Standard 60056, the peak transient recovery voltage is 1.82 per unit for HV circuit breakers.

Even though switching surges may not have the major impact on substation insulation design and coordination at voltages below 345 kV where lightning effects could be dominant, transient recovery voltages on circuit breakers have to be evaluated by studies which utilize switching surge level data.

Short circuit impedances for the short circuit capacity contributed by the portion of the system which is not to be included in detail in the rest of the system but has been reduced to provide the same short circuit capacity at busses A and B as if the total network was represented. Note that the short circuit impedances are representing the reduced equivalent of the network beyond two busses away from the main busses A and B being studied.

very least, the sources should represent a resistive portion modeled with the series R-R//L impedance configuration of the Three Phase Voltage Source component. The zero sequence portion of the short circuit impedances should also be modeled with the sources. It is preferable that X1, X2 and X3 should be frequency dependent network equivalents.

It may not always be possible to obtain the equivalent short circuit impedances X1, X2 and X3 as described above. Another way to ensure they are correctly entered if they are not available, but the total short circuit capacity at each location is known, is to build the case with estimated values for X1, X2 and X3. Then, when the model is fully assembled, apply short circuits at the strategic busses, and manually vary X1, X2 and X3 until the desired short circuit capacities are measured.

The short circuit impedances X1, X2 and X3, as described above for each of the Three Phase Voltage Source components, are required both for maximum expected short circuit capacity over the life of the station equipment, and for minimum expected short circuit capacity.

Power Flow Conditions

Typically, the investigation should cover the probable/worst system operating conditions throughout the expected life of the equipment. The power flow should include fundamental frequency voltage angles and magnitudes so that the internal source voltages and angles can be determined.

The load flow conditions for maximum expected power flow through the study system at maximum and minimum short circuit capacity are typically used in studies. Another load condition may be a light power flow condition for maximum and minimum short circuit capacity.

Transmission Line Data

Transmission line and cable data is applied to the line and cable constants components of PSCAD to generate the line and cable models.

For each transmission line represented in the network diagram, dimensions and data are required. This can be given at the tower, and should include conductor sag. Shield wire dimensions and resistance should also be provided. The transmission line data required includes:

- Transmission line conductor diameter and resistance per unit length (can also be selected from a user-defined list for standard/commonly used conductors).
- Total length of each transmission line.
- Phase transformation data and distances between phase transformations.
- Spacing between conductors in a phase bundle.
- Spacing between phases.
- Shield wire diameter and resistance per unit length.
- Height of each conductor and shield wire at the tower and sag to midspan, or average height of each conductor and shield wire above ground.
- Tower dimensions (a diagram of the towers with dimensions is useful).
- Ground conductivity.

Transformer Data
For each transformer to be represented in detail, the following information is required for the PSCAD transformer components:

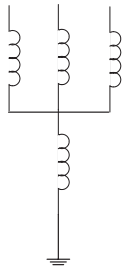
- Transformer MVA rating.
- Winding configuration and winding voltage.
- Transformer tap change ranges and normal setting.
- Leakage reactances between windings (this information can be obtained from the load flow data used in system operating studies if not readily available from the name plate data).
- Knee point of transformer core saturation characteristic in per unit of rated flux or voltage.
- Estimated saturated air core reactance of transformer and the winding it is based on (see PSCAD online help for more details).

Circuit Breakers
The locations of the circuit breakers that will be switched must be identified on the study system network diagram. Other parameters of the circuit breakers should be determined from the study:

- Protection delay or clearing times.
- Maximum fundamental frequency switching voltage.
- Maximum capacitive switching capability.
- Reclosing sequences and whether they will be used.
- Rated transient recovery voltage and maximum rate of rise of transient recovery voltage.
- Mechanical closing time (msec) and variation in pole closing times. This is of particular importance if point-on-wave closing is to be investigated.
- Half cycle closing resistor range of values and the additional cost for such.

Surge Arresters
The expected location and rating of surge arresters should be provided. The minimum ratings, and in particular the energy absorption capability, will be determined from the studies.

Shunt Reactors
The location of shunt reactors should be identified. This will include whether they are line connected (located on the line side of the energizing circuit breakers) or bus connected (located on the station side of the line energizing circuit breakers). Information on whether the shunt reactors are switched and if so, the time it takes to close its switch to connect it into service and the time delay to switch it out of service.



Configuration of line connected shunt reactors with a neutral reactor for compensating long AC lines utilizing single pole reclosing.

The reactor rating should be supplied along with its characteristic if it is a saturating reactor. If single pole switching is required for the transmission line, line connected shunt reactors connected to a neutral reactor may be necessary on long lines to assist in the reduction of secondary arc current.

Note: A saturable reactor can be implemented in PSCAD using a suitable transformer model.

Note: The grounding impedance of different equipment will have an impact on the magnitude and the nature of the transients and the over-voltages.

Shunt and Series Capacitors
It is important to include shunt and series capacitor data and the associated equipment, such as switches, circuit breakers, surge arresters, etc. to ensure their effects are included in the transients study.

Note: In series capacitor related studies, the bypass protection of the capacitors may have to be adequately represented.

FAST FRONT STUDY DATA

Lightning effects generally occur over 50 to 100 µsecs and consequently, line lengths need only be long enough to ensure that wave reflections return after they have any impact on surge arrester operation.

To minimize reflection effects if an overhead transmission line is modeled for fast fronts with a shorter length, they can be terminated with resistors representing the surge impedance of the line located at the end away from the busbar under study.

Lightning studies are important for insulation design of stations at voltages below 345 kV. The system modeled for lightning studies will largely entail a fast front model of the busbar under study, the transmission lines directly connected to the busbar for several kilometers away, and the transformers also connected to the busbar.

Station Layout
A detailed station layout diagram is required which should contain or be accompanied by the following information:

- Physical length of each busbar section between station equipment.
- Location of each circuit breaker.
- Location of each transformer.
- Location of wound potential transformers and lead length.
- Location of capacitive divider potential transformers and lead length.
- Location of current transformers.
- Location of shunt reactors (and shunt capacitors) and lead lengths.
- Location of disconnect switches.
- Location of every transmission line entrance.

Calculation time steps for steep front studies of transmission stations is usually in the range of 20 to 50 nanoseconds.

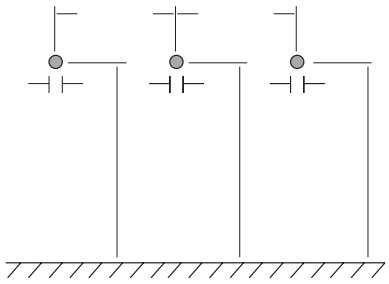
- Power line carrier blocking filters and the filter values (ohm, µF and H).
- Anticipated location of surge arresters and tentative ratings.

Busbar Dimensions

The fast front surge usually enters the station from a transmission line as a result of lightning striking a tower top or shield wire near the station causing a back flashover, or directly onto a phase conductor. The surge propagates through the station along the busbar. It is appropriate to represent the overhead busbar as a transmission line if its length is greater than the length of wave propagation over two calculation time steps. The data required is similar to that for transmission lines as follows:

- Busbar conductor diameter and resistance per unit length.
- Spacing between busbar conductors and phases.
- Average height (or height at supports and sag) of each busbar conductor above ground.
- Length of any vertical sections of busbar.

Overhead busbar sections and lead lengths shorter than the wave propagation distance of two time steps can be modeled as lumped inductance at 1 ¼H/metre.



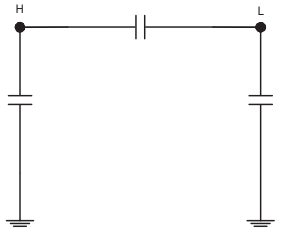
Busbar and transmission line dimensions

Ground conductivity for the line constants component for calculation of transmission lines for busbar sections can be assumed to be low because of the station ground mat. Values of 1 to 10 Ù-metre may be suitable.

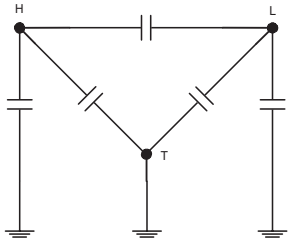
Transformer Data

Each transformer connected to the station busbar under study will have a strong influence on fast front surges due to the dominant bushing and winding capacitances. Usually the bushing and winding capacitances are lumped values determined by test measurements. The magnetic coupling and winding inductance are considered to have no effect for fast front surges.

If the transformer is considered open circuited except at the winding connected to the busbar under study, the winding capacitances can be lumped into a single value for that bus connection.



Equivalent circuit of the capacitance coupling of one phase of a two winding transformer.



Equivalent circuit of the capacitance coupling of one phase of a three winding transformer.

Transformer Winding Capacitances

Manitoba Hydro measured lumped winding capacitances on two winding single phase distribution transformers with 600 volt secondary windings. This information is provided as a resource as follows:

Legend:

CH = Capacitance H to Ground (pF)

CL = Capacitance L to Ground (pF)

CHL = Capacitance H to L (pF)

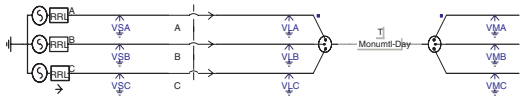
Measured winding capacitances one phase of a Y-Y-Ä HVDC converter transformer, whose three phase rating is 341 MVA, 138/134/13.8 kV as follows:

CH = 13,000 pF (winding closest to core)
CL = 4,000 pF
CT = 10,000 pF
CHL = 4,000 pF
CHT = 6,000 pF
CLT = 8,000 pF

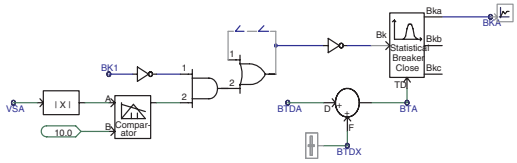
Note: Phase-to-phase capacitances are considered negligible.

Example of energizing a transmission line with Point-on-Wave closing.

Consider the 500 kV transmission line:



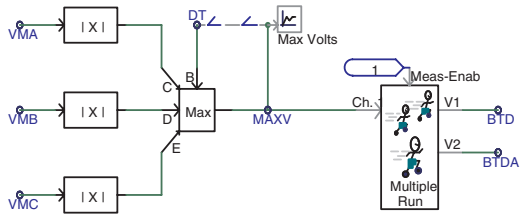
Each pole of the circuit breaker must be individually controlled. The closing signal "BKA" for the pole on phase A must be initiated knowing that the closing time of the pole is fast and consistent. The same applies for the other two breaker poles.



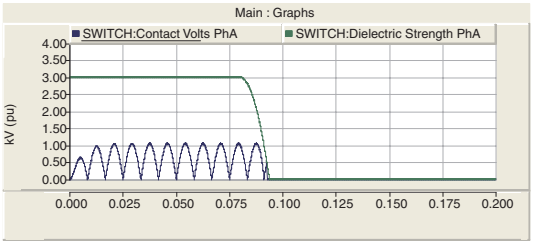
Consider Phase A:

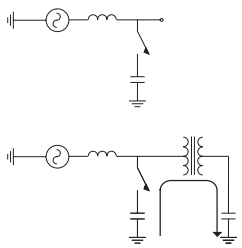
Supply side phase voltage VSA is monitored and the absolute value of the signal is fed into a comparator. This establishes a common reference time if the closing signal BK1 is received to initiate breaker closing.

The Statistical Breaker Close component receives the "close" signal, but it is delayed by manual setting BTDX and a random statistical varying signal BTDA (from the Multiple Run Component).



Signals VMA, VMB and VMC are line end voltages. Signal BTD randomly initiates circuit breaker closing over one cycle. Signal BTBA adds a 0.1 msec random variation to manual delay adjustment BTDX, which is adjusted by trial and error for pole closing at voltage zero. Signal BTA is fed to the Statistical Breaker Close Components on the other two phases. Signal BK1 from the Timed Breaker Logic Component is also fed to the other two phases.





Capacitor switching configurations that can lead to overvoltages.

NOTE: IEEE Standard C37.011-1994 lists typical stray capacitance values of station equipment.

SWITCHING SURGE TOV STUDIES

The objective for switching surge transient overvoltage studies is to size surge arresters and ensure equipment insulation levels are adequate. For EHV lines and stations where switching surges are a deciding factor in this regard, there is incentive to minimize the transient overvoltages to lower new equipment costs or limit the voltage stresses on aging equipment still in service.

Limiting Fundamental Frequency Load Rejection Overvoltags

It is inevitable that when one end of a heavily loaded and long transmission line opens up because of a fault in the ac system, the delay before the protection cross trips the other end to de-energize the line may result in a large load rejection fundamental frequency overvoltage with possible harmonic voltages superimposed. Careful design is required to ensure the overvoltage is not greater than the equipment or nearby loads can withstand. The circuit breaker to clear the transmission line must be able to break the capacitive current of the open circuited line at the load rejection overvoltage. This may entail having line reactors or controlled or rapidly switched compensation in place to assist the circuit breaker in this duty.

Line Energizing

There are a number of line energizing contingencies that need to be examined for impact of switching surge TOVs. These include:

1. Energizing or reclosing the transmission line with a single line to ground fault on the line.
2. Out-of-step closing, or closing with a large angle and voltage across the circuit breaker.
3. Energizing a transformer, or a transformer and a transmission line.

A statistical switching study undertaken for these cases and variations thereof will determine the maximum switching transients possible. The accumulated probability of distribution of transient overvoltages can be determined using the multiple run feature of PSCAD and the Breaker Pre-Strike component discussed above. From the most severe conditions, the voltage stresses and arrester duties can be examined and adjustments made.

Reduced switching surge transient overvoltages can be designed with closing resistors or point-on-wave closing.

Shunt Capacitor Switching

Shunt capacitors, when switched or when fixed away from where the switching is occurring, can cause significant transient voltages. The transient overvoltages tests because of capacitor bank switching are [2]:

1. Capacitor bank energization. If the system impedance is inductive and lightly damped, the energization of the capacitor bank will set up oscillating voltages.
2. Resonance with lower voltage capacitors. If a fixed capacitor bank is removed from the bank being energized through a transformer, the normal oscillations generated on the main bank being energized can set up sympathetic oscillations with it. The overvoltages on the fixed bank may be larger than across the bank being energized.
3. Transformer phase-to-phase overvoltages. Transient overvoltages generated by capacitor bank energizing can reflect at a transformer terminal and are limited by the surge arresters. If the transient overvoltages are of opposite polarity on two phases, the phase-to-phase transient overvoltages may be twice the line-to-ground overvoltages and be very stressful to the transformer.
4. Breaker re-strike. The surge arrester across the capacitor bank may be stressed if the circuit breaker re-strikes. It is usual to size the surge arrester to withstand one re-strike, even when the circuit breaker is designed to be "re-strike free."
5. Switching capacitor banks back-to-back. To limit the inrush current due to back-to-back switching, an inductor is placed in series with the capacitor bank.
6. Capacitor discharge into nearby fault. A current limiting reactor will limit the peak discharge current from the capacitor bank into a nearby fault. ANSI standards establish a maximum value of 2 * 107 for the product of the peak magnitude of the discharge current and its frequency.

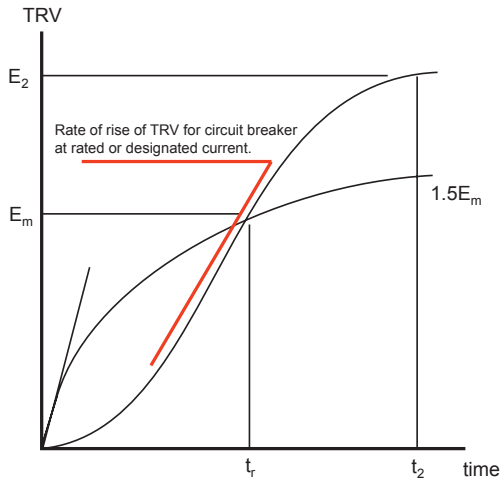
Other overvoltages of concern are generated by load rejection overvoltages which in causing nearby transformer saturation may, through resonances, lead to prolonged harmonic overvoltages on the terminals of the transformer or other equipment.

Capacitor switching surge overvoltages can be limited by circuit breaker closing resistors and capacitor bank current limiting reactors.

TRANSIENT RECOVERY VOLTAGE (TRV)

Transient recovery voltage of a circuit breaker is the difference of voltage measured between each side of the circuit breaker to ground.

The most severe TRV from an amplitude point of view, follows the interruption of the first phase to clear an ungrounded three phase fault. The shift in system neutral results in a high amplitude TRV. However, the probability of this fault ever occurring is low, but it is a basis for rating a circuit breaker's TRV capability.



For TRV analysis, the above curves can be defined based on the published capabilities of the circuit breaker:

E_2 = Maximum TRV published for the breaker. May be a function of load current and power factor. This is a 1-Cos curve at fundamental frequency.

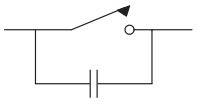
E_m = The line-to-ground component of the TRV at fundamental frequency.

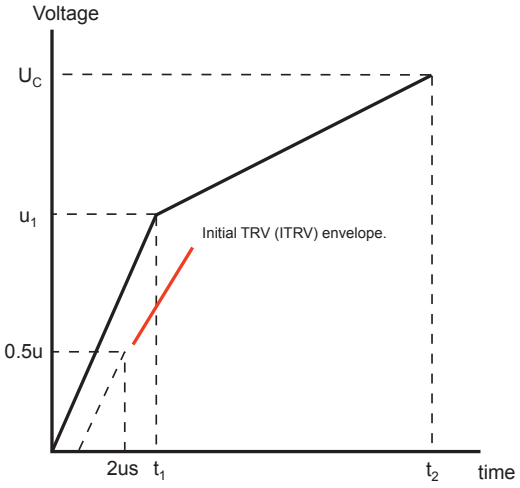
t_r = Time the first reflection is observed.

At rated current, the circuit breaker can then be applied if the observed TRV lies below the defined envelope. Use the three phase ungrounded fault for the test.

The concept of Initial TRV (ITRV) is introduced by IEC Standard 60056 (1987-03). This is due to substation reflections and may cause initial higher rate-of-rise but to a smaller initial amplitude. An ITRV envelope is defined to accommodate ITRV.

ITRV is neglected for metal enclosed switchgear and when rated short circuit current is less than 25 kA.





A circuit breaker clearing a capacitor bank is also prone to re-strike due to the TRV.

The transmission lines and equipment connected to the station busbar impact the TRV for the three phase ungrounded fault test. In studying the transient recovery voltage, ensure that all suitable lines, transformers and bus equipment are represented in the transient simulation. It is a good idea to include a lumped capacitor to ground on each phase of the station busbar to encompass all bushing, winding and stray capacitances which might exist at the station. The value used will be an approximation dependent upon the number of transformers and other equipment connected to the busbar.

(See IEEE Standard C37.011-1994 for typical stray capacitance values)

The most severe case for rate of rise of TRV is when the circuit breaker is fed from only transformers (no other transmission lines) from its substation side. When the circuit breaker opens to clear the line fault, it does so at a current zero. But since the fault is fed through the transformer, which is inductive, the current zero for current extinction corresponds to a voltage maximum for the source voltage behind the transformer. Consequently, there is a fast rise of voltage on the transformer terminal of the cleared phase, limited only by the capacitances of the transformer windings, bushings, buswork, circuit breakers, voltage transformers, etc. When there are only one or more transformers feeding the fault clearing circuit breaker, these capacitances should be lumped onto the bus on the substation side of the circuit breaker.

Many modern circuit breakers have a grading capacitor across each set of main contacts that helps limit rate-of-rise of TRV. For modern classes of SF6 circuit breakers, it is typical to have 800 to 1600 pF across each set of contacts. 1500 pF is a normal value to use if a specific circuit breaker is not being studied. 230 kV circuit breakers will have two heads in series so that 750 pF can be used. 500 kV circuit breakers have four heads in series resulting in 375 pF as the equivalent value to use.

The grading capacitor will have negligible effect if there are one or more transmission lines in operation at the substation bus where the circuit breaker being switched is located. Where the fault clearing circuit breaker is only connected to transformers at the substation, the grading capacitor should be included in the model along with a lumped shunt capacitor for the transformer windings, bushing, buswork, voltage transformers, etc. Although fast front modeling is not required, the calculation time step should be around 10 to 20 sec when adding these capacitors rather than the normal 50 sec.

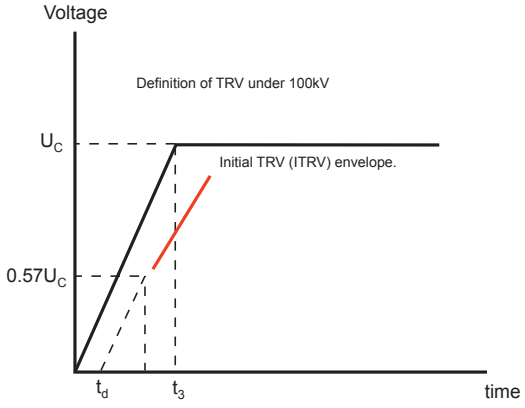
According to IEC 60056 standard, circuit breakers directly connected only to transformers without appreciable additional capacitance between the circuit breaker and transformer, the

Definition of TRV in IEC 60056 (1987-03)

U kV	u_1 kV	t_1 µsec	u_c kV	t_2 µsec
123	131/151	65/75	183/211	195/225
145	154/178	77/89	215/249	231/267
245	260	130	364	390
300	318	159	446	477
362	384	192	538	576
420	446	223	624	669
525	557	279	780	837
765	812	406	1137	1218

For specifying TRV, u_1/t_1 and u_c may be used. Rate of rise u_1/t_1 is a maximum of 2 kV/sec.

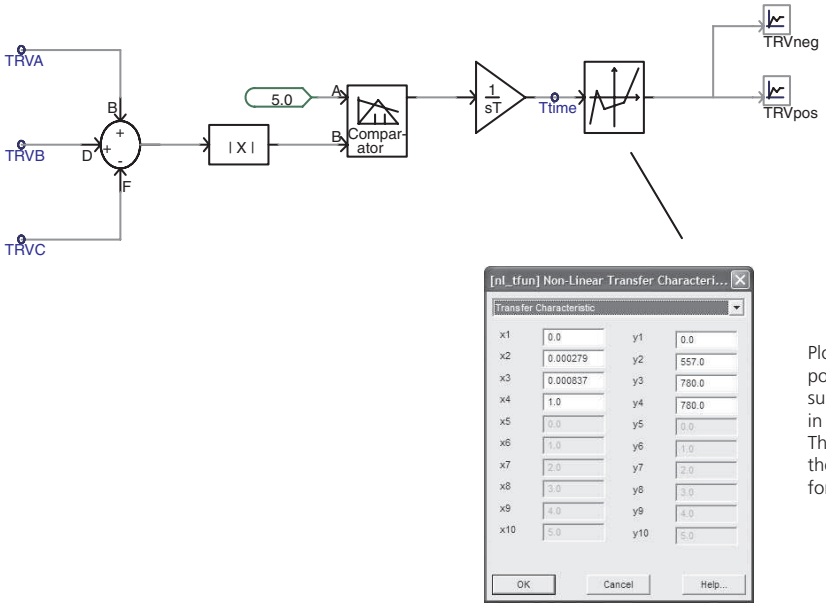
First-pole-to-clear factor = 1.3 or 1.3/1.5



TRV under 100 kV in IEC 60056 (1987-03)

U kV	u_c kV	t_3 µsec	t_d µsec	u_c / t_3
3.6	6.2	40	6	0.15
7.2	12.3	52	8	0.24
17.5	30	72	11	0.42
24	41	88	13	0.47
36	62	108	16	0.57
52	89	132	7	0.68
72.5	124	166	8	0.75

standard values for TRV shall be subject to agreement between manufacturer and user.



Plotting TRV limits. The TRV measurements from each pole of the circuit breaker (TRVA, TRVB and TRVC) are summed to trigger a timer (an Integrator whose output is in seconds) when the circuit breaker commences to open. The Non-linear Transfer Characteristic component defines the TRV limits and can be plotted with the measured TRV for comparison.

REFERENCES

1. D.A. Woodford, L.M. Wedepohl, "*Impact of Circuit Breaker Pre-Strike on Transmission Line Energization Transients*," IPST'97, International Conference on Power Systems Transients, Seattle, June 22-26, 1997, pp250-253.

2. "*Modeling and Analysis of System Transients Using Digital Programs*," IEEE Publication No. TP-133-0, 1998, Section 4, Switching Transients.

EXERCISE

2.1 Load Lesson2_1 in Section2. This is the transmission line case studied in Lesson3_1 but with the circuit breakers added to energize the transmission line. The user defined component for circuit breaker pre-strike is included. Run the case and see if it operates correctly. Replace the slider defining the delay before the contacts commence closing [TD] with a multiple run component. Set it up to initiate random closing over a one cycle period. Set the case to run with 20 or more multiple runs and search for the maximum line end voltage. Repeat the case with one phase at the open end solidly grounded and search for the maximum line end overvoltage.

To load Lesson2_1, if you are changing the directory to run the case, you must transfer both the case file Example2_1.psc as well as the FORTRAN file for the Circuit Breaker Prestrike component Swlib.f into the new directory.

If the case does not run because the component is not in place correctly, see the course teacher or contact the Centre at support@pscad.com .

Chapter 3:

Controls

Network analysis without controls analysis would be very limiting. Systems may consist of both, and each may be non-linear. For example, power electronic controllers, networks with saturating transformers, and protection systems require simulation methods of study with both advanced network and controls capability.

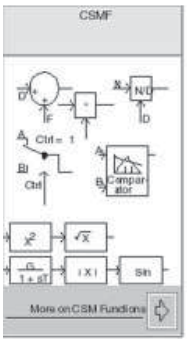
Continuous Systems Modelling Functions (CSMF) are assembled into the Master Library and provide basic linear and non-linear control components. It is recognized that not all functions are provided in the CSMF page in the Master Library. PSCAD/EMTDC provides the capability to construct user defined functions, but this is covered in a later section, and some guidelines to do this are presented in the PSCAD On-line Help. A simple way to create a user defined function as a page component is covered in section 5 of the PSCAD User's Guide, or in the PSCAD on-line help.

CSMF COMPONENTS

A number of basic examples are presented to illustrate some of the applications possible with CSMF. A system of CSMF components, whether simple or complex, can be linked to an electric network. Note that CSMF components can be used to simulate dynamic or logic systems without any electrical network.

Each CSMF component has On-Line Help available. When assembling a dynamic system from CSMF components, it can be formed as a block diagram using PSCAD. Any interface to a network is achieved with voltage and current transducers as inputs. Active power, reactive power, rms voltage and current measurements, phase angle, measured frequency and harmonic frequencies can all be used as inputs to a system comprising one or more CSMF components.

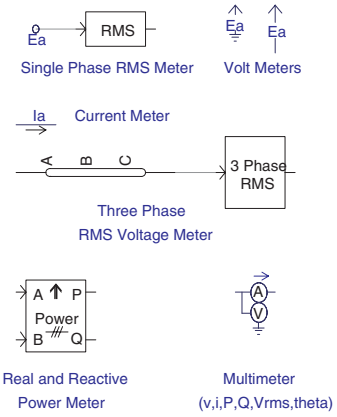
Output from CSMF components may be used to control voltage and current sources, switching signals or firing pulses for thyristors, GTOs or IGBTs. It is possible to dynamically control the value of resistors, inductors and capacitors. CSMF components can also be used for signal analysis and outputs from such may be directed to on-line plots or meters. It should be noted that interpolation compatibility is added to current CSMF components when applicable.



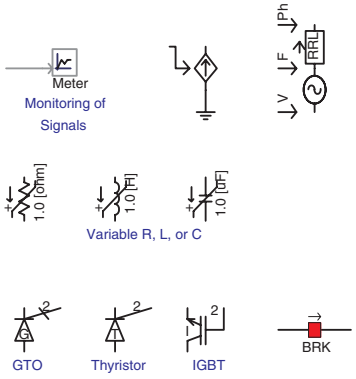
CSMF page in the Master Library.

When undertaking an important study, it is always best if verification of results can be achieved by some method other than simulation. Perhaps a mathematical modeling analysis can be applied by taking suitable approximations and linearizations.

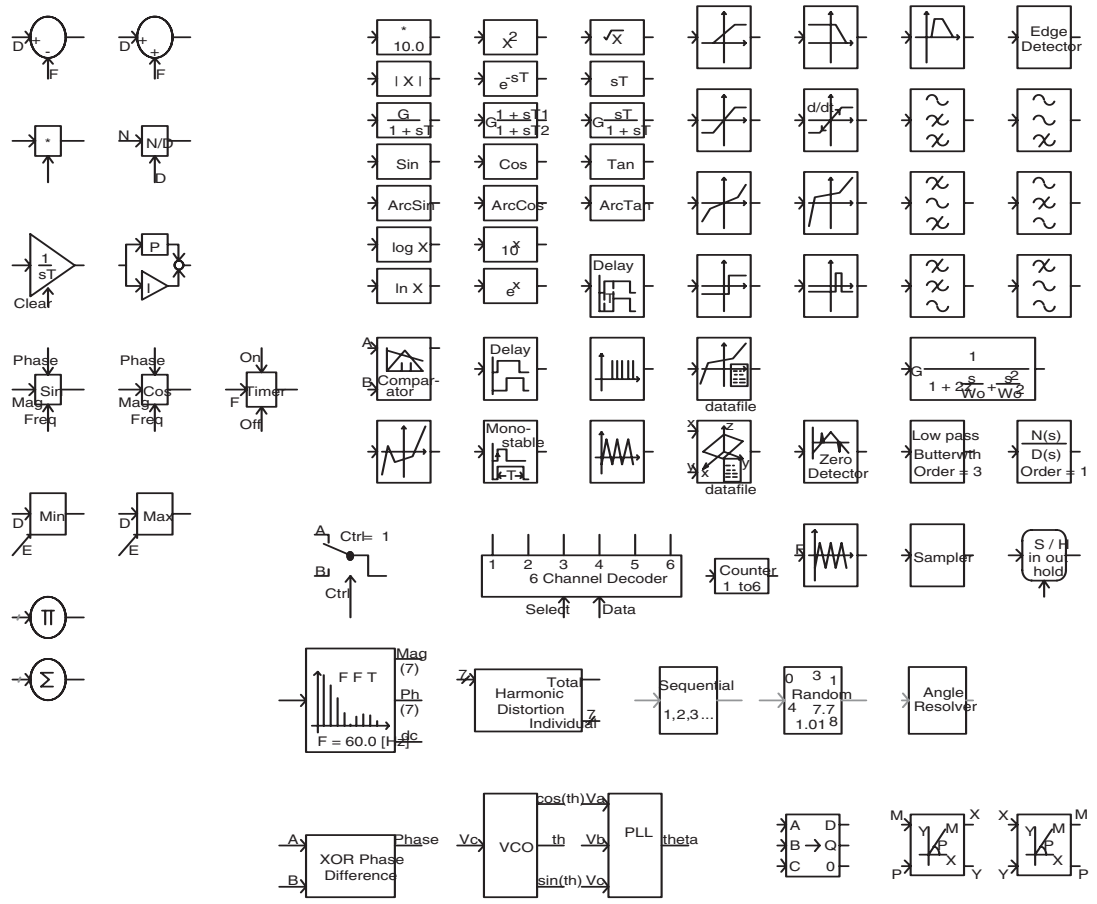
The simulation analysis can be as precise as the known data allows, but if non-linearities are present, an orderly study procedure involving trial and error methods with rigorous testing may be needed.



Interface components generating signals from the network as inputs to CSMF components.



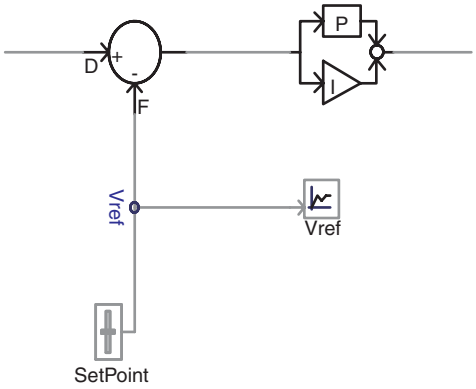
Network components which can receive output signals from CSMF components.



USE OF SLIDER, SWITCH, BUTTON AND DIAL

To cause parameters to be modified on-line by the user while a case is running or in pause mode requires application of the slider, switch, button or dial components.

For modification of parameters during a run, each must be accompanied by a control panel and be linked to it. They can be used as follows:

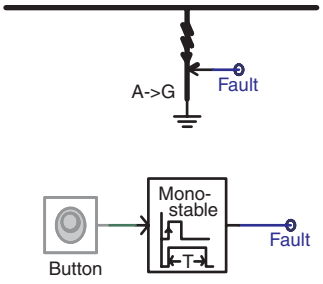


Use of a slider as a set point

The Slider is like a slide potentiometer and can adjust in steps of 0.01 of the maximum and minimum range. It is useful for set points in control systems, such as desired voltage in a voltage controller. It is also useful for gain changing, limit changing and new time constant values.

The Switch enables two states to be selected and is useful for turning a portion of the controls on or off, changing gains, initiating a switch, creating disturbances or forcing initial conditions on a controller during start-up before a snapshot is taken.

The Button can be used for initiating a sequence or disturbance, or forcing a reset.

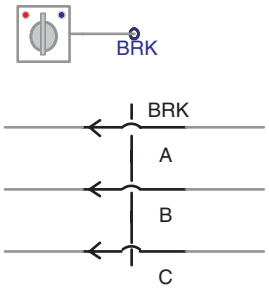


Use of a button to initiate a line fault

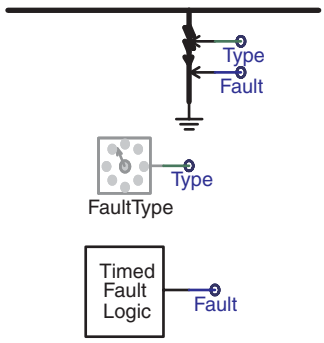
The Dial allows 3 to 10 user specified parameters to be selected based on position. When a study requires similar cases run with different disturbances, each can be pre-defined and selected by the dial before the case is run from the snapshot. For example, each dial position might represent a different magnitude of lightning current for a lightning insulation coordination study.

The procedure for linking the slider, switch, button or dial component to a control panel is as follows:

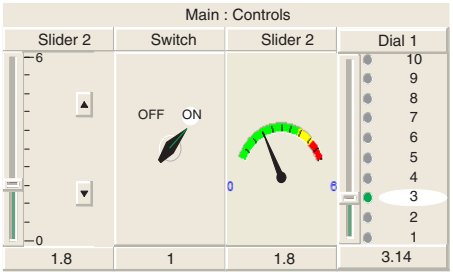
1. Place a control panel on the page where it will be obvious what it is being used for. There are two ways to place a control panel on the page. The first is to place the mouse cursor on a blank part of the page near where the control panel is to be located, hold down the right mouse button, select **Add a Control Panel**, lift right mouse button. The other way is to open up the Master Library and go to the I/O_Devices page and open it up. The control panel is copied and pasted on the project page. Note that if the control panel is copied from the Master Library, it may have sliders, meters etc., already pasted in it. These should be deleted before proceeding.
2. Now the actual slider, switch, button or dial components already located on your page must be linked to the control panel. Place the mouse cursor on the component, hold down the right mouse button, select **Input/Output Reference, Add as Control**. Lift right mouse button. Place mouse cursor on the top bar of the control panel, hold down right mouse button, select Paste, lift right mouse button. The controller for the component should appear on the control panel.
3. Place all slider, switch, button or dial components on this or other control panels. If a component is not linked to a control panel, it will function at the constant, uncontrolled level defined by its initial value setting.



Example use of a switch for breaker control



Use of a dial to change fault type



Control panel with components linked to it

A title for the control panel can be placed in the top bar. This is done by placing the cursor on the control panel top bar, hold down the right mouse button, select **Panel Properties**. A Control Panel Properties panel will open up which has provision for the title to be added or changed.

The order in which two or more sliders, switches, buttons or dials appear on the control panel can be changed. Place mouse cursor on the slider, switch, button or dial to be repositioned, select **Set Control Order** and one of **Move Left**, **Move Right**, **Left Most** or **Right Most**.

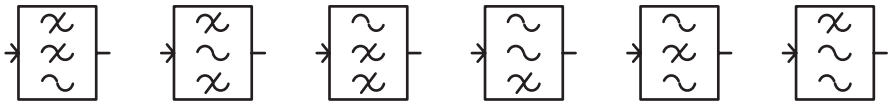
NOTE: a meter linked from an output channel can also be placed on a control panel. This is a similar process to linking the slider, switch, button or dial components to the control panel.

To link a meter to a control panel, place the mouse cursor on the desired output channel, hold down the right mouse button, select **Input/Output Reference, Add as Meter**, lift right mouse button. Place mouse cursor on top bar of control panel, hold down right mouse button, select **Paste**, lift right mouse button.

APPLICATIONS FOR CSMF COMPONENTS

Filtering with a Second Order Function

The first example considers use of a second order function as a filter. From the Master Library under the CSMF page, a selection of second order functions is available for use as filters. These are:



High, Mid, Low 2nd order filters from the CSMF library

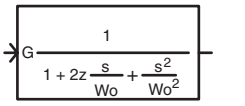
The On-Line Help available for the second order functions explains their Laplacian formulation. For this application, a low pass filter is explained. A low pass filter is the most useful filter as it serves to attenuate signal noise. Understanding the theory of filters enables the parameter selection for the second order components to be chosen wisely. The Laplacian formulation for a low pass second order filter is:

$$LP(s) = \frac{1}{1 + \frac{2\xi s}{\omega_0} + \frac{s^2}{\omega_0^2}}$$

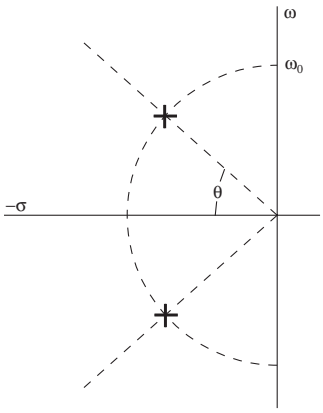
Where:

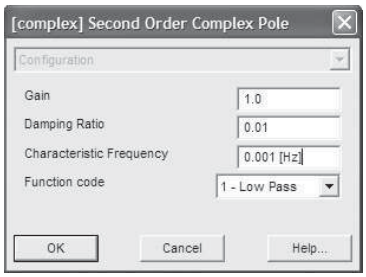
ξ = damping ratio = Cos(θ)
ω_0 = characteristic frequency (rad/sec)
s = Laplacian operator

Any frequencies greater than ω_0 will be attenuated providing the function is optimally damped with ξ selected at approximately 0.7 (θ = 45°).



This component is the same as the second order low pass filter.





Entering parameters of second order filter.

When entering the parameters for a second order filter component (place mouse cursor on the component, hold down the right button and select **Edit Parameters**, lift right button. Alternatively, place mouse cursor on the component and double click the left button), the characteristic frequency is entered in Hz rather than radians/second.

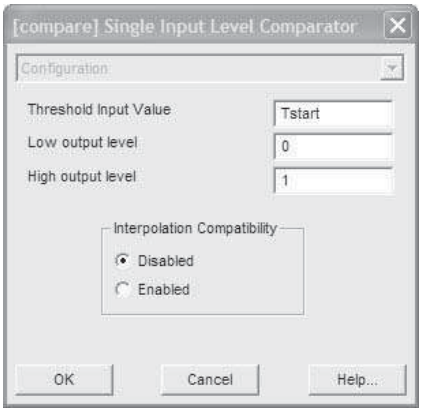
An example where second order filters can be used is in the voltage feedback signal to a voltage controller. The low pass filter can effectively inhibit high frequency noise and if specific frequencies are to be blocked, such as fundamental power frequency or 2nd harmonic, second order blocking filters can be applied. Blocking filters will in general be more effective if their damping factor is reduced to a small value. However, if it gets too close to 0.0, the filter will lose effectiveness by being too undamped.

Timer to Change a Parameter

A useful function in the CSMF library is the Single Input Level Comparator. It is often used to cause an action during a case start-up sequence. For example, when running up a snapshot for

a power electronics case, the first requirement is to establish voltage, then to deblock the firing pulses to the thyristors, GTOs, etc.

The input signal can be TIME from the Time component. When TIME exceeds the level set in the Single Input Level Comparator, its output will change state causing the necessary action.



Dialogue box for Single Level Input Comparator showing settings.

Controlling an AC Source

The Source library within the Master Library contains a number of single and three phase voltage sources. The voltage sources can be self-regulating if that option is chosen.

The sources can also be externally regulated. The obvious way is to control the phase, frequency or magnitude of the voltage source with sliders. One other option is to use a control circuit to regulate the controllable parameters. A simple example is to cause a simple three-phase source to have the characteristics of a synchronous generator with electromechanical phase oscillating properties of a "classical machine model."

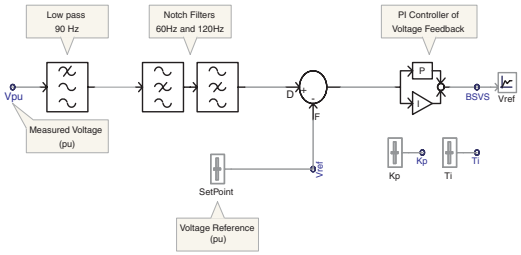
This is simply accomplished by ensuring the three-phase source used is controlled "externally." Power is measured at the terminals of the source, and after comparing the measured value of power with the desired level, it is integrated twice.

The output of the first integrator approximates incremental rotor speed in radians per second. The output of the second integrator produces rotor (source) phase angle in radians that is fed into the source model.

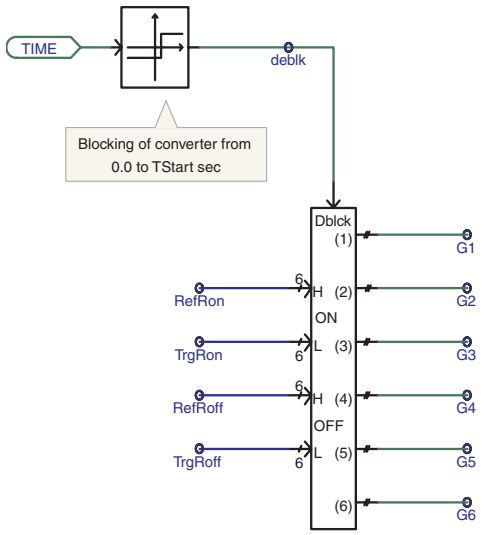
The time constant required for the first integrator is:

$$z = \frac{2 \cdot H \cdot MVa}{2\pi f}$$

Where:

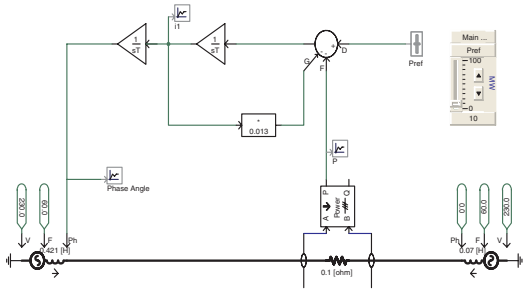


The above figure is a voltage feedback signal for an SVC voltage frequency controller. The first filter is a low pass, the other two filters are blocking any fundamental frequency or second harmonic component of the measured voltage.



Here a slider is used to set a value for the "Tstart" signal. When it's exceeded by TIME, the output of the Single Input Level Comparator changes from 0 to 1, thus deblocking the firing pulses.

A self-regulating voltage source will attempt to maintain the rms value of its terminal voltage constant according to a specified time constant, and/or control the power flow from its terminals without any external controller.



Example of creating a simple classical synchronous generator model from an externally controlled three-phase source. Note that the feedback around the first integrator is for damping.

H = Inertia (MW-Sec/MVA)
MVA = Machine rating (MVA)
f = System Frequency (Hz)

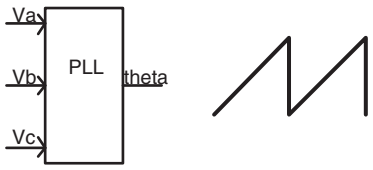
The time constant for the second integrator is 1.0

A damping constant must be included as feedback around the first integrator. This is adjusted to whatever damping of mechanical swings is desired.If left out, the electromechanical damping will be negative because of the inherent lag in the power calculation.

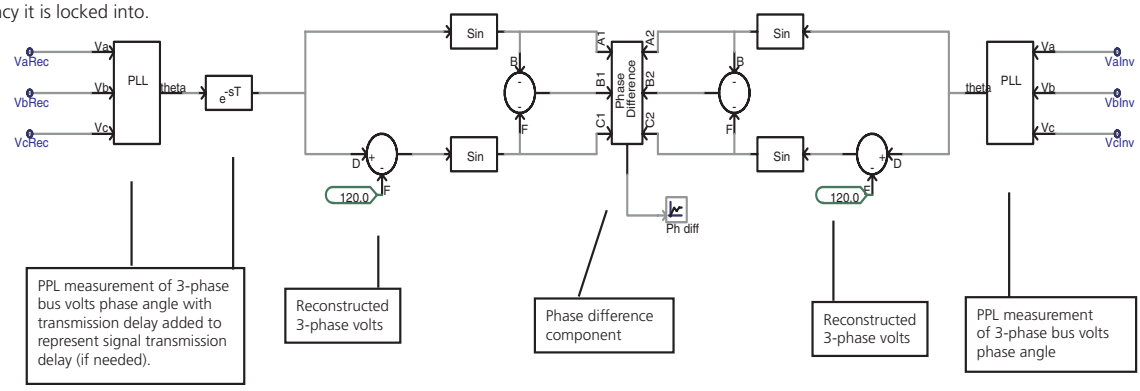
Measuring Relative Phase Angle

If there is ever a need to measure phase angle between two three-phase busbars, the Phase Difference component located in the Meters library of the Master Library can be used. However, with unbalance and harmonic distortion in the phase voltages, the measured phase angle will be very noisy.

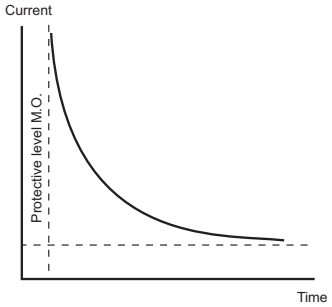
For the case where voltage distortion and phase unbalance exists, then one procedure to generate voltage phase angle between two three-phase busbars is based on the Phase-Locked Loop (PLL) component found in the CSMF library. This component has superior measurement capabilities in synchronizing to a three-phase voltage with significant distortion. Therefore, the method of phase angle measurement simply consists of locating a Phase-Locked Loop component at each three-phase busbar, re-create a three-phase voltage from its output, which will be balanced and almost free of distortion, and then use the Phase Difference component to measure the resulting phase angle.



The output of the Phase-Locked Loop component is a ramp function climbing between 0 to 360 degrees once every cycle of the frequency it is locked into.



Measuring relative voltage phase angle between two three-phase bus bars

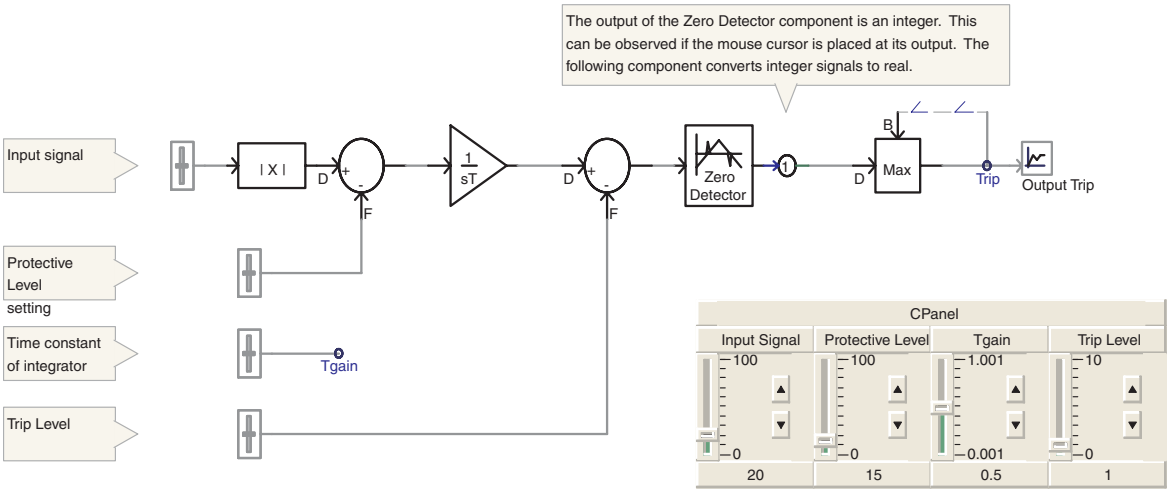


Building an Inverse Time Function

Components in the CSMF library can be applied to measurement, signal processing, protective and control functions. An inverse time function is useful in overcurrent relaying, or representing the protective action of a fuse.

The signal representing the quantity to be protected by the inverse time function (such as current) is processed through an integrator. The protective level is set by subtraction from the absolute value of the input signal. The speed of response is determined

by the value of the time constant of the integrator. Whenever the output of the integrator passes a specified level (say 1.0), it instigates the trip action of the inverse time function.



The minimum internal limit of the integrator is set to 0.0. This means that with the input signal less than the protective level, the output of the integrator will remain at zero. The output trip signal will go from 0 to 1 and lock at 1. A reset on the integrator component would need to be added if it is required during the run.

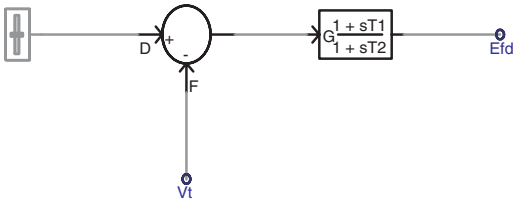
EXERCISES

3.1 A second order component configured as a low pass filter is used to filter a 5th harmonic from a signal containing a fundamental frequency component (50 Hz) and a 5th harmonic (250 Hz). Replace the 2nd order low pass filter with a low pass Butterworth filter. Experiment with the Butterworth filter to achieve best blocking of the 5th harmonic and allowing the fundamental frequency component of the input signal to pass.

3.2 Build a simple exciter for the classical machine model created from an externally controlled source as demonstrated above. The configuration of a simple solid state exciter is as shown. Enter parameters you might consider realistic and see if performance is stable.

3.3 Develop a 10 amp rms fuse with a protective level (minimum operating) of 15 amp rms. If the current should increase to 20 amps rms, it will open up at the first current zero after 0.1 seconds.

The Output Trip signal is locked up using the Maximum/ Minimum Function component as a "select maximum" with a feedback. A special one-time step delay component can be inserted at strategic locations in feedback control systems to force a desired sequence of processing. It is not needed in this instance but has been inserted as shown. It is found on the main page of the Master Library:



Simple exciter model for classical machine model for use in Exercise 3.2.

Chapter 4:

Surge Arresters

Metal oxide surge arresters (MOVs), when carefully chosen, provide a compromise between the protective levels, temporary overvoltage (TOV) and energy absorption capability. Selecting a higher rated surge arrester increases its TOV capacity and thus its ability to survive system voltage stresses, but reduces the margin of protection provided by the arrester for a given protective level. An arrester with a higher energy capability reduces the risk of failure but at increased costs.

Voltage considerations that need to be understood and evaluated when selecting an arrester include:

1. Continuous operating voltage (COV, MCOV or U_{ca}). By definition, this is "the designated permissible r.m.s. value of power frequency voltage that may be applied continuously between the arrester terminals." Since harmonics may be present, U_{ca} is taken as the system voltage crest divided by √2 or if the harmonics are not known, divide the system voltage (L_L) crest by √6 for normal phase to ground arresters. If the system voltage crest is not known, the highest voltage for equipment Um should be used instead. U_m is normally 5 – 10% above normal system voltage. U_c is always selected higher than U_{ca}.

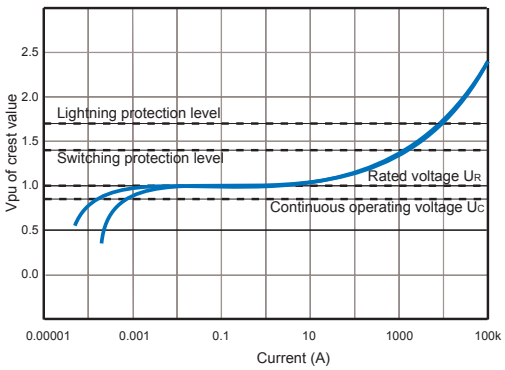
   If there are uncertainties in surge arrester and equipment expose use, there is good incentive for using PSCAD/EMTDC to determine these exposures for precise specification of equipment.

2. Temporary Overvoltages. All voltages higher than U_c are defined as TOV. TOV can be from a few cycles to several hours. From IEC 60099-1, a temporary overvoltage is: "An oscillatory phase-to-ground or phase-to-phase overvoltage at a given location of relatively long duration and which is undamped or only weakly damped. Temporary overvoltages usually originate from switching operations or faults (e.g. load rejection, single phase faults) and/or from non-linearities (ferroresonance effects, harmonics). They may be characterized by their amplitude, their oscillation frequencies, their total duration or their decrement."

   Different arresters may have the same U_c but different rated voltages to meet different overvoltage requirements.

3. Fast front transients. The primary cause of fast front transients is lightning strikes to transmission lines and the associated back flashovers. Fast front transient overvoltages are limited to a higher level than from TOVs generated from switching surges. To reflect this property

Voltage in p.u. of rated voltage (crest value)



Typical voltage - current characteristics of MOV

Definitions

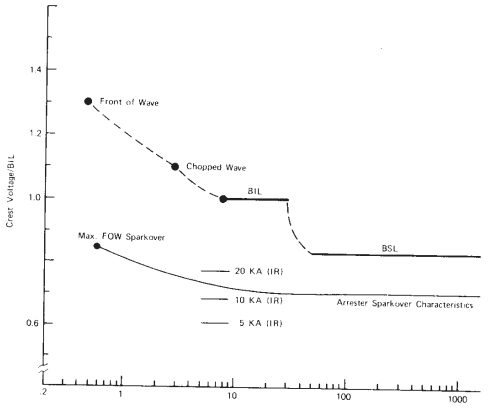
Rated Arrester Voltage U_r. The rated voltage is the highest r.m.s. power frequency voltage that is applied to the arrester in the operating duty test for 10 s after being pre-heated and subjected to an energy injection in accordance with clause 2.8 of IEC 60099-4. The TOV capability of the arrester for 10 s has therefore to be minimum with reference to rated voltage U_r. Often the real capability is higher.

Nominal Discharge Current I_n. The peak value of current of an 8/20 ¼sec impulse used to classify an arrester.

For systems with U_m 52 kV, I_n = 5–10 kA.
For systems with U_m 300 kV, I_n = 10 kA.
For systems with U_m > 300 kV, I_n = 10–20 kA.

The associated arrester discharge voltage U_n is sometimes used. For example, U_{10} is the arrester discharge voltage for I_{10} (10 kA).

Crest voltage (p.u. of BIL)



Insulation coordination of transformer

More Insulation Coordination Definitions:

Protective Margin $P_M = (V_W - V_P)/V_P$

Where:
V_W = Withstand capability of the power components under protection.

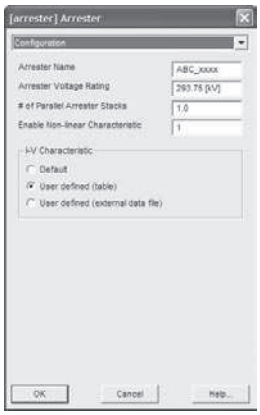
V_P = Protective level (at the selected current discharge level through the surge arrester).

BSL – (Basic switching impulse insulation level) is the crest value of a standard switching impulse that the insulation can withstand. Eg, 250 x 2500 µs.

BIL – (Basic lightning impulse insulation level) is the crest value of a standard 1.2 x 50 µs impulse that the insulation can withstand.

Chopped Wave – (Chopped wave withstand) is the crest value of a standard 1.2 x 50 µs impulse "chopped" by action of a rod gap placed in parallel with the insulation after a specified time (2 µs for HV breakers, 3 µs for HV transformers and reactors).

Surge arrester component as found in the Main Library



The user defined I-V Characteristic shown entered here reflects the 20°C characteristic shown on page 5-1. Note that the p.u. values entered for the Y-axis are "2 times greater to reflect the crest value of rated voltage.

Note: if Arrester Voltage Rating is entered in kV, r.m.s., then the X-axis currents should be entered in kA.

For arresters of similar class and type, the I-V Characteristic entered is directly scaleable by the Arrester Voltage Rating.

into the arrester, simulation requires important modeling considerations.

Insulation design for distribution arresters is based largely on fast front transients. Higher voltage arrester applications may be significantly influenced by TOVs from switching transients.

ARRESTER MODEL

The switching surge arrester model available in the Master Library is modeled as a piece-wise-linear resistance whose volt-amp characteristic is entered by the user (or a default characteristic can be applied). It is suitable for designing switching surge TOV protection. It can also be developed for fast front transients, as would be discussed in a later section.

Switching Surge TOV

The network model for application of the surge arrester is developed. For high voltage applications above 220 kV, the switching surge TOV should be taken into account.

Equipment suppliers can be contacted for the characteristics of the latest range of surge arresters available. Care has to be taken in interpreting their data. One supplier may define their per unit characteristic such that 1.0 p.u. is the crest value of rated voltage U_r as shown above. Another supplier may define their per unit characteristic such that 1.0 p.u. is the crest value of continuous operating voltage U_c.

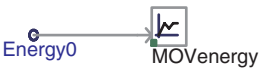
The component Configuration is first entered. The Arrester Name should reflect the supplier and model name of the arrester being represented so that it is easy to identify. There is a default **I-V Characteristic** available but it is best if the actual arrester characteristic is entered by selecting "User." There is also the feature of adding identical arrester stacks in parallel. This is useful when energy capability is being selected. If two or more stacks are selected for "**# of Parallel Arrester Stacks**," then the discharge current is increased proportionally and hence its energy absorption capability. Sometimes it is useful to effectively take the arrester out of service. The "**Enable Non-linear Characteristic**" entry when changed to "**0**" from "**1**" will leave the arrester in the model but inactive.

The volt-amp characteristic for the Surge Arrester Component is entered in per unit for voltage for the vertical [Y] axis and kA for the horizontal [X] axis under "I-V Characteristic." Some points to consider in entering an I-V Characteristic:

- The points X1,Y1 should not be entered as (0.0,0.0). This will cause it to use the default characteristic.
- Enter all 11 sets of points with the X-axis representing current for a single arrester/stack.

- Enter the Y-axis representing crest voltage in per-unit of the arrester rating (which is usually an rms value). Care must be exercised here to correctly interpret the supplier's published data as mentioned above.

Output for arrester absorbed energy and current is entered as "**Internal Output Variables**" by designating appropriate signal names. Energy is in kJoules and current in kA if the arrester is operating under conditions of kV and kA. Often, absorbed energy is desired in kJoules/kV based on the "**Arrester Voltage Rating**." If the arrester rating is 192 kV, this is achieved through scaling the output component by 1.0/192.



Scaled by 1/192 for kloules/kV

Note: The PSCAD model (V4.2.1) does not account for the energy dissipation to the surrounding medium during its normal steady state operation nor during transient events.

The value entered for "Arrester Voltage Rating" under "Configuration" directly scales the per unit voltage accordingly. So for this switching example, if the impact of a 228 kV rating of a similar arrester is to be investigated, change the 192 kV rating previously entered to 228 kV and re-run the case.

Typical specific single impulse energy absorption capabilities of various classes of surge arresters in kJ/kV based on rating U_r : 2.5, 4.5, 7.0, 10.0, 13.0

Fast Front Transients

When fast front transients, such as from lightning, are to be investigated, the MOV surge arrester (behavior) representation is significantly different. The voltage across the arrester increases as the time to crest of the arrester current decreases and the arrester voltage reaches its peak before the arrester current reaches its peak.

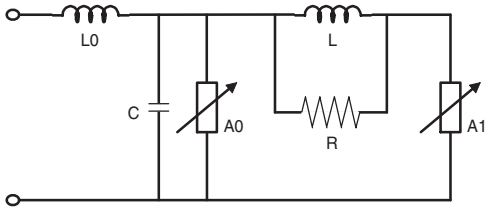
The time to crest for lightning surges can range from 0.5 sec to several sec. The frequency dependent model proposed will give good results for current surges with time to crest from 0.5 sec to 40 sec.

Dan Durback of PTI first proposed the fast front model in a presentation to the IEEE Surge Protective Devices Committee WG 3.4.11 on Surge Arrester Modeling Techniques, September 29, 1983 at a meeting of the Working Group in Memphis, Tennessee.

The model was refined and presented in a paper by the IEEE Working Group 3.4.11, "*Modeling of Metal Oxide Surge Arresters*," IEEE Transactions of Power Delivery, Vol. 7, No. 1, January 1992, pp 302-309 and is now adopted into IEEE Standard C62.22-1997, Annex G.

For the fast front model, there are two sections of non-linear resistance designated A0 and A1; each comprised of the surge arrester model used for switching surge transients above. The two sections are separated by an R-L filter. For slow front surges, this R-L filter has very little impedance, but is significant for fast front surges.

Characteristic A0 has a higher voltage for a given current than A1, but when the two are considered in parallel when the R-L filter is not acting significantly, their combined characteristic is that for slow front (switching surges).



Fast Front surge arrester model

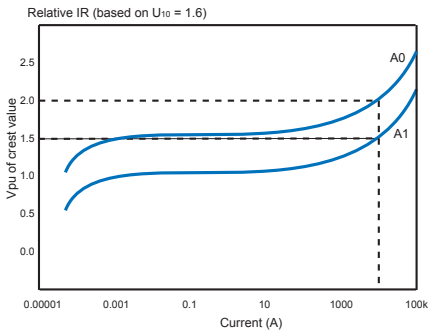
The RLC elements are initially determined by the following formulae:

L1 = 15d/n microhenries
R1 = 65d/n ohms

Where:

d = is the estimated height of the arrester in metres (use the overall dimension from the catalog data).
n = number of parallel columns of metal oxide in the arrester.

Lead inductance is usually estimated at 1.0 microhenries per metre.

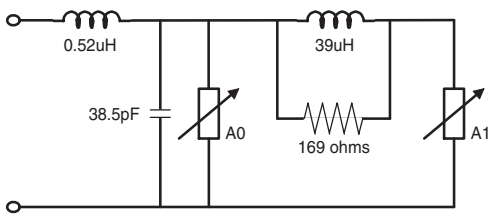


V-I relationships for non-linear resistor part of model based on a characteristic where U_{10} = 1.6

Voltage-current relationships for the two non-linear sections of the fast front arreter model.

I-V Characteristic for A0

I-V Characteristic for A1



Initial Fast Front Arrester

The inductance L0 represents the inductance from the magnetic fields in the immediate vicinity of the arrester. The capacitance C represents the terminal-to-terminal capacitance of the arrester.

L0 = 0.2d/n microhenries
C = 100n/d picofarads

Any lead inductance or stray capacitance is extra. This would apply particularly to L0 where the lead inductance to the arrester must be added. When it is known that arrester discharge will not occur, just the representation of L0 and C is adequate (blocks A0 and A1 are not needed).

The individual characteristics of each non-linear section A0 and A1 are determined from Figure 2 in [3] which is reproduced here.

The best way to model A0 and A1 for scaling is to enter each characteristic into the "I-V Characteristic" of two separate Surge Arrester Components.

The fast front models are based on a surge arrester having its 10 kA discharge voltage (U10) at 1.6 per unit (crest value). The correct scaling is achieved by replacing the "Arrester Voltage Rating" under "Configuration" with the following factor for both A0 and A1:

Arrester Voltage Rating = U_{10}/1.6

Where U_{10} is 10 kA discharge voltage in kV for the actual arrester under consideration.

For example, if the discharge voltage U10 is 470.0 kV for the arrester rated at 192 kV, then in both fast front arrester sections A0 and A1 under "Arrester Voltage Rating" enter 470/1.6 = 293.75 [kV] instead of 192. This must only be done provided that the "I-V Characteristics" for both A0 and A1 are entered as indicated.

Determining Fast Front Model Parameters

In addition to knowing the arrester length "d" and the number of metal oxide stacks "n," also required is the U10 discharge voltage in kV for the standard 8/20 µsec nominal discharge current impulse and the switching surge discharge voltage for an associated switching surge current impulse.

Consider a one column surge arrester rated at 192 kV with an overall length of d = 2.6 metre. The U_{10} discharge voltage for this arrester is 470 kV and the switching surge discharge voltage U_{ss} for a 3 kA, 300/1000 µsec switching surge current impulse is 403.9 kV. The fast front model parameters are determined through the following steps:

Step 1: Determine the initial parameters for L0, C, L1 and R1 when d = 2.6 metres and n = 1.

L0 = 0.2d/n = 0.52 µH

C = 100n/d = 38.5 pF
L1 = 15d/n = 39.0 µH
R1 = 65d/n = 169 ohm

Step 2: Evaluate the scaling factor U_{10}/1.6 to apply to the surge arrester component for both sections A0 and A1 under "Arrester Voltage Rating."

U_{10}/1.6 = 470/1.6 = 293.75 kV

Step 3: Ensure the relative IR "I-V Characteristic" for both A0 and A1 sections are entered into the surge arrester component.

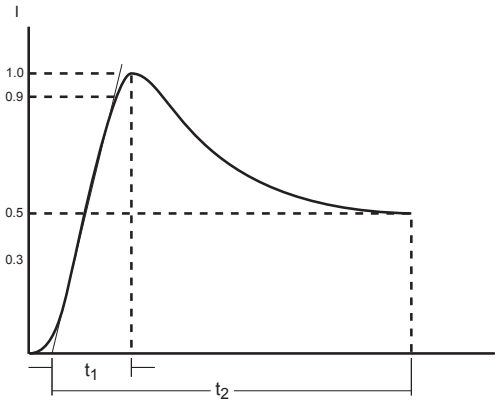
Step 4: Adjustment of the U_{10}/1.6 scaling factor for the A1 non-linear resistance section to match the switching surge discharge voltage. This is done by trial and error until there is a good match between the manufacturer's switching surge discharge voltage U_{ss} and current and the model test results.

The current injected into the surge arrester should be the same magnitude and waveshape as the current used by the manufacturer to determine the switching surge discharge voltage. Inject the switching surge test current and examine the resulting peak voltage.

In order to undertake this step, a surge test is done on PSCAD. The current impulse I_{TEST} is approximated by two exponential functions:

$$I_{TEST} = I(e^{-at} - e^{-bt})$$

The values of I, a and b of the above equation may be determined for the impulse wave if the crest value I_1 and the time to crest t_1 and time to half settle on the tail t_2 are known. This relationship is approximated through use of curves.

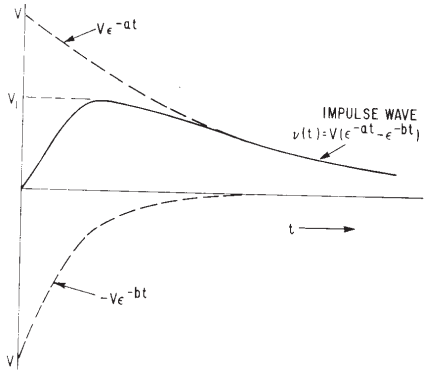


Impulse wave specification

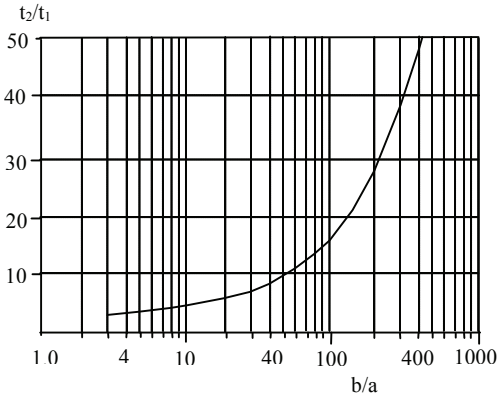
Consider synthesizing an 8/20 µsec impulse. t_2/t_1 = 2.5. This is outside the range of the charts. From a mathematic assessment,

X-axis current [kA]	A0 Y-axis volts [p.u.]	A1 Y-axis volts [p.u.]
1.0E-7	1.1	0.72
1.0E-6	1.28	1.0
1.0E-5	1.33	1.08
1.0E-4	1.37	1.11
0.001	1.39	1.15
0.01	1.42	1.18
0.1	1.52	1.22
1.0	1.65	1.32
3.816	1.75	1.40
10.0	1.9	1.55
100.0	3.8	1.95

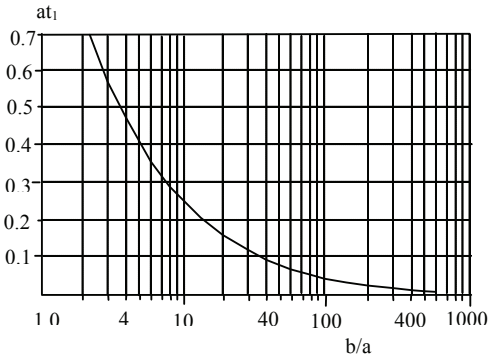
I-V Characteristic for both A0 and A1 sections for entry in the surge arrester components based on U_{10} = 1.6 per unit. These characteristics can be used initially for all ratings of MOV surge arresters.



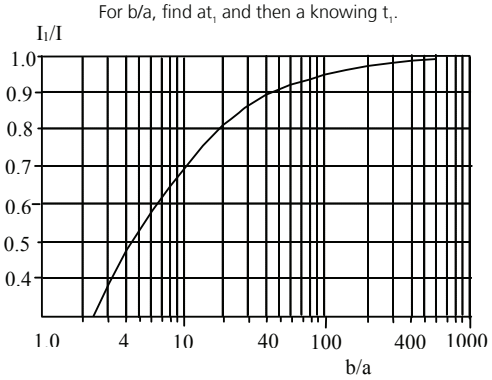
Impulse wave shape expressed as sum of two exponential functions.



Determining parameters for impulse wave expressed by $I_{TEST} = I(e^{-at} - e^{-bt})$. For known t_1 and t_2, find b/a.



For b/a, find at_1 and then a knowing t_1.



For b/a, find I_1/I and then determine I knowing crest surge current I_1.

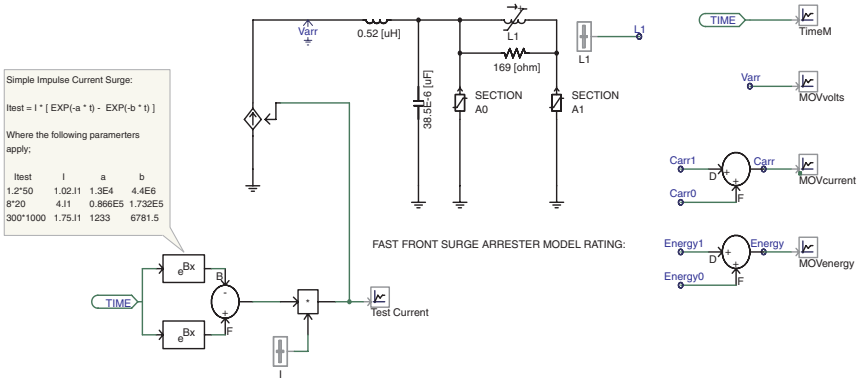
b/a ≈2, at_1 ≈0.7 and I_1/I ≈0.25. The current impulse for the 8/20 µsec test is:

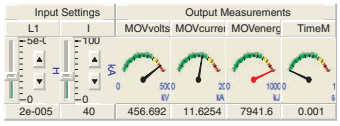
$$I_{8/20} \approx 4I_1(e^{-0.866E5t} - e^{-1.732E5t})$$

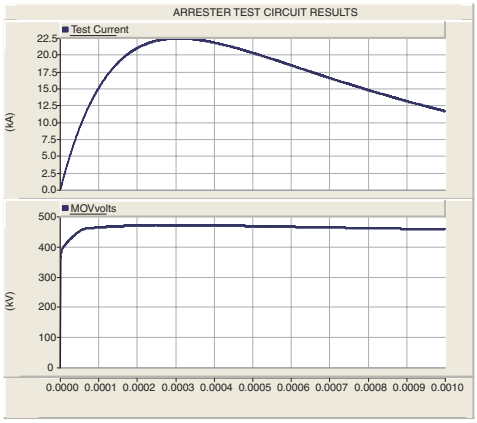
The switching discharge test current for this example is a 300/1000 µsec impulse which can be determined from the charts. t_2/t_1 = 3.33. From the chart, b/a ≈5.5. at_1 ≈ 0.37 and I_1/I ≈ 0.57. With t_1 = 300 µsec, a = 0.37/300E-6 = 1233. b = 5.5a = 6781.5. The current impulse for the 300/1000 µsec switching discharge test is:

$$I_{300/1000} = 1.75I_1(e^{-1233.0t} - e^{-6781.5t})$$

This designated current impulse for the switching surge discharge is injected into the arrester model with the initial parameters for a match with the switching surge discharge voltage U_{ss} of 403.9 kV. The resulting peak voltage is examined, and minor adjustments are made to the U_{10}/1.6 scaling factor for the A1 non-linear resistance section to provide a close match. For this example, negligible adjustment is required.







The test circuit on PSCAD/EMTDC for the fast front surge arrester model shows the 300/1000 µsec switching surge impulse current is injected and the arrester discharge volts observed to be 403.947 kV (403.9 kV is desired).

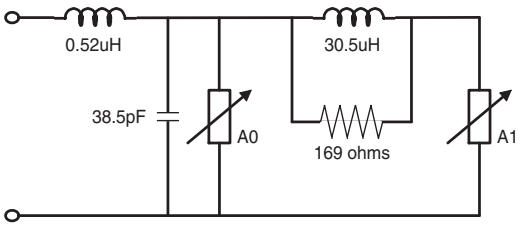
Note: Filter inductance L1 is variable through a slider. In this case it is set at the initial value of 3.9e-05 H.

For this example with the 8/20µsec impulse test current, the value of L1 was adjusted by trial and error. L1 = 3.05E-5 H was selected as follows:

L [H]	U10 [kV]
3.9E-5	482
3.0E-5	469.2
3.05E-5	469.95 (470 is desired)

Step 5: The arrester model now has correct non-linear resistances for the A0 and A1 sections for switching surges. It is now tested to obtain a good match for the discharge voltage with the 8/20 µsec injected current. The filter inductance L1 in the model is adjusted until the test produces a good match with the manufacturer's U_{10} discharge voltage.

Step 6: As an optional final check, Step 5 could be repeated with the standard 1.2/50 µsec lightning impulse test. This result can be compared with any information provided by the supplier to increase confidence in the precision of the fast front arrester model.



Final fast front arrester model

FAST FRONT STUDIES

A good reference on this subject is a report prepared by the Fast Front Transients Task Force of the IEEE Modeling and Analysis of System Transients Working Group [4]. Selection of calculation time step is an important consideration in fast front overvoltage studies. One concern is the physical length of conductors, leads, busbars and bus ducts that compose the network under study. Waves travel at near the speed of light at 0.3 metres per nano-second. In other words, a wave will propagate 3 metres along a lead in 10 nano-seconds. Consequently, lightning studies involving transmission and outdoor stations may be undertaken with calculation time steps of 5 to 20 nanoseconds for 50 to 100 µseconds. A good rule of thumb is to use a calculation time step of one half the propagation time along the shortest of the main conductors under study. The calculation time step for gas insulated substations (GIS) might be 0.1 to 1 nano-second and the computation might be for 1 or 2 µseconds.

Modeling Transmission Lines and Buswork

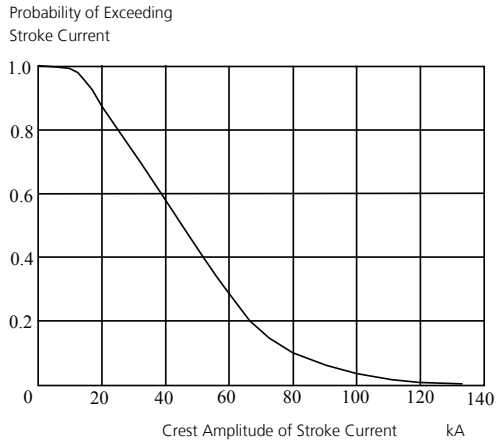
Overhead lines and busbars in the main surge propagation path should be modeled with frequency dependent transmission lines even if the length is only a few metres. If the overhead line is outside a substation, the normal known ground resistivity should be entered into the **Edit Parameters** field of the Tline interface component. If the overhead line or buswork is above a grounding mat in a substation, a nominal low ground resistivity should be entered (say 1 to 10 ohm-metre). Shorter sections can be modeled with the Coupled Pi Section component. Short leads are modeled as a lumped inductance of approximately 1 µH/m.

GIS bus ducting is best modeled with a coaxial cable distributed cable model. The Underground Coaxial Cable Constants Interface (see Cables page in the Master Library) can be used with **C1-I1-C2** configuration selected. Enter a very large resistivity value (1E6 ohm-metre) for the ground model to reflect the duct's positioning in air. However, grounding straps to the outer conductor are important to represent as either lumped inductance if the strap's length is less than the propagation distance of one calculation time step, or by a single conductor Bergeron distributed line model, if longer. Modeling grounding grids for GIS is an

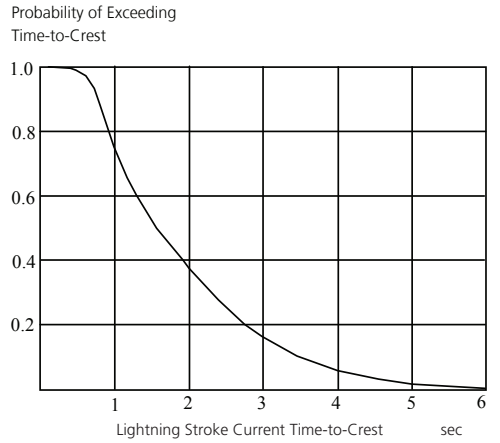
Representing the ground strap to GIS ducting as a single conductor Bergeron distributed line model can use the following calculation for surge impedance:

$$Z_0 = 60 \ln (2\sqrt{2}\, h/r)$$

Where h is the average height of the conductor and r is the equivalent strap radius. Use speed of light to determine the propagation time.



Probability of distribution of lightning stroke current amplitudes based on combined field data [5].



Probability of distribution of lightning stroke front times based on combined field data [5].

Transmission tower surge impedances:

For a vertical cylindrical conductor

$Z_o = 132.8 \log_{10}(2h/d) + 45\ d/h - 60$ (ohms)

Where:

h = vertical length (m)
d = diameter of conductor (m)

For a horizontal cylindrical conductor, the high frequency surge impedance is approximated:

$Z_o = (377/2p)*\ln(2h/r)$ (ohms)

Where:

h = height of conductor above ground (m)
r = radius of conductor (m)

inexact science at this stage. Simplified modeling represents the GIS grounding grid as a low value constant resistor.

Lightning

The magnitude of a current impulse due to a lightning discharge is a probability function. Low discharge levels between 5 to 20 kA may result in a higher tendency for the lightning strike to pass by any shield wires and directly hit a phase conductor. The larger lightning impulse currents may tend to strike the tower top and lead to a back flashover. This requires that the tower be modeled as a vertical distributed transmission line. The surge impedance of the tower and the propagation velocity down the tower are estimated and applied in a Bergeron distributed line model.

In deciding the amplitude of lightning stroke currents to apply to a transmission tower or conductor, probability of distribution of the crest values and front times can be considered. Knowing the nature of lightning surge impact on system components is important. This is particularly so considering back flashovers on towers and severity on the surge arrester and their discharge duties and protective levels.

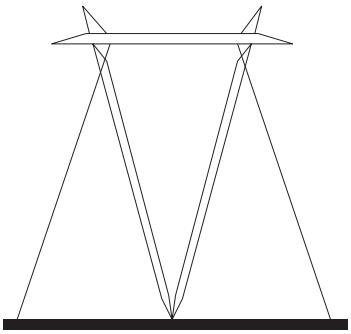
A lightning strike of 40,000 amps peak direct to a phase conductor on a transmission line entering a substation is considered a severe condition. Transmission shielding failures tend to occur for low current levels in the lightning strike, in the range 10,000 amps to 20,000 amps. In addition, over half the lightning strikes contain more than one strike. The mean number of strikes per lightning flash is three, typically separated by 20 to 50 milliseconds of time. The current in the strikes can vary and subsequent strikes may have higher or lower current than the first strike.

The time between strikes is sufficiently long that the fast front transient effects will have dissipated before the next strike arrives, but the energy in the surge arresters will not have reduced, and will add with each strike. Consequently, a worst case for study purposes is to consider a transmission shielding failure at the substation entrance, with five direct strikes to a line phase conductor of 25,000 amps per strike. The arrester energy for one such strike is multiplied five times to determine its total energy absorption requirement due to lightning.

A second study consideration is to have a lightning strike to a tower top at the station entrance that causes a back flashover. In this case, a severe condition is 150,000 amps. To accommodate multiple strikes, five strikes of around 80,000 amps each may be a worst case condition. If an 80,000 amp lightning strike to the tower or shield wire causes a back-flashover, then the sum of arrester energies is an estimate of the total energy absorption requirement for the station arresters. Ensure that for such a study, all arresters in the station are represented, at least for the phase effected by the lightning.

Transmission Towers

Transmission towers should be modeled as a vertical, single conductor Bergeron distributed line model. The surge impedance of the transmission line tower or pole and the travel time of wave propagation down the tower are required.

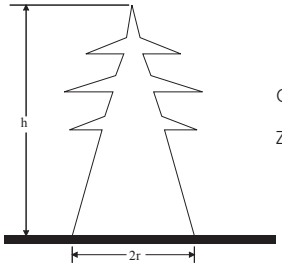


Experimental studies have shown tower surge impedance reduces from 300-400 ohms at the shield wire to less than 100 ohms near the base [6]. Tower crossarms are open circuit stub transmission lines extending propagation time down the tower. If a back flashover is to be simulated, the associated crossarm can be modeled as a Bergeron line with a representative surge impedance applied. Published values for average surge impedance for various tower structures are presented.

Wave propagation velocity down a smooth conductor, such as a grounding wire or tubular steel structure, is close to the speed of light. Lattice structures impede the velocity of propagation and along with the crossarm effects, effective wave propagation velocity may be 80% to 85% the speed of light.

Tower Footing Resistance

The tower footing resistance for fast front surges is not well understood. An R,L,C equivalent circuit [4] can be used for known counterpoise grounding configurations extending beyond 30 metres from the tower base. Within 30 metres of the tower base, a variable grounding resistance approximation can be applied which is surge current dependent.



Conical Tower:

$Z_o = 30 \ln [2(h^2 + r^2)/r^2]$ (ohms)

$$R_T = \frac{R_g}{\sqrt{1 + \frac{I}{I_g}}}$$

Where:

R_T = Tower footing resistance (ohm)

R_g = Tower footing resistance at low current and low frequency (ohm)

I = Surge current into ground (kA)

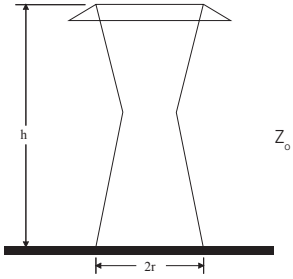
I_g = Limiting current initiating soil ionization (kA)

$I_g = \frac{1}{2} \bullet \frac{E_o \rho}{R_g}$ (kA if E_o is in kV/m)

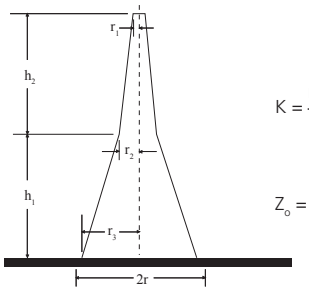
Where:

ρ = Soil resistivity (ohm-metre)

E_o = Soil ionization gradient (about 300 kV/m)



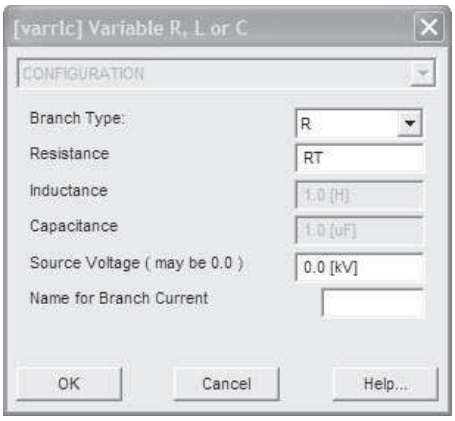
$Z_o = 60 [\ln (2\sqrt{2}h/r) - 1]$



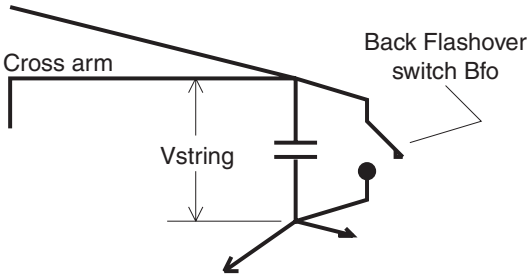
$$K = \frac{r_1 h_2 + r_2(h_1+h_2) + r_3 h_1}{(h_1+h_2)^2}$$

$Z_o = 60 \ln \cot 0.5 \tan^{-1}(K)$

The variable resistance can be modeled in PSCAD/EMTDC with the variable resistor component. To restrict resistance changes occurring at every calculation time step, use can be made of the



Modeling variable tower footing resistance with variable resistance component and sampler component. Sampler frequency = 10^7 Hz. I_g = 47 kA so that $1.0/I_g$ = 0.021. Low frequency footing resistance = 10 ohm.



sampling component in the CSMF page of the Master Library with internal frequency triggering.

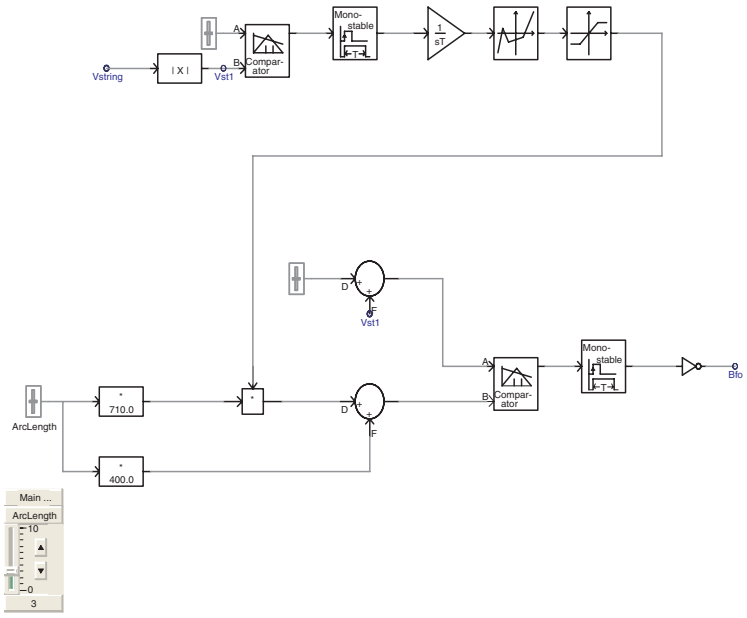
Capacitances of Equipment

Stray and winding capacitances have an impact on fast front surge propagation and should be modeled wherever possible. If values are not known, the following can be used as very rough approximations [4]:

Equipment	Capacitance-to-Ground		
	115 kV	400 kV	765 kV
Disconnector Switch	100 pF	200 pF	160 pF
Circuit Breaker (Dead Tank)	100 pF	150 pF	600 pF
Bus Support Insulator	80 pF	120 pF	150 pF
Capacitive Potential Transformer	8000 pF	5000 pF	4000 pF
Magnetic Potential Transformer	500 pF	550 pF	600 pF
Current Transformer	250 pF	680 pF	800 pF
Auto Transformer	3500 pF	2700 pF	5000 pF
Suspension Insulators (per unit)	10 pF	10 pF	10 pF
Pin Insulators (per unit)	100 pF	-	-

Back Flashover

Line insulators from tower to conductor can be represented as a capacitor if their capacitance is known. Where a back flashover might occur, a parallel switch is applied. If the voltage across the insulator exceeds the insulator voltage withstand capability, the back flashover occurs and is simulated by closing the parallel switch. The arc can form in around 20 nanoseconds and in most studies a detailed arc model is not required as the switch will suffice.



Breakdown of air as an insulator is very much a function of environmental conditions in addition to the fast front voltage build up. A very simplified expression for the insulator voltage withstand capability is proposed [7]:

$$V_{fo} = K_1 + K_2/t^{0.75}$$

Where:

V_{fo} = Flashover voltage (kV)
K_1 = 400L
K_2 = 710L
L = Insulator length (m)
$t^{0.75}$ = Elapsed time after the lightning strike (μsec)

It is a challenge to be precise when modeling fast front transients. However, when the simulation and study are undertaken with care, a very valid insulation coordination study is possible. The other option is to use the guidelines in the standards that are more general in nature but can serve as a check to the refinement possible with a judicious simulation study. The inclusion of corona on conductors can be added, but the lowering of observed overvoltages that results, may remove some of the safety factor built into the models. Usually corona is not considered in studies for this reason.

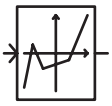
SUMMARY OF ARRESTER SELECTION

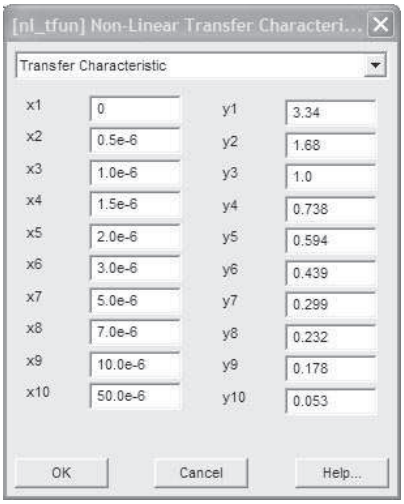
A selection procedure for determining suitable arrester characteristics is summarized based on continuous operating voltage Uc, rated voltage Ur and energy capability [1], [2].

1. Select r.m.s. continuous operating voltage Uca which is always equal to or greater than actual applied crest voltage divided by 2. If harmonic effects are not known, Uca should be taken as the system voltage crest divided by 6 for normal phase-ground arresters. If the system voltage crest is not known, the highest voltage for equipment U_m should be used instead.
2. Select rated voltage Ur through evaluating TOV capability. **Calculations and switching surge studies are required to select U_{ca}**. Note that different arresters may have the same U_{ca} but different U_r. IEC standards require a TOV capability for 10 seconds equal to or greater than the rated voltage after being pre-heated to 60OC and dissipating a required energy. For 5 kA arresters (class 1) and 10 kA arresters (classes 2 and 3), the energy is taken by 1 current impulse. For 20 kA lightning arresters, classes 4 and 5, the energy is taken by three high current impulses.
3. Select nominal discharge current. For systems with U_m 52 kV, use a nominal discharge current I_n = 5 – 10 kA. For systems with U_m 300 kV, use a nominal discharge

CSMF circuit to initiate a back flashover arc across an insulator string. The Integrator ramps time (Tstart) when the surge is detected by the Comparator component. A Non-Linear Transfer Characteristic component models the elapsed time factor $1/t^{0.75}$. A slider sets insulator string length L and another Comparator component compares the computed flashover voltage Vfo with the voltage across the string Vstring and initiates the switch shorting the conductor to the tower.

The settings in the Non-Linear Transfer Characteristic component modeling $1/t^{0.75}$ are:





The Monostable components in the back flashover model are included to hold the Comparator output to 1 for the duration of interest.

current I_n = 10 kA. For systems with U_m > 300 kV, use a nominal discharge current I_n = 10 – 20 kA.

4. Select protection level for insulation coordination. Take into account:

   (i) prospective amplitude and steepness of overvoltage;
   (ii) distance between arrester and protected equipment;
   (iii) insulation level, surge impedance and/or capacitance of protected equipment;
   (iv) safety margin for station and equipment insulation (typically 20% as given by IEC 60099);
   (v) acceptable risk, i.e. the importance of the station; and
   (vi) the number and positioning of arresters.

5. Selection of energy capability. Usually at higher voltages, switching surges may define energy capability. Switching-in against a trapped charge on a transmission line is generally considered to be the decisive case for an arrester installed at the open far end of the line, particularly if closing onto a single phase bolted fault is also considered. Lightning discharge tests must be made taking into account the probabilities associated with strike amplitude and waveshape. Switching of capacitor banks can impose heavy duties on surge arresters, especially if the decisive case takes into account single or two phase re-strikes of the breaker.

REFERENCES

1. L. Stenström, "*Metal Oxide Surge Arresters in AC Systems, Part VI: Selection of Metal Oxide Arresters from the Standards*," Electra, December 1990, No.133, 146-165.

2. IEC 60099 Series of Standards, Parts 1 to 5.

3. IEEE WG 3.4.11, "*Modeling of Metal Oxide Surge Arresters*," IEEE Transactions of Power Delivery, Vol. 7, No. 1, January 1992, pp 302-307.

4. IEEE PES Special Publication edited by A.M. Gole, J. Martinez-Valesco, A.J.F. Keri, "*Modeling and Analysis of System Transients*," IEEE Working Group 15.08.09, IEEE Publication No. 99TP133-0.

5. IEEE Tutorial Course, "*Surge Protection in Power Systems*," 79 EHO144-6-PWR. 1978.

6. W.A. Chisholm, Y.L. Chow, "*Travel Time of Transmission Towers*," IEEE Transactions on Power Apparatus and Systems, Vol. PAS-104, No. 10, October 1985, pp 2922-2928.

7. Transmission Line Reference Book, 345 kV and Above, Second Edition, Electric Power Research Institute, Palo Alto, California, 1982.

EXERCISES

4.1 Load example case Example4-1.psc. This is the test circuit to develop the fast front surge arrester model parameters. Check that the surge arrester U_{10} discharge voltage with an 8/20 sec standard impulse is 470 kV. Check also that the switching surge discharge voltage U_{ss} is 403.9 kV for a 3 kA, 300/1000 sec test impulse. Develop a fast front surge arrester model for a one column arrester of length 1.45 metre. Its U_{10} discharge voltage with an 8/20 sec standard impulse is 248 kV and the switching surge discharge voltage U_{ss} is 225 kV for a 3 kA, 300/1000 sec test impulse.

4.2 Load example case Example4-2.psc. This is where a 10 kA lightning strike hits a phase conductor at a 230 kV station entrance. The lightning is modeled by a 1.2/50 sec standard impulse. The surge arrester is located at the transformer terminals. Observe the maximum overvoltage at the transformer terminal. Increase the amplitude of the lightning surge to 20 kA and observe the transformer terminal over-voltages. Move the surge arrester 10 metres away from the transformer terminal and repeat the tests.

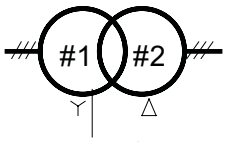
Chapter 5:

Transformers

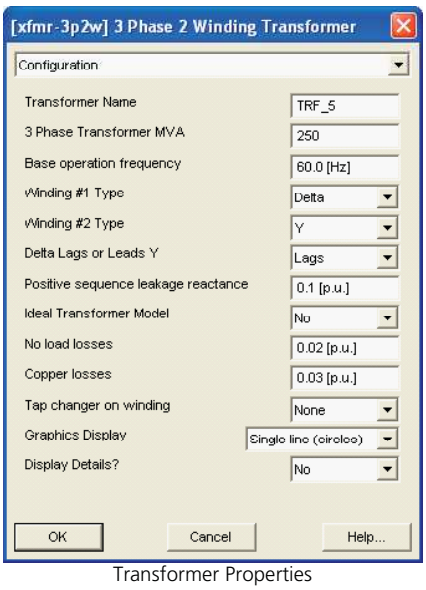
Simulation of transformers requires an understanding of some of their basic properties involving both core and winding configurations. This is complicated by the fact that transformer cores are prone to saturation given the non-linear characteristics of their materials. This leads to different phenomena like inrush currents, remanence, geomagnetic current effects and ferroresonance, among others.

The main emphasis of this chapter is placed on the simulation of the transformers' magnetic properties. The effects of winding capacitances are generally minimal at lower frequencies and for most studies where the frequencies of interest are below 2000 Hz might not need be modeled. The study of switching transients could require a simple representation of the winding capacitances. Inter-winding and winding to ground capacitances become important when fast front studies are to be performed. In these cases, the core's magnetic effects can usually be neglected.

The transformer models are in the Transformers Library Group in the Master Library of PSCAD.



Three phase Component of General Transformer model



Transformer Properties

TRANSFORMER MODELS

There are two basic types of transformer models available in PSCAD. The original 'General Transformer Model' constructed with single phase units and the UMEC model which has provision for specifying the configuration of the core in single and three phase units.

When using the General Transformer Model with the "non-ideal option" selected, the unsaturated magnetizing current of the transformer at rated volts is directly incorporated into the transformer impedance matrix. Usually, the unsaturated magnetizing current at rated volts is less than 1% for most power transformers.

When the 'Saturation enabled' option is selected as 'yes' (see below), a saturation branch is included in the model and the magnetizing current effects are also modeled as part of this saturation branch. Therefore, it is not recommended to select 'non-ideal transformer' and 'saturation' at the same time. It will cause duplicity in the calculation of the magnetization, and can lead to erroneous results when working at voltages close to the nominal value.

The p.u. no-load and load losses can be specified for the base MVA of the transformer. These losses will be evenly allocated to each voltage rating of the transformer by means of shunt resistors (for no-load) and series resistors (for load losses). If a non-even distribution of losses between voltage ratings is desired, it is recommended

For users using the GNU FORTRAN compiler, there are dimensioning limits on the number of transformers that can be applied in a model.

If this limit is reached, convert three-phase transformers to the UMEC models as these are counted as one transformer only. Regular three-phase transformers are counted as three units, since they use a single phase transformer for each of their phases.

to setup the losses to 0.0 p.u. and to add the respective external resistances. For many studies, the effect of winding resistance is negligible, especially if the system losses are dominant.

Core Configuration

The positive and zero sequence leakage impedances of three phase transformers are dependent upon both core configuration and winding configuration. If the core is three-limb, then the effect is to have a zero sequence impedance voltage relatively similar in value to the positive sequence impedance voltage. This is because when the transformer is subjected to zero sequence voltages, there isn't a closed core path for zero sequence flux to flow. Consequently, the zero sequence flux passes through air, yoke and tank, causing the zero sequence impedance voltage to be slightly lower. In the General Transformer Model, this effect can be approximated by adding a fictitious delta winding and fine tuning the impedances from the existing windings to the added delta winding. Note that there is no need to do this when using the three-phase UMEC model, since its magnetic circuit configuration accounts for the zero sequence flux path.

Some three phase transformers have their zero sequence impedance larger than their positive sequence impedance. A compensating neutral reactance XN can be added at the star point to ground. If the positive sequence leakage reactance is XH-L, then the zero sequence reactance XO of the transformer from its star winding is:

$$X_O = X_{H\text{-}L} + 3 \cdot X_N$$

From which;

$$X_N = [\, X_O - X_{H\text{-}L} \,]/3$$

The neutral reactance is patched into the network model as an inductance. Its value is:

$$L_N = X_N * MVA / (\omega * V_H^2)$$

Where:

X_N = Neutral reactance in per unit on the transformer base MVA and the star winding voltage rating.
MVA = Transformer base MVA rating.
V_H = Rated line-to-line rms volts of the star winding.
ω = System frequency in radians per second.

The three phase UMEC transformer model provides the option of selecting either a three-limb core or a five-limb core configuration which is inherent to the model. A simple short circuit test can be undertaken by simulation to determine if the positive and zero sequence impedances are as expected. If additional zero sequence impedance is required, the above method can be applied.

Modeling three-limb core transformers with single-phase units is an accepted procedure. The reason for this is that there is a direct relationship between transformer sequence impedances and mutually coupled impedances:

$$Z_S = 1/3\ (Z_O + 2Z_1)$$

$$Z_M = 1/3\ (Z_O - Z_1)$$

Where: Z_S = Transformer Self impedance
Z_M = Transformer Mutual impedance
Z_O = Transformer Zero Sequence impedance
Z_1 = Transformer Positive Sequence impedance.

The windings of the transformer will be correctly represented as mutually coupled by the impedance coupling matrix, which for a three phase transformer looks like this:

$$\begin{bmatrix} Z_S & Z_M & Z_M \\ Z_M & Z_S & Z_M \\ Z_M & Z_M & Z_S \end{bmatrix}$$

With a Y-Y three-phase three-limb transformer, or for that matter any three phase transformer, the procedure to represent it in simulation out of single phase banks is to add a fictitious delta winding so that the zero sequence and positive sequence impedances match correctly.

In order to use the UMEC model, some core construction parameters (aspect ratios) such as:

Yoke - winding limb length ratio,
Yoke – winding limb cross-sectional area ratio,
Yoke – outer limb length ratio, and
Yoke – outer limb cross-sectional area ratio

are needed in addition to name plate data. They may have to be estimated if not known. In most situations, the Core Cross-sectional Area ratio can be set to 1.0. Leakage reactances are not affected by these ratios. They mainly affect the distribution of flux among the limbs.

Ungrounded Windings

Sometimes a transformer has an ungrounded winding without any load connected to it. When the case is run, a warning message may appear or the case may stop with numerical instability. This is because the winding has no way to keep itself from accumulating voltage and it will drift until the problem manifests itself in some way compromising the precision of the simulation. Delta windings on three phase transformers are often at risk in this way.

The solution is to simply ground one terminal of the winding through a very large resistance. A suitable resistance value should add shunt losses no higher than 0.1% of the MVA rating of the winding. If it is a three phase winding, apply such a resistor on at least one phase, but if on all three, then balanced winding terminal voltages should result.

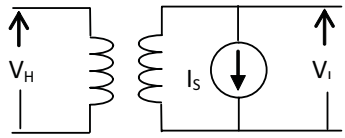
SATURATION

The General Transformer model represents saturation with a current source placed across a selected winding. The winding wound closest to the core is the winding usually selected as it is closest to where the magnetic effects are occurring. This is often the lowest voltage winding or the tertiary winding if there is one. In a HVDC converter transformer, the HV winding is usually closest to the core.

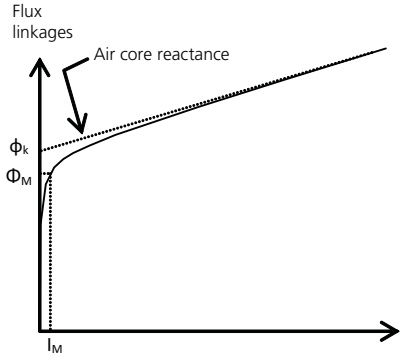
The saturation characteristic is represented in PSCAD with a single valued continuous function that converges to the vertical flux axis at low currents, and asymptotically to the air core reactance line at high currents. Although it is modeled in a simple manner, as seen in the Saturation Properties Sheet, it is a reasonable modeling technique, since the true saturation characteristic of a transformer is rarely known with any degree of precision.

The Saturation Property Sheet includes the Inrush decay time constant parameter. The decay of the inrush current in a transformer is given by the resistance in the transformer's primary circuit (or transformer winding being energized). If the resistance in such circuit is very low, the Inrush current will take several seconds to decay. PSCAD offers the possibility of forcing a fast decay of the inrush current by artificially introducing damping in the circuit. The smaller the inrush decay time constant (in seconds), the faster the inrush current will decay. However, if a value of 0.0 is entered, PSCAD will not introduce any artificial damping in the circuit and the inrush damping will be dictated solely by the network.

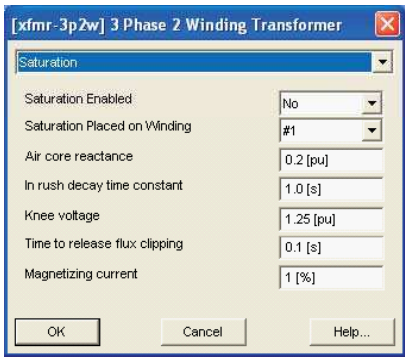
Time to release flux clipping is also an important parameter to consider. When a case is starting up initially, for calculation TIMES less than the value entered here, the flux is inhibited or clipped and can't pass into saturation. This has the effect of centering the flux. This feature allows the network to initialize with the transformers being in saturation. If 0.0 seconds is



Saturation in a General transformer model represented by a current source



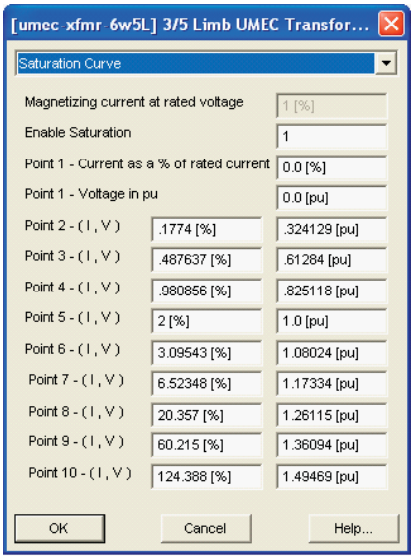
ω_k = Knee flux (p.u.)
ω_M = Flux at rated volts (p.u.)
I_M = Magnetizing current at rated volts (taken from the value entered in the Windings Property Sheet)



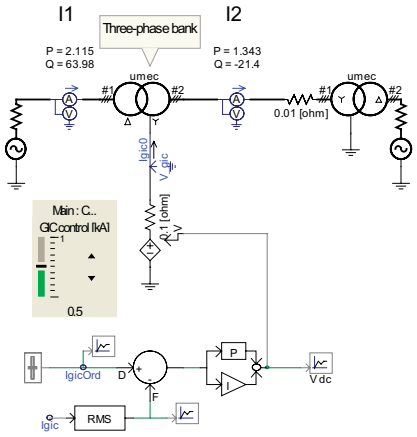
Saturation Property Sheet for the General Transformer component

Air core reactance is often not known with accuracy. A rule-of-thumb is twice the leakage reactance, but consideration must be given to which winding this is observed from, and the leakage reactance too.

Care has to be taken in studying power electronic cases where converters are connected to transformers. If controls and conditions are not properly designed, the transformers may drift into saturation. This is a real condition which can exist. The classical example is at a HVDC converter. If the DC side current has a power frequency component, it can saturate the converter transformer. In some HVDC converter stations, a fundamental frequency blocking filter is added to the neutral side of the converter bridge to prevent power frequency currents from flowing through the converter. STATCOMs.



Data entry for saturation characteristic of UMEC transformer for 0.24 p.u. air core reactance and 1.26 p.u. knee point.



Test circuit to evaluate the effect of saturation due to zero sequence DC currents flowing through the grounded star winding.

Note: The measured dc component of the neutral current Igm is filtered using a RMS component in order to take out the harmonics in the neutral connections:

Note:
For this method to work effectively with the general transformer model, the Inrush decay time constant in the Saturation Property Sheet should be set to 0.0.

In the UMEC transformer model, there is no inrush decay time constant.

entered, sustained inrush currents during start-up may inhibit an effective steady state condition for the snapshot. This effect is lessened if the ac voltage sources are ramped up slowly over many cycles.

After the calculation TIME has exceeded the **Time to release flux clipping**, the clipping is removed and the flux may migrate into saturation if network conditions dictate so.

The UMEC transformer model has a distributed saturation characteristic defined in straight line segments by ten pairs of entered points. It is not necessary to place the saturation across a specific winding because the saturation is distributed to all windings.

GEOMAGNETICALLY INDUCED CURRENTS

Geomagnetically induced currents (GIC) as they effect transformers, are the slow varying components of induced currents which may flow in transmission networks during a geomagnetic storm. GIC are more severe the closer the transmission network is to one of the Earth's magnetic poles. GIC are zero sequence, quasi direct current and if they flow through a grounded transformer winding, may cause the transformer to saturate.

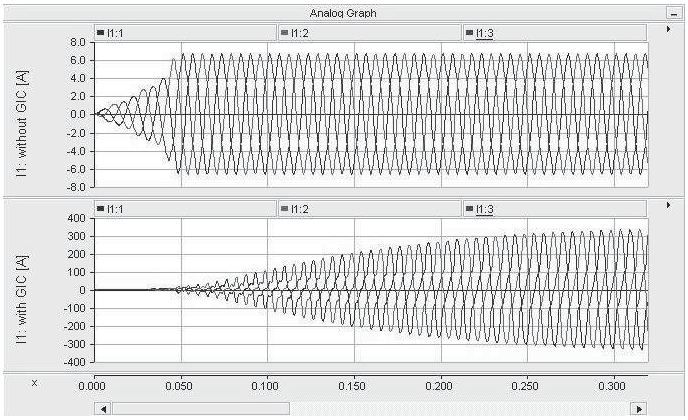
The same effect occurs if some DC ground return current from an HVDC transmission system spills into the nearby AC system through substation grounds. The consequence of saturation due to such DC or quasi DC currents is that the transformer will demand AC reactive power from the system and place a strain on the AC voltage. In addition, the saturated transformer will generate an increased amount of harmonics causing the AC system voltage to become distorted.

To examine the DC saturation effect on a particular transformer, a test circuit is created in PSCAD/EMTDC.

The zero sequence DC current flowing through the star winding is achieved by means of a DC voltage source in the transformer neutral. The DC current level in this neutral source is achieved by a simple feedback control. The desired DC neutral current is set by the Slider Component and is compared with the measured DC current in the neutral. The difference is then passed through a PI controller that adjusts the DC voltage accordingly.

Something that should be taken into consideration when using the General Transformer Model to model GIC is that the DC current will mathematically transform between the ideally coupled windings. In steady state, this DC current will divert through the inductive magnetizing branch, being forced out of the other windings by the secondary winding resistances. Therefore, in order to effect the correct level of saturation due to the DC current, the test circuit must have some winding resistance inserted in the secondary winding. If the UMEC model is used, copper loss must also be introduced in order to obtain correct results.

Three-phase banks and five-limb core type transformers are the most prone to saturate due to geomagnetically induced currents. Three-limb transformers require comparatively larger Igic in order to saturate.



Primary AC current (I_1) in a transformer affected by GIC. Note that the magnetizing current has an amplitude of 320 A when affected by GIC phenomena, compared with 7.0 A peak magnetizing current under normal conditions (no GIC).

REMANENCE

At times it is important to investigate energizing events of transformers. There is usually residual magnetism in the core. This phenomenon is commonly known as "remanence." The degree of magnetizing inrush current during energizing is a function of:

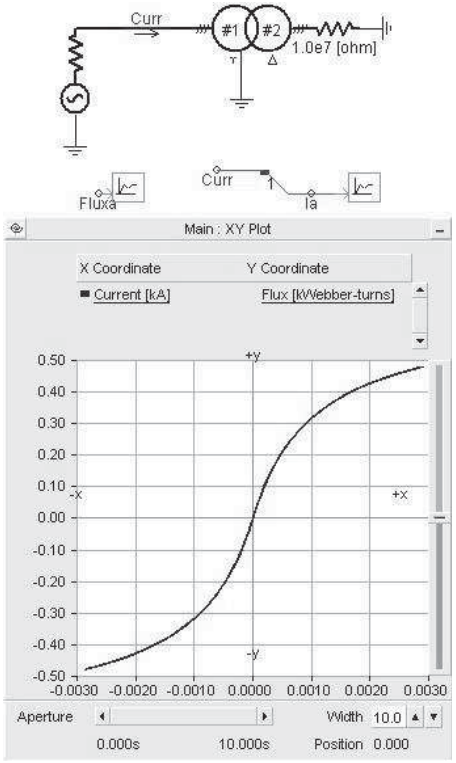
1. The position on the supply voltage wave shape that each phase of the closing circuit breaker actually closes on.
2. The remanence existing in each of the main legs of the transformer core.

The level of remanence in the core is determined by the conditions associated with the de-energizing event of the transformer. Even though such conditions are usually unknown, it is useful to anticipate the worst scenario that might be expected on any random energization. The maximum remanence that might exist in any leg of the core is around 80% of the peak flux generated at rated volts. This is determined from the rated RMS voltage V_r of the winding that is being referenced for remanence. Peak flux linkage M referenced to winding at rated V_r is:

$$M = V_r / 4.44\ fr \qquad [1]$$

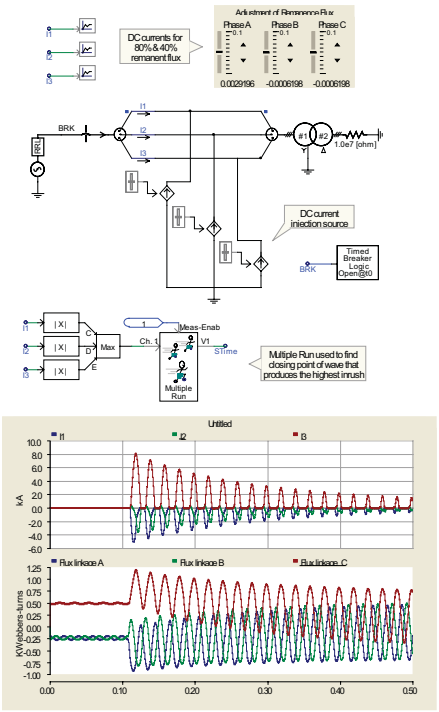
Where fr is rated power frequency in Hz

The core's magnetic non-linearity is modeled in PSCAD through a single valued curve (see figure); therefore, the core's magnetic hysteretic behavior is not directly represented. Because of this, it is necessary to resort to alternative methods in order to simulate the effects of remnant flux in the core.

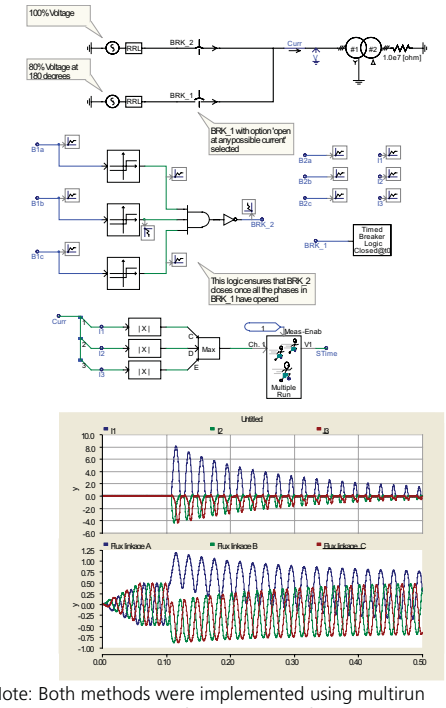


Setup used to plot the flux linkage in kWebbers·turns vs. magnetizing curve of a transformer

Note: Since the saturation option in the transformer component is selected for this type of study, it is recommended to select the 'ideal transformer' option as 'yes' when working with the 'General transformer model,' as it was explained in the 'Transformer models' section.



The current sources controlled by the sliders inject DC current through each primary winding phase before the transformer is energized and while the circuit breaker is open. The remanence in each leg is adjustable by setting the sliders and the resulting flux linkages can be observed. When the energizing circuit breaker is closed at 0.1 seconds, the resulting transformer inrush current is evident.



Note: Both methods were implemented using multirun components in order to find the point of wave or switching time that led to the maximum inrush current.

One way to simulate remanence in a de-energized transformer is by introducing controlled DC current sources. The case is run with the circuit breaker open and the current sources in each phase adjusted to generate the required remanence. The current sources can remain in the circuit at their remanence setting during the run as they do not impact the results.

The application of this method is better explained through an example case. Let's have a three-phase transformer with wye-delta connection. It will be assumed that when the breaker de-energized the transformer, it opened all the phases at the same instant of time, and that one of the phases (phase A) was opened when its voltage was at its peak leaving an 80% remanence, and a -40% remanence in each of the other two phases.

In order to find out how much direct current should be injected, it is necessary to plot the flux linkage vs current curve for the given transformer winding. The flux linkage can be obtained directly from one of the outputs in the transformer component or by integrating the voltage over the primary winding. This curve should be plotted with the voltage set to 80% and to 40%. The current peak values should be read for both cases. These two currents are the magnitude of the DC currents to be injected in the inrush test circuit. $(+)Im_{80\%}$ for one phase and $(-)Im_{40\%}$ for the other two phases.

Note: A method that can be used to check if the simulation is properly setup and is measuring the fluxes before the energization of the transformer. The fluxes should approximately match the values read in the flux linkage vs magnetizing current plot.

In a transformer with its primary circuit connected in delta, there is no direct access to the terminals of each winding, therefore making it difficult if not impossible to control how much of the DC injected current goes to each of the winding phases. In this kind of case, a second method can be used for simulating inrush like currents.

In this method, two sources 180 degrees apart are connected in parallel through a couple of breakers. One of the sources is used to obtain the required remanence flux in the core during the pre-energization period, while the other one represents the system the transformer is going to be energized from.

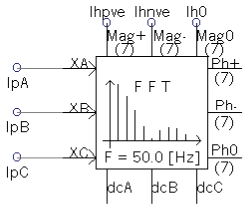
Here, the results will depend greatly on the moment at which the breaker is setup to be opened, at 0.0 kA or at some value higher than this. In the case illustrated in the figure, BRK_1 was set to open at any current value in order to comply with the assumption that all the phases were de-energized at the same instant of time. Even though this method is mostly intended for transformers with primary windings connected in delta, the example was run using the same wye connected transformer given in the first example in order to show that both methods lead to similar results.

HARMONIC MEASUREMENTS

With transformer saturation effects being of interest, on-line measurement of current and voltage harmonics is sometimes required in a study. The On-Line Frequency Scanner component (FFT) is most useful for this purpose. It can read in 1, 2 or 3 phase signals of current or voltage, and measure phase or sequence (if 3 phase) harmonics, as desired. It generates from 7 to 255 harmonics on-line which can be plotted or observed on meters.

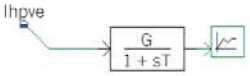
The On-Line Frequency Scanner component is most useful for studying effects of GIC on transformers by running the case in saturated steady state. The option to produce harmonic currents in sequence components will indicate that the 1st harmonic is dominantly +ve sequence, the 2nd harmonic is dominantly –ve sequence, the 3rd harmonic is dominantly 0 sequence, the 4th harmonic is dominantly +ve sequence, and so it cycles around.

The on-line measurement enables a quick assessment of the harmonics being generated. The other option is to write the input signals from the On-Line Frequency Scan component into an output file. PSCAD/EMTDC output files can be read by a post-processor, such as Z Systems' LiveWire plotting package from which a Fourier analysis can be performed.



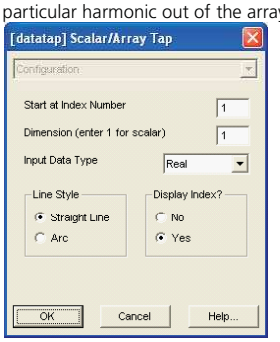
On-Line Frequency Scan component measuring three phase currents and generating sequence harmonic currents up to the 7th harmonic.

Components from the Master Library when assembled, enable a harmonic magnitude or phase to be measured.



The key component to differentiate the harmonic from the signal array named in this instance as "Ihpve" is the Datatap Connection component or Data Signal Array Tap Connection which is:

The Datatap Connection component can be edited in order to select the particular harmonic out of the array signal:



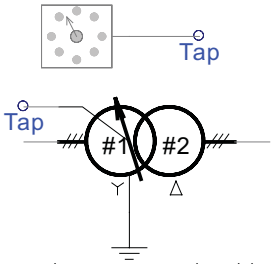
LOAD TAP CHANGER

Most of the transformer components have provision for a tap changer adjustable on-line. The transformer component data entry sheet has an entry "**Tap changer on winding**" to define the number of the winding on which the tap changer is applied.

General Transformer models bring out a signal wire when the tap changer is requested. A signal in per unit of winding rated voltage must be generated and fed to the signal wire controlling the tap position.

UMEC transformer models have an internal input request when the tap changer is requested. In this model, the per unit tap value is entered into the data entry sheet.

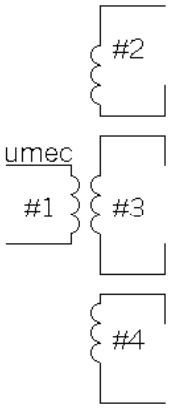
The on-line tap change is not affected the way a tap change occurs on an actual transformer. Instead, when the change in tap is detected, the network solution is adjusted. It is possible to have a continuous change of tap but this would require re-ordering the network solution every calculation time step. It is practical to change taps in steps, either from manual adjustment using a slider or rotary switch component, or from a controller with appropriate delays and steps built in (To build steps into a continuous signal, use the "datafile" component from the CSMF page of the Master Library. When used in Sample and Hold output mode, a continuous signal can be broken up into discrete steps).

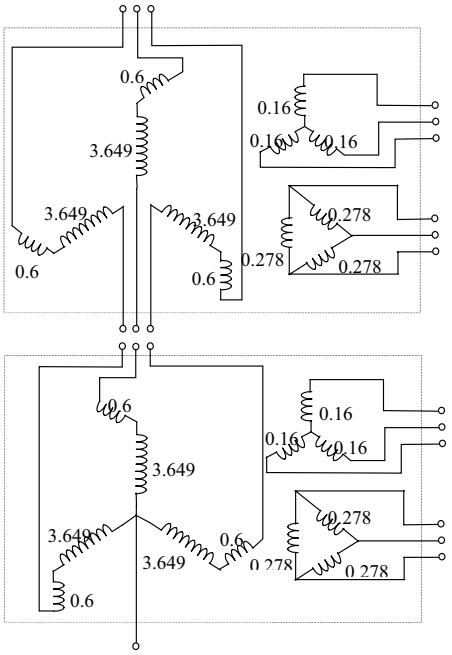


Tap changer on general models

The winding connections for each transformer are shown. The winding turns for each winding and is proportional to the number indicated (kV rating of the winding). The core on which each winding is wound is defined by the angle of alignment depicted in the diagram.

The AC side windings are wound to provide a 7.5° phase shift.





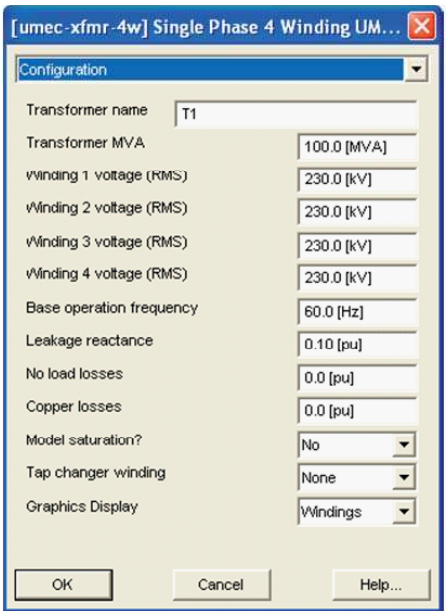
More complex winding arrangements might require more than four coupled windings, which is not available in the Master Library. Contact support@pscad.com if you have a need for more coupled windings.

PHASE SHIFTING TRANSFORMERS

Phase shifting transformers can be assembled in PSCAD using multi-winding single phase transformers. This requires that the winding connections be known. Tap changers can be applied to effect a variable phase shift. If core modeling is a requirement, the advantage of the UMEC three phase transformer with its core modeling capability is of limited benefit because each winding end cannot be brought out for connections. If the actual phase shifter is constructed with a three limb core, a fictitious delta winding may need to be added in the model built from single phase units to obtain the correct zero sequence effects.

As an example, converters with 24 pulse or higher employ phase shift transformers. Consider a 24 pulse converter transformer comprised of two similar 12 pulse converter transformers, one phase shifted +7.5° and the other phase shifter –7.5°.

Each 12 pulse transformer is assembled in single-phase units from the UMEC four winding model in the Transformers Page in the Master Library. The connections are made as shown above with the star primary windings in series.



Leakage reactance is best checked by undertaking a simulated short circuit test. Apply a short circuit to the secondary windings with small resistances and determine the p.u. transformer short circuit reactance as calculated from the measured voltages. Adjust the transformer leakage reactance until the desired short circuit reactance is observed by short circuit test.

Other types of complex transformers, such as 6-phase and zig-zag transformers, can also be built by assembling single-phase units.

REFERENCES

1. Hermann W. Dommel, "*Transformer Models in the Simulation of Electromagnetic Transients*," 5th Power Systems Computation Conference, Cambridge, England, Sept 1-5, 1975.

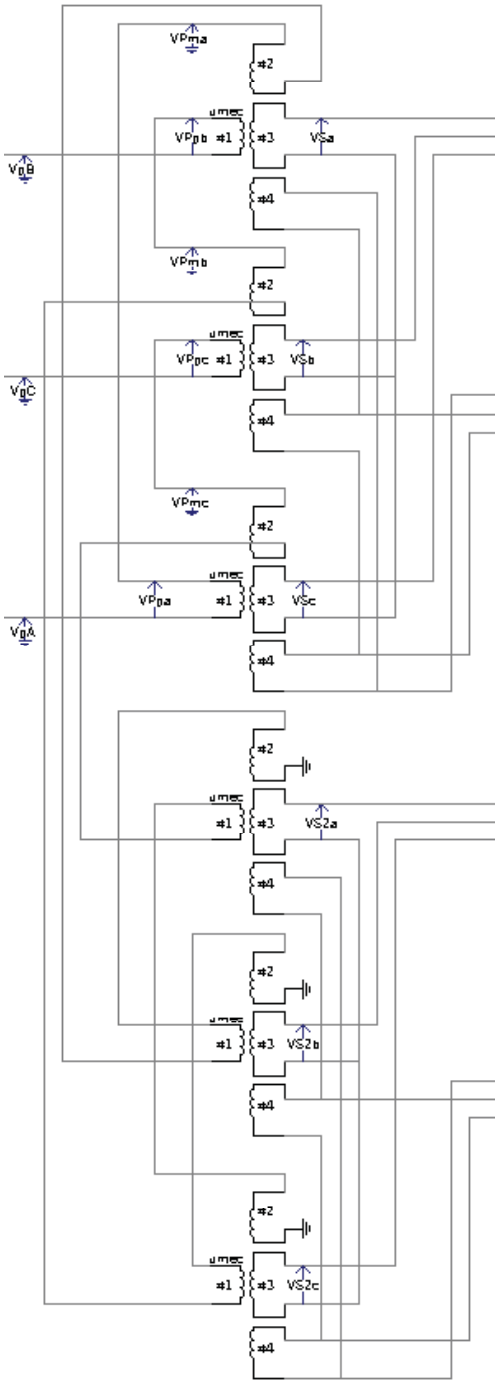
2. W. Enright, O.B. Nayak, G.D. Irwin, J. Arrillaga, "*An Electromagnetic Transients Model of Multi-limb Transformers Using Normalized Core Concept*," Proceedings of IPST'97 – International Conference on Power System Transients, Seattle, June 22-26, 1997, pp 93-98.

EXERCISES

5.1 Load example case *Example5.1.psc* which is the case of a DC current saturation test with a Y-Y winding configuration and a UMEC three limbed core. Start the case with 0.1 kA of DC current in the neutral and confirm the transformer does not saturate. Change to a 5 limbed core and repeat the test. Build the transformer from single phase units for a Y-Y winding configuration of the same 3 phase rating as the UMEC model using the general transformer model. Repeat the test with 0.1 kA in the transformer neutral showing saturation. Design a third delta winding to represent a 3 limb core and repeat the test and compare with the UMEC test with a 3 limb core.

5.2 With example case *Example5.1.psc* studied above for the Y-Y winding configuration, observe the harmonics detected in the primary windings of the transformer (winding #1). Make note of the 3rd harmonic level. Change the secondary winding to a Δ winding and repeat the test with all other parameters remaining equal. Was any 3rd harmonic detected and why?

5.3 Load example case *Example5.3.psc* which is a case to energize a transformer with remanence setting. With the circuit breaker initially closed, and the remanence at zero in each phase, ramp the source volts up slowly (change the Three Phase Source parameter **Voltage Input Time Constant** on the data entry sheet) and observe what the peak flux linkages are in reference to the 230 kV winding (#1). Is this level expected? Return the breaker to close at 0.5 second, and the **Voltage Input Time Constant** to 0.05 seconds, and adjust the remanence initializing current sources until a maximum inrush current on one of the phases is observed. Do not take the remanence above 0.8 p.u. of rated flux. Adjust the **In rush decay time constant** in the saturation data sheet of the transformer model to 0.0, thus removing any artificial inrush current damping, and observe response.



Connection of six four-winding single-phase UMEC transformers for 24 pulse converter application.

Chapter 6:

DC Transmission

Electric power transmission was originally developed with direct current. The availability of transformers and the development and improvement of induction motors at the beginning of the 20th Century, led to greater appeal and use of AC transmission.

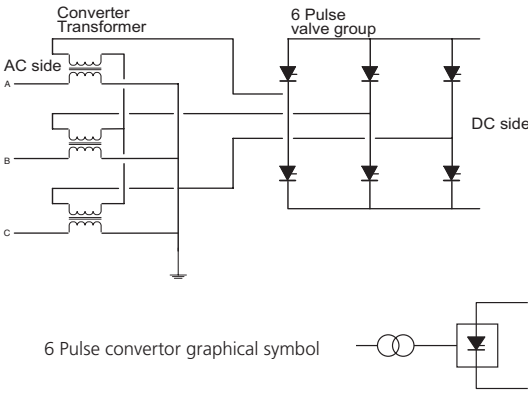
DC transmission became practical when long distances were to be covered or where cables were required. Originally, mercury arc valves were used in the converters. Thyristors were applied in the late 1960s and solid state valves became a reality. In 1969, a contract for the Eel River DC link in Canada was awarded as the first application of solid state valves for HVDC transmission. Today, the highest functional DC voltage for DC transmission is +/- 600 kV for the 785 km transmission line of the Itaipu scheme in Brazil. DC transmission is now an integral part of the delivery of electricity in many countries throughout the world.

WHY USE DC TRANSMISSION?

The question is often asked, "Why use DC transmission?" One response is that losses are lower, but this is not correct. The level of losses is designed into a transmission system and is regulated by the size of conductor selected. DC and AC conductors, either as overhead transmission lines or submarine cables, can have lower losses but at higher expense since the larger cross-sectional area will generally result in lower losses but cost more.

When converters are used for DC transmission in preference to AC transmission, it is generally by economic choice driven by one of the following reasons:

1. An overhead DC transmission line with its towers can be designed to be less costly per unit of length than an equivalent AC line designed to transmit the same level of electric power. However, the DC converter stations at each end are more costly than the terminating stations of an AC line and so there is a breakeven distance above which the total cost of DC transmission is less than its AC transmission alternative. The DC transmission line can have a lower visual profile than an equivalent AC line and so contributes to a lower environmental impact. There are other environmental advantages to a DC transmission line through the electric and magnetic fields being DC instead of AC.
2. If transmission is by submarine or underground cable, the breakeven distance is much less than overhead transmission. It is not practical to consider AC cable systems exceeding approximately 60 km but DC cable



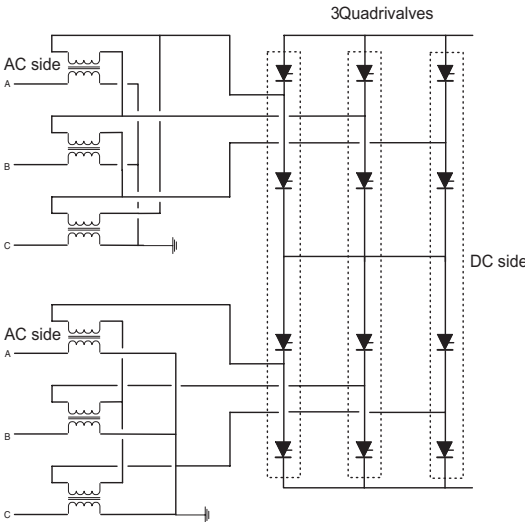
Electric circuit configuration of the basic six pulse valve group with its converter transformer in star-star connection.

transmission systems are in service whose length is in the hundreds of kilometers and even distances of 600 km or greater have been considered feasible.

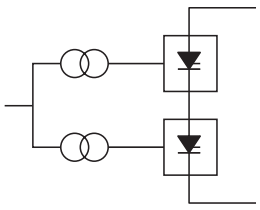
3. Some AC electric power systems are not synchronized to neighboring networks even though the physical distances between them is quite small. This occurs in Japan where half the country is a 60 Hz network and the other is a 50 Hz system. It is physically impossible to connect the two together by direct AC methods in order to exchange electric power between them. However, if a DC converter station is located in each system with an interconnecting DC link between them, it is possible to transfer the required power flow even though the AC systems so connected remain asynchronous.

DC CONVERTER CONFIGURATIONS

The integral part of an HVDC power converter is the valve or valve arm. It may be non-controllable if constructed from one or more power diodes in series or controllable if constructed from one or more thyristors in series. The standard bridge or converter connection is defined as a double-way connection comprising six valves or valve arms (six pulse) that are connected as illustrated above. Electric power flowing between the HVDC valve group and the AC system is three phase. When electric power flows into the DC valve group from the AC system, then it is considered a rectifier. If power flows from the DC valve group into the AC system, it is an inverter. Each valve consists of many series connected thyristors in thyristor modules. The six pulse valve group was usual when the valves were mercury arc.



The twelve pulse valve group configuration with two converter transformers. One in star-star connection and the other in star-delta connection.



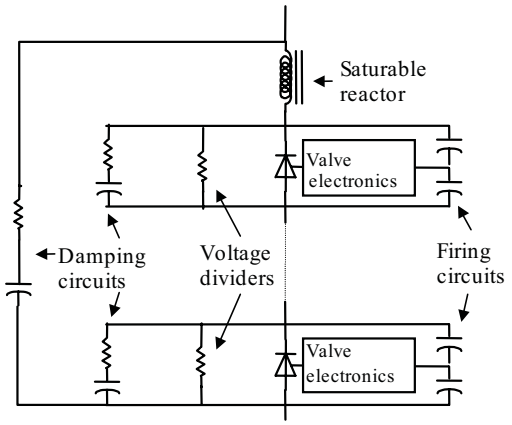
The twelve pulse converter unit graphical symbol.

TWELVE PULSE CONVERTERS

Nearly all HVDC power converters with thyristor valves are assembled in a converter bridge of twelve pulse configuration. The most common twelve pulse configuration is the use of two three phase converter transformers with one DC side winding as an ungrounded star connection and the other a delta configuration. Consequently, the AC voltages applied to each six pulse valve group which make up the twelve pulse valve group have a phase difference of 30 degrees which is utilized to cancel the AC side 5th and 7th harmonic currents and DC side 6th harmonic voltage, thus resulting in a significant saving in harmonic filters. A group of four valves in a single vertical stack is known as a "quadrivalve" and is assembled as one valve structure by stacking four valves in series. Since the voltage rating of thyristors is several kV, a 500 kV quadrivalve may have hundreds of individual thyristors connected in series groups of valve or thyristor modules. A quadrivalve for a high voltage converter is mechanically quite tall and may be suspended from the ceiling of the valve hall, especially in locations susceptible to earthquakes.

THYRISTOR MODULES

A thyristor or valve module is that part of a valve in a mechanical assembly of series connected thyristors and their immediate auxiliaries include heat sinks cooled by air, water or glycol, damping circuits (also known as "snubber" circuits) and valve firing electronics. A thyristor module is usually interchangeable for maintenance.

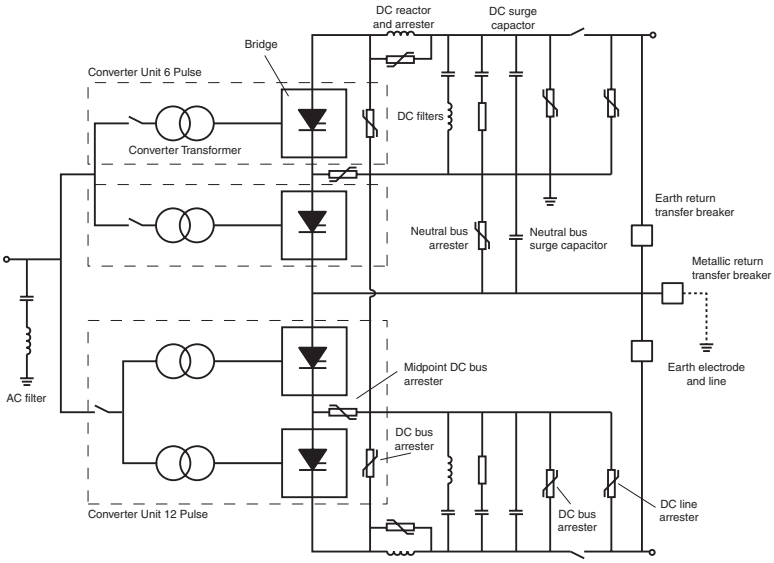


Components of the thyristor modules that make up a valve or quadrivalve.

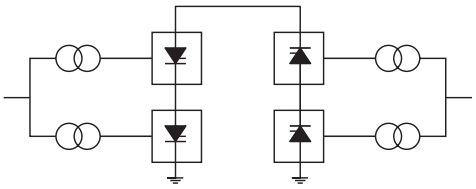
SUBSTATION EQUIPMENT

The central equipment of a DC substation is the thyristor converter and converter transformer. They may be configured into poles and bipoles. Some DC cable systems only have one pole or "monopole" configuration and may either use the ground as a return path when permitted or use an additional cable to avoid earth currents.

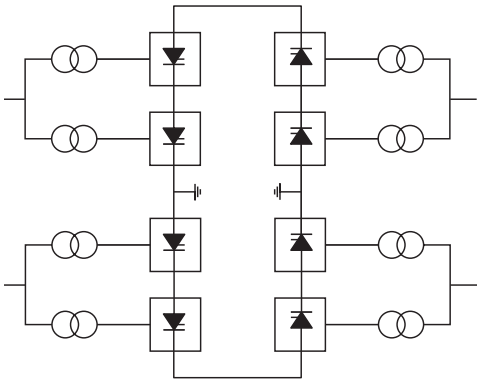
Harmonic filters are required on the AC side and usually on the DC side. The characteristic AC side current harmonics generated by 6 pulse converters are 6n +/- 1 and 12n +/- 1 for 12 pulse converters where n equals all positive integers. AC filters are typically tuned to 11th, 13th, 23rd and 25th harmonics for 12 pulse converters. Tuning to the 5th and 7th harmonics is required if the converters can be configured into 6 pulse operation. AC side harmonic filters may be switched with circuit breakers or circuit switches to accommodate reactive power requirement strategies since these filters generate reactive power at fundamental frequency. A parallel resonance is naturally created between the capacitance of the AC filters and the inductive impedance of the AC system. For the special case where such a resonance is lightly damped and tuned to a frequency between the 2nd and 4th harmonic, then a low order harmonic filter at the 2nd or 3rd harmonic may be required, even for 12 pulse converter operation.



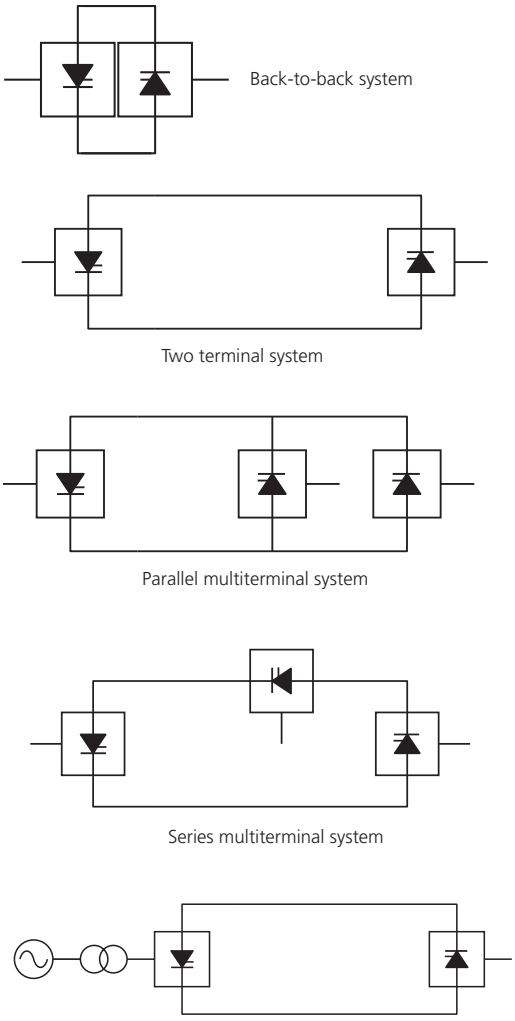
Layout of an HVDC substation



(a) Monopolar



(b) Bipolar



HVDC converter bridge arrangements

Characteristic DC side voltage harmonics generated by a 6 pulse converter are of the order 6n and when generated by a 12 pulse converter, are of the order 12n. DC side filters reduce harmonic current flow on DC transmission lines to minimize coupling and interference to adjacent voice frequency communication circuits. Where there is no DC line, such as in the back-to-back configuration, DC side filters may not be required.

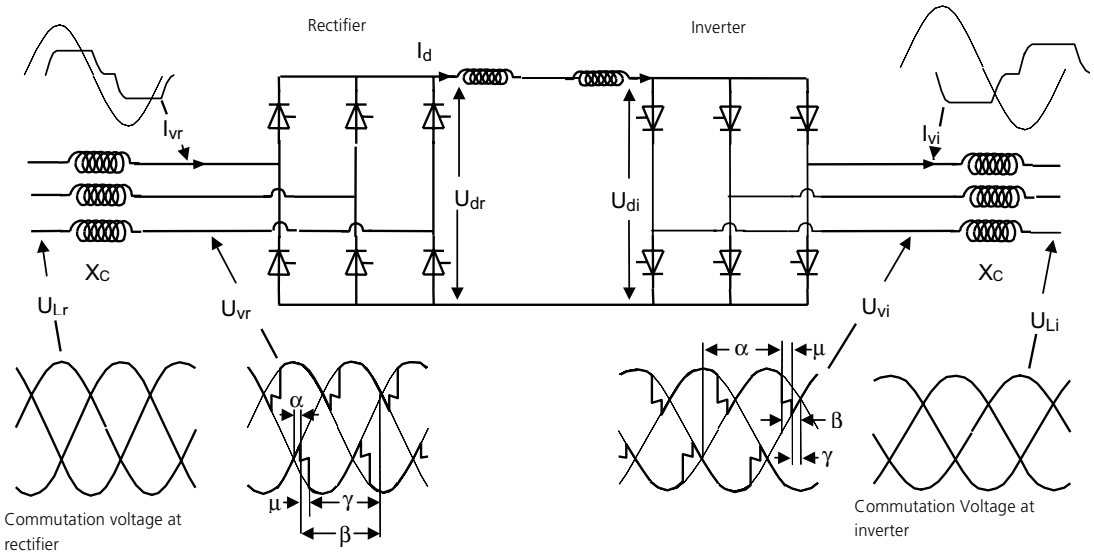
DC reactors are usually included in each pole of a converter station. They assist the DC filters in filtering harmonic currents and smooth the DC side current so that a discontinuous current mode is not reached at low load current operation. Because rate of change of DC side current is limited by the DC reactor, the commutation process of the DC converter is made more robust.

Surge arresters across each valve in the converter bridge, across each converter bridge and in the DC and AC switchyard are coordinated to protect the equipment from all overvoltages regardless of their source. They may be used in non-standard applications, such as filter protection. Modern HVDC substations use metal-oxide arresters and their rating and selection is made with careful insulation coordination design.

COMMUTATION

Rectification or inversion for HVDC converters is accomplished through a process known as line or natural commutation. The valves act as switches so that the AC voltage is sequentially switched to always provide a DC voltage. With line commutation, the AC voltage at both the rectifier and inverter must be provided by the AC networks at each end and should be three phase and relatively free of harmonics. As each valve switches on, it will begin to conduct current while the current begins to fall to zero in the next valve to turn off. Commutation is the process of transfer of current between any two converter valves with both valves carrying current simultaneously during this process.

Consider the rectification process. Each valve will switch on when it receives a firing pulse to its gate and its forward bias voltage becomes more positive than the forward bias voltage of the conducting valve. The current flow through a conducting valve does not change instantaneously as it commutates to another valve because the transfer is through transformer windings. The leakage reactance of the transformer windings is also the commutation reactance so long as the AC filters are located on the primary or AC side of the converter transformer. The commutation reactance at the rectifier and inverter is shown as an equivalent reactance XC in the figure below. The sum of all the valve currents transferred to the DC side and through the DC reactor is the direct current and it is relatively flat because of the inductance of the d. reactor and converter transformer.



Dc voltage and current waveshapes associated with dc converter bridges.

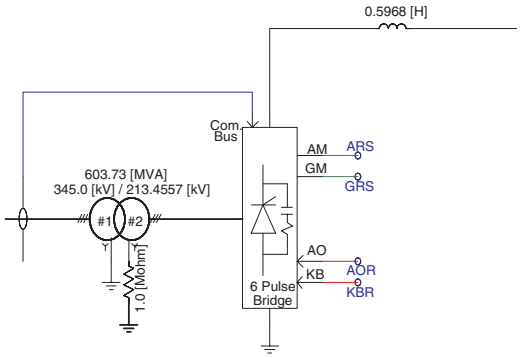
At the inverter, the three phase AC voltage supplied by the AC system provides the forward and reverse bias conditions of each valve in the converter bridge to allow commutation of current between valves the same as in the rectifier. The inverter valve can only turn on and conduct when the positive direct voltage from the DC line is greater than the back negative voltage derived from the AC commutation voltage of the AC system at the inverter.

Reversal of power flow in a line commutated DC link is not possible by reversing the direction of the direct current. The valves will allow conduction in one direction only. Power flow can only be reversed in line commutated DC converter bridges by changing the polarity of the direct voltage. The dual operation of the converter bridges as either a rectifier or inverter is achieved through firing control of the grid pulses.

CONVERTER BRIDGE ANGLES

These converter bridge angles are measured on the three phase valve side voltages and are based upon steady state conditions with a harmonic free and idealized three phase commutation voltage. They apply to both inverters and rectifiers.

Delay angle α. The time expressed in electrical angular measure from the zero crossing of the idealized sinusoidal commutating voltage to the starting instant of forward current conduction. This angle is controlled by the gate firing pulse and if less than 90 degrees, the converter bridge is a rectifier and if greater than 90 degrees, it is an inverter. This angle is often referred to as the firing angle.



Converter bridge in PSCAD/EMTDC. The valve firing controls are internally set up with a phase locked oscillator. The input control signals are firing angle α (in radians) and pulse blocking signal KB (0 or 1, 0 to block, 1 to deblock).

$$\beta = 180.0 - \alpha$$

Advance angle ß. The time expressed in electrical angular measure from the starting instant of forward current conduction to the next zero crossing of the idealized sinusoidal commutating voltage. The angle of advance β is related in degrees to the angle of delay α.

Overlap angle μ. The duration of commutation between two converter valve arms expressed in electrical angular measure.

$$\gamma = \beta - \mu$$

Extinction angle γ. The time expressed in electrical angular measure from the end of current conduction to the next zero crossing of the idealized sinusoidal commutating voltage. γ depends on the angle of advance β and the angle of overlap μ.

STEADY STATE DC CONVERTER EQUATIONS

It is useful to express the commutation reactance of a 6 pulse converter bridge in per-unit of the converter transformer rating S_N.

$$S_N = \sqrt{2}\ U_{VN}\ I_{dN}$$

I_{dN} is the rated direct current and U_{VN} is the rated phase-to-phase voltage on the valve or secondary side of the converter transformer. Usually the DC converter bridge power rating is known from its rated DC current I_{dN} and rated DC voltage U_{dN}. The valve and converter bridge design is very dependent upon the commutation reactance X_C and so consequently its value is established and known. In modern HVDC converter bridges, it is usually in the range 0.1<XC<0.15 in per unit where 1.0 per unit is $(U_{VN})2/S_N$ ohms.

A reasonably good approximation for the power factor of a converter bridge at the AC commutating bus is given. Note that the delay angle α is usually known or determined. For example, the normal steady state range of delay angle for a rectifier may be $10° < \alpha < 18°$ and the lowest normal operating power factor will be when $\alpha = 18°$.

At a rectifier:
Power Factor
= Cos(q)
= Cos(a) - 0.5 $X_C(I_d/I_{dN})$

and at an inverter:
Power Factor
= Cos(q)
= Cos(g)- 0.5 $X_C(I_d/I_{dN})$

where I_d is the dc load current and I_{dN} is rated dc current and q is the power factor angle. For the inverter, the normal rated extinction angle is established in the converter bridge design, usually at g = 18°.

$P_d = I_d\ U_d$

where I_d is the operating direct current through the converter bridge and U_d is the operating direct voltage across the converter bridge.

$Q_d = P_d\ Tan(\theta)$

$U_{VN} = U_{dN}/[1.35\ Cos(\theta)]$

Power flow P_d through a converter bridge is determined by assuming zero losses. Reactive power requirements for a converter bridge Q_d is always inductive and is readily derived from the power factor angle θ and power P_d.

It may be that the rated phase-to-phase voltage on the valve or secondary side of the converter transformer U_{VN} is not known. It is possible to compute what it should be if the power factor $Cos(\theta)$ is known at the converter bridge rating and whose rated DC voltage is U_{dN}. Then a good estimate of U_{VN} can be determined.

Once U_{VN} is known, it is possible to find the converter transformer rating S_N.

During the operation of a converter bridge, the converter transformer on-line tap changer will adjust to keep the delay angle α at a rectifier at its desired normal operating range. Similarly, at

the inverter, the on-line tap changer will adjust to maintain the inverter operation at its desired level of DC voltage U_d or extinction angle γ. Knowing the desired levels of DC voltage (U_d), DC current I_d, the nominal turns ratio TR_N of the converter transformer, the operating level of the primary side AC voltage U_L, and the extinction angle γ (if an inverter) or delay angle α (if a rectifier), the per-unit turns ratio TR of the converter transformer can be determined.

It may be necessary to determine the overlap angle μ. At the rectifier, an approximate expression can be applied when delay angle α, per-unit commutating reactance X_C and DC load current I_d are known.

Similarly at the inverter, the extinction angle γ is usually known for steady state operation and a similar expression involving μ can be determined.

The delay angle α at the inverter may not be inherently known, but once extinction angle γ and overlap angle μ have been determined, α can easily be derived.

It is also possible to determine the nominal turns ratio of the converter transformer once the rated secondary (DC valve side) voltage U_{VN} is known and if the primary side rated phase-to-phase AC bus voltage U_{LN} is also known. Based on phase-to-phase voltages, the nominal turns ratio of the converter transformer TR_N is determined.

These equations are the steady state and reasonably accurate expressions defining the state of a 6 pulse converter bridge under ideal conditions. Defining the performance and operation of a converter bridge under dynamic or transient conditions requires the use of PSCAD/EMTDC that has the capability of modeling the valves, converter transformer, control system, the firing pulses to the valves, and the associated AC and DC networks.

SHORT CIRCUIT RATIO

The strength of the AC network at the bus of the HVDC substation can be expressed by the short circuit ratio (SCR), defined as the relation between the short circuit level in MVA at the HVDC substation bus at 1.0 per-unit AC voltage and the DC power in MW.

Shunt capacitors and AC filters connected to the AC bus reduce the short circuit level. The expression "effective short circuit ratio (ESCR)" is used for the ratio between the short circuit level reduced by the reactive power of the shunt capacitor banks and AC filters connected to the AC bus at 1.0 per-unit voltage and the rated DC power.

At a rectifier:

$$\cos(\alpha+\mu) = \cos(\alpha) - X_C \, I_d / I_{dN}$$

At an inverter:

$$\cos(\gamma+\mu) = \cos(\gamma) - X_C \, I_d / I_{dN}$$

and

$$\alpha = 180° - (\gamma + \mu)$$

Transformer turns ratio:

$$TR_N = \frac{\text{Valve side rated line voltage}}{\text{Ac side rated line voltage}} = U_{VN}/U_{LN}$$

$$TR = \frac{U_D + U_{dN}\frac{I_d}{I_{dN}} \cdot \frac{X_C}{(2\cos(\varphi) - X_C)}}{1.35 \cdot TR_N \cdot U_L \cdot \cos(\varphi)}$$

where X_C is the commutating reactance for the converter bridge in per-unit and $\varphi = \alpha$ for a rectifier and $\varphi = \gamma$ if an inverter. I_{dN} is the rated dc current for the converter bridge and U_{dN} is its rated dc voltage.

The above equations are useful in setting up the operating conditions of the converter. When operating parameters are unknown, these equations can be used to determine the converter transformer rating, the converter transformer tap setting and the operating range for firing angle α or extinction angle γ.

Usually the commutating reactance of a converter transformer is around 10 to 12% based on the transformer rating for more recent dc transmission systems, and 16 to 20% for older dc systems.

Short circuit ratio

Strong systems:	-ESCR > 3.0
Systems with Low SCR:	-3.0 > ESCR > 2.0
Weak systems with very low SCR:	-ESCR < 2.0

Lower ESCR or SCR means more pronounced interaction between the HVDC substation and the AC. AC networks can be classified in the following categories according to strength.

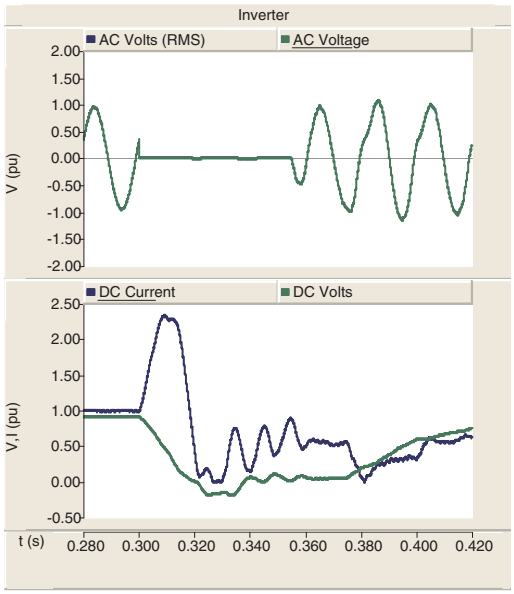
In the case of high ESCR systems, changes in the active/reactive power from the HVDC substation lead to small or moderate AC voltage changes. Therefore, the additional transient voltage control at the busbar is not normally required. The reactive power balance between the AC network and the HVDC substation can be achieved by switched reactive power elements.

In the case of low and very low ESCR systems, the changes in the AC network or in the HVDC transmission power could lead to voltage oscillations and a need for special control strategies. Dynamic reactive power control at the AC bus at or near the HVDC substation by some form of power electronic reactive power controller, such as a static var compensator (SVC) or static synchronous compensator (STATCOM), may be necessary. In earlier times, dynamic reactive power control was achieved with synchronous compensators.

COMMUTATION FAILURE

When a converter bridge is operating as an inverter as represented at the receiving end of the DC link, a valve will turn off when its forward current commutates to zero and the voltage across the valve remains negative. The period for which the valve stays negatively biased is the extinction angle γ, the duration beyond which the valve then becomes forward biased. Without a firing pulse, the valve will ideally stay non-conductive or blocked, even though it experiences a forward bias.

All DC valves require removal of the internal stored charges produced during the forward conducting period (defined by period $\alpha + \mu$ at the inverter) before the valve can successfully establish its ability to block a forward bias. The DC inverter therefore requires a minimum period of negative bias or minimum extinction angle γ for forward blocking to be successful. If forward blocking fails and conduction is initiated without a firing pulse, commutation failure occurs. This also results in an immediate failure to maintain current in the succeeding converter arm as the DC line current returns to the valve which was previously conducting and which has failed to sustain forward blocking.



Effect of a commutation failure on dc voltage and current

Commutation failure at a converter bridge operating as an inverter is caused by any of the following reasons:

1. When the DC current entering the inverter experiences an increase in magnitude that causes the overlap angle μ to increase, the extinction angle γ is reduced and may reach the point where the valve is unable to maintain forward blocking. Increasing the inductance of the DC current path through the converter by means of the DC smoothing reactor and commutating reactance reduces

the rate of change of DC current. This has the greatest effect on commutation failure onset.

2. When the magnitude of the AC side voltage on one or more phases reduces or is distorted causing the extinction angle to be inadequate as commutation is attempted.

3. A phase angle shift in the AC commutating voltage can cause commutation failure. However, the AC voltage magnitude reduction and not the corresponding phase shift is the most dominant factor determining the onset of commutation failures for single phase faults.

4. The value of the pre-disturbance steady state extinction angle γ also affects the sensitivity of the inverter to commutation failure. A value of $\gamma = 18°$ is usual for most inverters. Increasing γ to values of 25°, 30° or higher will reduce the possibility of commutation failure (at the expense of increasing the reactive power demand of the inverter).

5. The value of valve current prior to the commutation failure also affects the conditions at which a commutation failure may occur. A commutation failure may more readily happen if the pre-disturbance current is at full load compared to light load current operation.

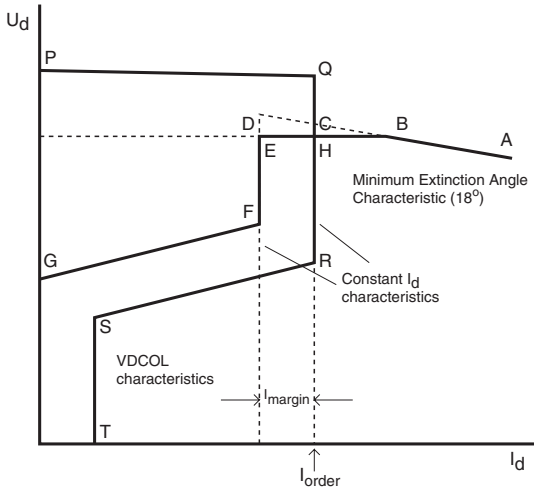
In general, the more rigid the AC voltage to which the inverter feeds into and with an absence of AC system disturbances, the less likelihood there will be commutation failures.

CONTROL AND PROTECTION

HVDC transmission systems must transport very large amounts of electric power that can only be accomplished under tightly controlled conditions. DC current and voltage is precisely controlled to affect the desired power transfer. It is necessary therefore to continuously and precisely measure system quantities that include at each converter bridge, the DC current, its DC side voltage, the delay angle α and for an inverter, its extinction angle γ.

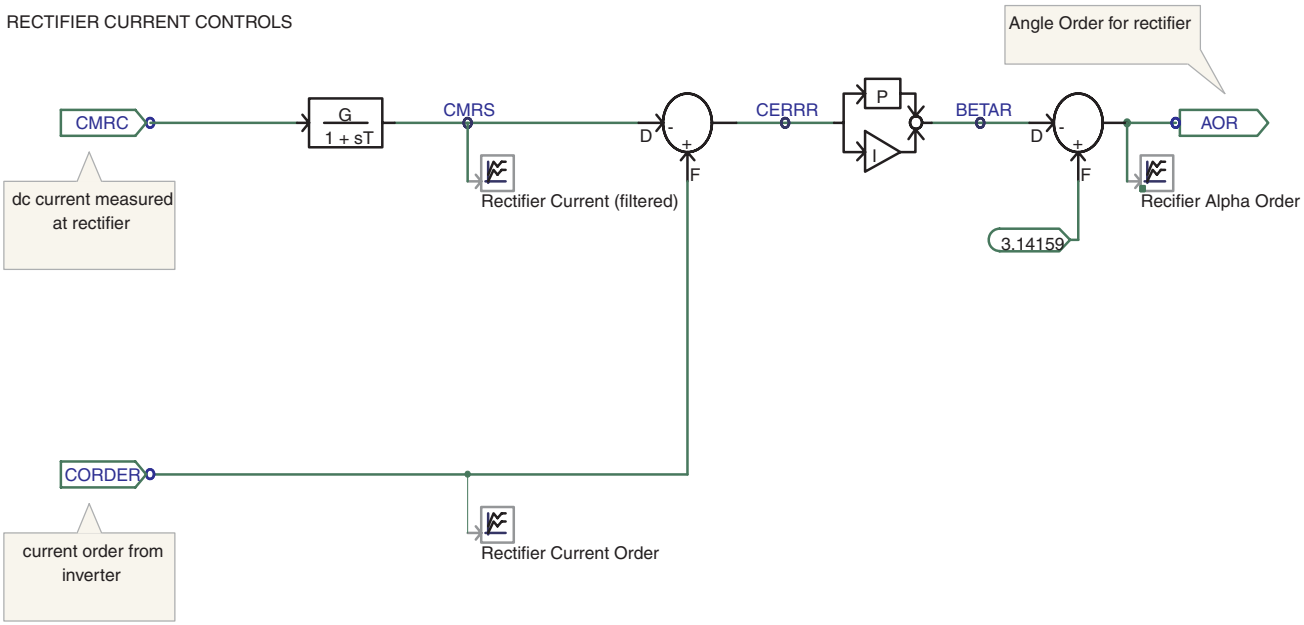
Two terminal DC transmission systems are the more usual and they have in common a preferred mode of control during normal operation. Under steady state conditions, the inverter is assigned the task of controlling the DC voltage. This it may do by maintaining a constant extinction angle γ causing the DC voltage U_d to droop with increasing DC current I_d, as shown in the minimum constant extinction angle γ characteristic A-B-C-D. The weaker the AC system at the inverter, the steeper the droop.

Alternatively, the inverter may normally operate in a DC voltage controlling mode which is the constant U_d characteristic B-H-E. This means that the extinction angle γ must increase beyond its minimum setting of 18°.



Steady state U_d-I_d characteristics for a two terminal HVDC system

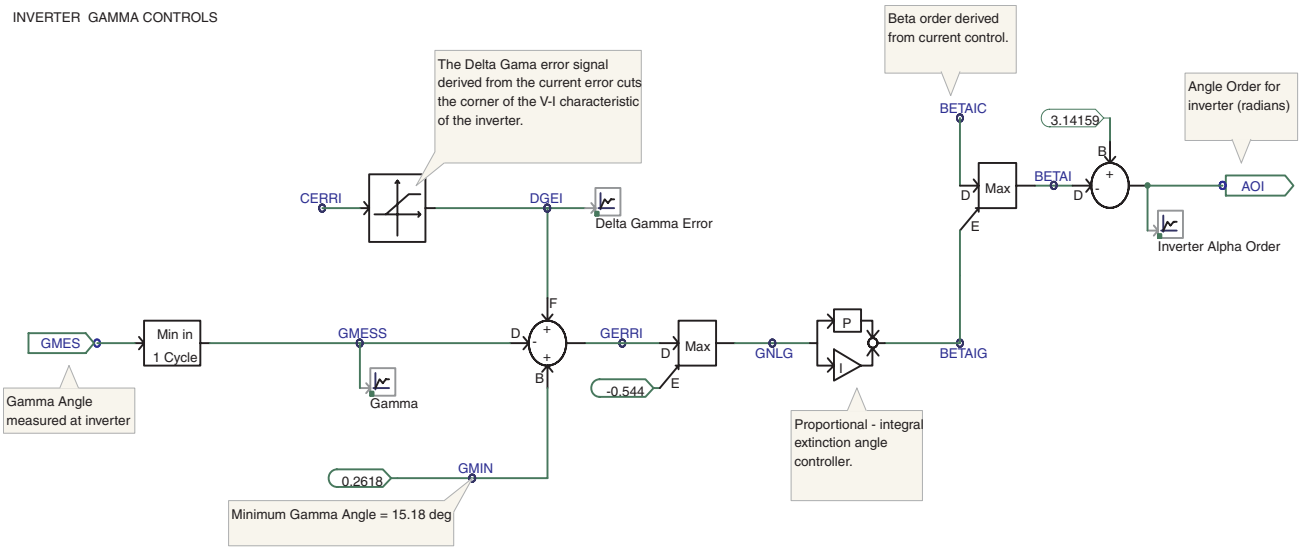
If the inverter is operating in a minimum constant γ or constant U_d characteristic, the rectifier must control the DC current Id. This it can do so long as the delay angle α is not at its minimum limit (usually 5°). The steady state constant current characteristic of the rectifier is the vertical section Q-C-H-R. Where the rectifier and inverter characteristic intersect, either at points C or H, is the operating point of the HVDC system.



The operating point is reached by action of the on-line tap changers of the converter transformers. The inverter must establish the DC voltage U_d by adjusting its on-line tap changer to achieve the desired operating level if it is in constant minimum γ control. If in constant U_d control, the on-line tap changer must adjust its tap to allow the controlled level of U_d be achieved with an extinction angle equal to or slightly larger than its minimum setting of 18° in this case.

The on-line tap changers on the converter transformers of the rectifier are controlled to adjust their tap settings so that the delay angle α has a working range at a level between approximately 10° and 15° for maintaining the constant current setting I_{order}. If the inverter is operating in constant DC voltage control at the operating point H, and if the DC current order I_{order} is increased so that the operating point H moves towards and beyond point B, the inverter mode of control will revert to constant extinction angle γ control and operate on characteristic A-B. DC voltage U_d will be less than the desired value, and so the converter transformer on-line tap changer at the inverter will boost its DC side voltage until DC voltage control is resumed.

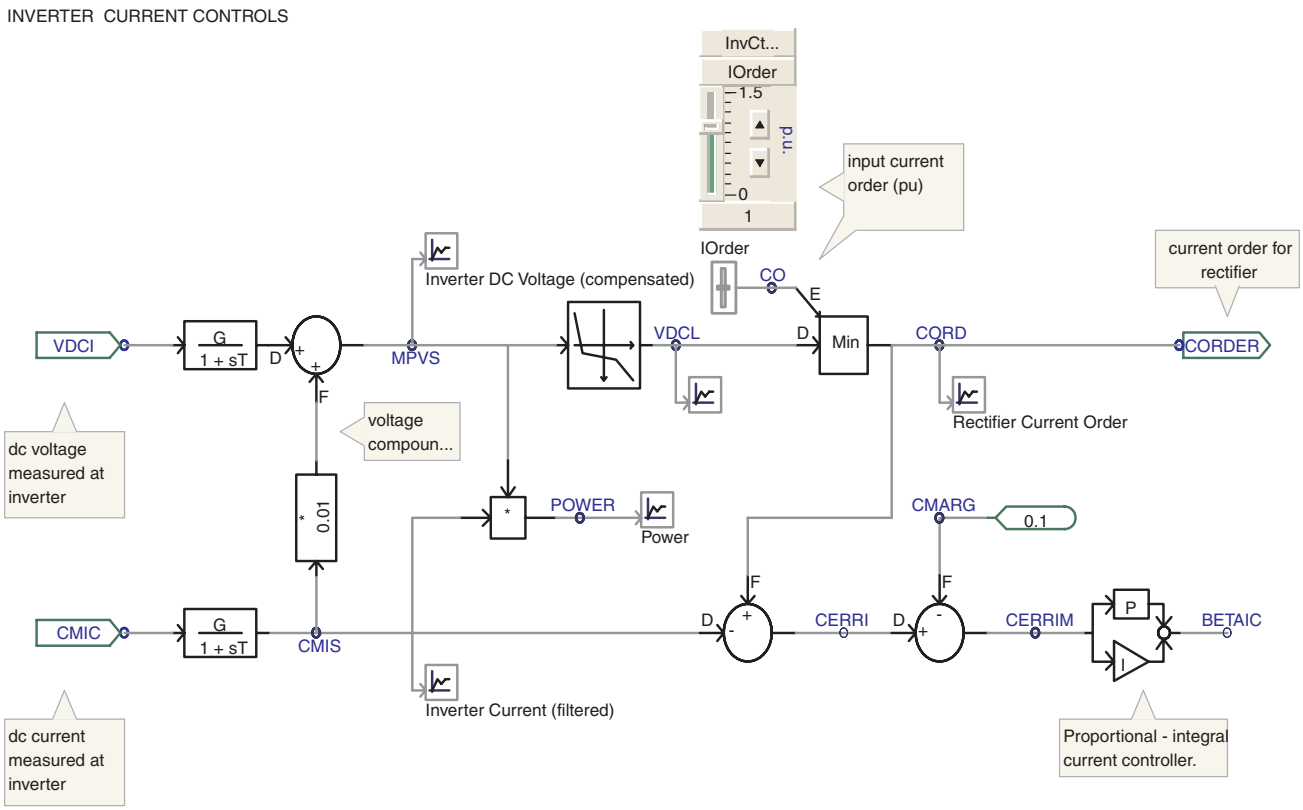
Dc Current controller using a Proportional - Integral controller to generate a firing angle that regulates the instant of valve firing of each valve.



Not all HVDC transmission system controls have a constant DC voltage control, such as is depicted by the horizontal characteristic B-H-E. Instead, the constant extinction angle γ control of characteristic A-B-C-D and the tap changer will provide the DC voltage control.

CURRENT MARGIN

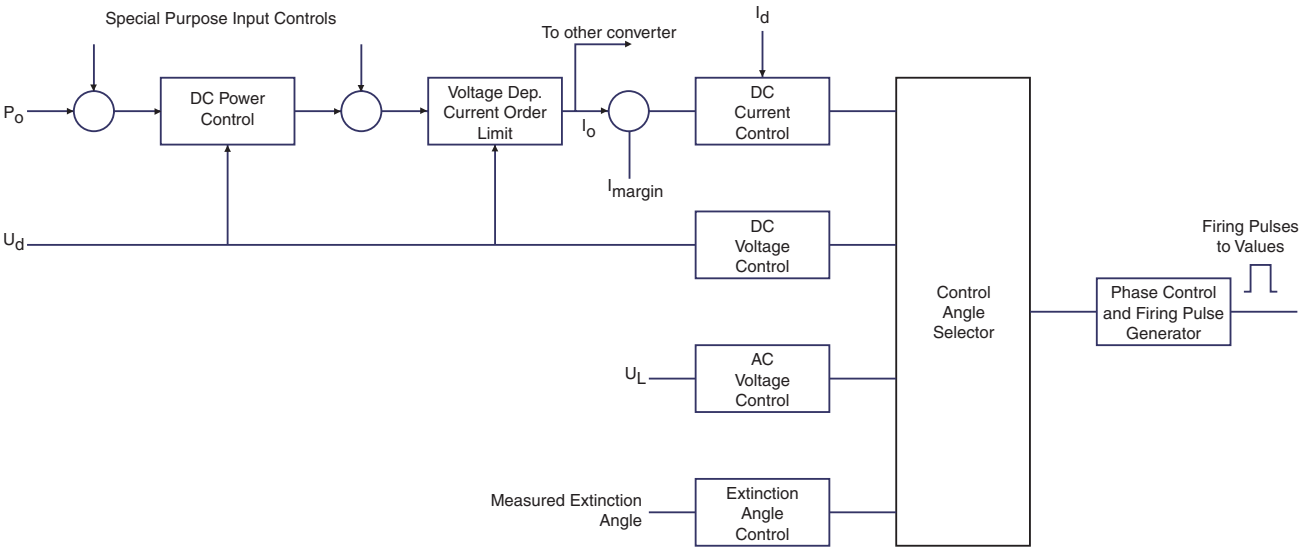
The DC current order I_{order} is sent to both the rectifier and inverter. It is usual to subtract a small value of current order from the I_{order} sent to the inverter. This is known as the current margin I_{margin}. The inverter also has a current controller and it attempts to control the DC current I_d to the value I_{order} - I_{margin} but the current controller at the rectifier normally overrides it to maintain the DC current at I_{order}. This discrepancy is resolved at the inverter in normal steady state operation as its current controller is not able to keep the DC current to the desired value of I_{order} - I_{margin} and is forced out of action. The current control at the inverter becomes active only when the current control at the rectifier ceases when its delay angle α is pegged against its minimum delay angle limit. This is readily observed in the operating characteristics where the minimum delay angle limit at the rectifier is characteristic P-Q. If for some reason or other, such as a low AC commutating voltage at the rectifier end, the P-Q characteristic falls below points D or E, the operating point will shift from point H to somewhere on the vertical characteristic D-E-F where it is intersected by the lowered P-Q characteristic. The inverter reverts to current control, controlling the DC current I_d to the value I_{order} - I_{margin} and the rectifier is effectively controlling DC voltage so long as it is operating at its minimum delay angle characteristic P-Q. The controls can be designed such that the transition from the rectifier controlling current to the inverter controlling current is automatic and smooth.



Modifying the current order with a voltage dependent current order control

VOLTAGE DEPENDENT CURRENT ORDER LIMIT (VDCOL)

During disturbances where the AC voltage at the rectifier or inverter is depressed, it will not be helpful to a weak AC system if the HVDC transmission system attempts to maintain full load current. A sag in AC voltage at either end will result in a lowered DC voltage too. The DC control characteristics shown previously indicate the DC current order is reduced if the DC voltage is lowered. This can be observed in the rectifier characteristic R-S-T and in the inverter characteristic F-G. The controller that reduces the maximum current order is known as a voltage dependent current order limit or VDCOL (sometimes referred to as a VDCL). The VDCOL control, if invoked by an AC system disturbance will keep the DC current I_d to the lowered limit during recovery which aids the corresponding recovery of the DC system. Only when DC voltage U_d has recovered sufficiently will the DC current return to its original I_{order} level.



AC VOLTAGE CONTROL

It is desirable to rigidly maintain the AC system and commutating bus voltage to a constant value for best operation of the HVDC transmission system. This is more easily achieved when the short circuit ratio is high. With low or very low short circuit ratio systems, difficulties may arise following load changes. With fast load variation, there can be an excess or deficiency of reactive power at the AC commutating bus which results in over and undervoltages respectively. When the AC system is weak, the changes in converter AC bus voltage following a disturbance may be beyond permissible limits. In such cases, an AC voltage controller is required for the following reasons:

1. To limit dynamic and transient overvoltage to within permissible limits defined by substation equipment specifications and standards.
2. To prevent AC voltage flicker and commutation failure due to AC voltage fluctuations when load and filter switching occurs.
3. To enhance HVDC transmission system recovery following severe AC system disturbances.
4. To avoid control system instability, particularly when operating in the extinction angle control mode at the inverter.

The synchronous compensator has been the preferred means of AC voltage control as it increases the short circuit ratio and serves as a variable reactive power source. Its disadvantages include high losses and maintenance that add to its overall cost. Additional AC voltage controllers are available and include:

The dc and ac voltage controls can be proportional – integral controllers. The measured voltage (dc or ac) is compared with a desired value, and if it exceeds the desired value, will become active on controlling the firing angle. Dc voltage control is usually only applied at one converter and all other converters in the same pole control dc current. Usually only one of dc current control, dc voltage control, ac voltage control or extinction angle control is active at any instant.

To minimize occurrence of commutation failure, the extinction angle control will become active if the measured extinction angle falls below the set value of 15 to 18 degrees.

The control angle selector is usually a "Select Maximum" or "Select Minimum" depending on whether the signal is for α or β.

1. Static compensators that utilize thyristors to control current through inductors and switch in or out various levels of capacitors. By this means, fast control of reactive power is possible to maintain AC voltage within desired limits. The main disadvantage is that it does not add to the short circuit ratio.

2. Converter control through delay angle control is possible to regulate the reactive power demand of the converter bridges. This requires that the measured AC voltage be used as a feedback signal in the DC controls, and delay angle a is transiently modulated to regulate the AC commutating bus voltage. This form of control is limited in its effectiveness, particularly when there is little or no DC current in the converter when voltage control is required.

3. Use of specially cooled metal oxide varistors together with fast mechanical switching of shunt reactors, capacitors and filters. The metal oxide varistors will protect the HVDC substation equipment against the transient overvoltages, and the switchings of reactive power components will achieve the reactive power balance. Its disadvantage is that voltage control is not continuous, reactive power control is delayed by the slowness of mechanical switching, and short circuit ratio is not increased.

4. Saturated reactors have been applied to limit overvoltages and achieve reactive power balance. Shunt capacitors and filters are required to maintain the reactors in saturation. AC voltage control is achieved without controls on a droop characteristic. Short circuit ratio is not increased.

5. Series capacitors in the form of CCC or CSCC can increase the short circuit ratio and improve the regulation of AC commutating bus voltage.

6. The static compensator or STATCOM makes use of gate turn-off thyristors in the configuration of the voltage source converter bridge. This is the fastest responding voltage controller available and may offer limited capability for increased short circuit ratio.

Since each AC system with its HVDC application is unique, the voltage control method applied is subject to study and design.

SPECIAL PURPOSE CONTROLS

There are a number of special purpose controllers that can be added to HVDC controls to take advantage of the fast response of a DC link and help the performance of the AC system. These include:

AC system damping controls. An AC system is subject to power swings due to electromechanical oscillations. A controller can be added to modulate the DC power order or DC current order to add damping. The frequency or voltage phase angle of the AC system is measured at one or both ends of the DC link, and the controller is designed to adjust the power of the DC link accordingly.

AC system frequency control. A slow responding controller can also adjust the power of the DC link to help regulate power system frequency. If the rectifier and inverter are in asynchronous power systems, the DC controller can draw power from one system to the other to assist in frequency stabilization of each.

Step change power adjustment. A non-continuous power adjustment can be implemented to take advantage of the ability of a HVDC transmission system to rapidly reduce or increase power. If AC system protection determines that a generator or AC transmission line is to be tripped, a signal can be sent to the DC controls to change its power or current order by an amount that will compensate the loss. This feature is useful in helping maintain AC system stability and to ease the shock of a disturbance over a wider area.

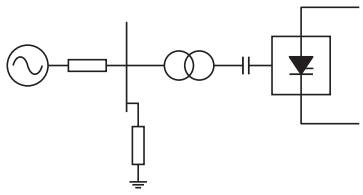
AC undervoltage compensation. Some portions of an electric power system are prone to AC voltage collapse. If a HVDC transmission system is in such an area, a control can be implemented which on detecting the AC voltage drop and the rate at which it is dropping, a fast power or current order reduction of the DC link can be affected. The reduction in power and reactive power can remove the undervoltage stress on the AC system and restore its voltage to normal.

Subsynchronous oscillation damping. A steam turbine and electric generator can have mechanical subsynchronous oscillation modes between the various turbine stages and the generator. If such a generator feeds into the rectifier of a DC link, supplementary control may be required on the DC link to ensure the subsynchronous oscillation modes of concern are positively damped to limit torsional stresses on the turbine shaft.

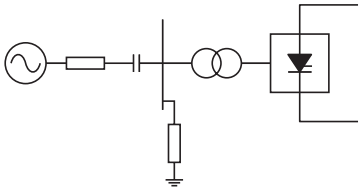
SERIES COMPENSATION OF DC CONVERTER

There are two ways series capacitors can be applied to compensate a DC converter. The capacitor compensated converter (CCC) applies a series capacitor between the converter transformer and the DC bridge. The controlled series capacitor converter (CSCC) places the series capacitor between the AC commutating bus and the AC system.

The unique aspect of the CSCC configuration is that the converter transformers may be subject to ferroresonance. This might happen following a disturbance or during recovery from a fault. The ferroresonance is remedied by protection causing the series



CCC dc transmission inverter



CSCC dc transmission inverter

capacitor to be bypassed either in part or entirely when it is detected. A thyristor controlled series capacitor (TCSC) is effective in damping out any ferroresonance. Conventional DC controls are used for a DC link with an inverter in CSCC configuration. The reactance of the series capacitor is selected at about 0.3 to 0.4 per unit (based on transformer rating). The value chosen should not cause 100% compensation of the AC system, a condition not to be tolerated.

The CCC configuration is not prone to ferroresonance. The DC link controls with CCC are also basically the same as conventional DC transmission except for the extinction angle controller. Extinction angle γ is modified and an effective value γ is defined. This is because the commutation voltage of a CCC is the sum of the AC line voltage and the voltage charge on the series capacitor. Therefore, the maximum firing angle γ is larger than that of a conventional DC inverter. A CCC inverter can operate at a higher power factor than a conventional DC converter.

With both CCC and CSCC configurations, minimum ac filtering can be applied. The filter MVAR ratings can be selected to small values (10 to 15% of rating) which result in a very narrow passband.

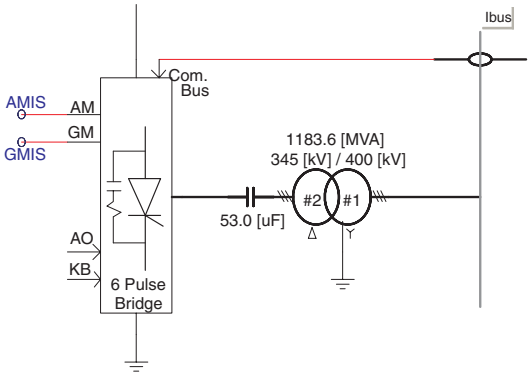
Harmonics are a little higher with CCC and CSC configurations compared to the conventional configuration.

Determining γ for the CCC configuration for a specific extinction angle is not straightforward. Use trial and error until acceptable performance is realized. Otherwise, refer to References 14 and 16 below.

In both CCC and CSCC configurations, the converter is less prone to commutation failure caused from any fault in the AC power system. The inverters with series capacitor compensation can also effectively operate into much lower short circuit ratio.

The great benefit of CCC and CSCC configurations is when DC cable transmission is used. If AC voltage at the inverter reduces for one reason or another, there is a tendency for the DC side voltage to reduce also. The cable with its large capacitance will discharge current into the inverter. When this happens with a conventional DC configuration, there is a good chance commutation failure will result causing total discharge of the DC cable. However, with CCC or CSCC configurations, the cable discharge current must flow through the series capacitor building up a back voltage to counteract it. Commutation failure is less likely to occur.

The control system for CCC and CSCC configurations can essentially remain the same as for the conventional configuration. The incentive is to apply the series capacitor at the inverter where low short circuit ratio and cable discharge effects are a challenge. It is suggested the phase locked oscillator derive its AC signals from the AC commutating busbar. For the CCC configuration, the series reactance of the capacitor can be 0.3 to 0.4 per unit based on the converter transformer rating. Note that also with the CCC configuration, the extinction angle order can be reduced to 2° to 5° instead of the normal 15° to 18°. The actual extinction angle setting to use depends upon the value for the series reactance used, as well as the degree of utilization of ratings of the transformer, series capacitor and valve group.



Connection of the phase locked loop for the CCC configuration

When either CCC or CSCC configurations are used, tests of transient overvoltages on the DC side volts, valves, the series capacitor, the converter transformer and AC busbar should be undertaken for various disturbances and protection sequences.

REFERENCES

1. IEC Committee SC22F, "*Terminology for high-voltage direct current transmission*," IEC reference number 22F/37/CDV.
2. "*Physical Layout of Recent HVDC Transmission Projects in North America*," IEEE Special Publication 87TH0177-6-PWR, September 1986.
3. R.L. Hauth, P.J. Tatro, B.D. Railing, B.K. Johnson, J.R. Stewart and J.L. Fink, "*HVDC Power Transmission Technology Assessment Report*," ORNL/Sub/95-SR893/1, Oak Ridge National Laboratory, April 1997.
4. C. Adamson, N.G. Hingorani, "*High Voltage Direct Current Power Transmission*," Garraway Limited, London, 1960.
5. W.H. Bailey, D.E. Weil and J.R. Stewart, "*HVDC Power Transmission Environmental Issues Review*," Report ORNL/Sub/95-SR893/2, Oak Ridge National Laboratory, April 1997.
6. E.W. Kimbark, "*Direct Current Transmission, Volume 1*," New York: John Wiley & Sons, 1971.
7. E. Uhlman, "*Power Transmission by Direct Current*," New York: Springer-Verlag, 1975.
8. J. Arrillaga, "*High Voltage Direct Current Transmission*," London: Peter Peregrinus Ltd., 1983.
9. K.R. Padiyar, "*HVDC Transmission - Technology and System Interactions*," New York: John Wiley & Sons, 1990.
10. "*Guide for Planning DC Links Terminating at AC Locations Having Low Short Circuit Capacities, Part 1: AC/DC Interaction Phenomena*," CIGRE Technical Brochure No. 68, 1992.
11. "*High-Voltage Direct Current Handbook*," First Edition, Palo Alto: Electric Power Research Institute, 1994.
12. "*FACTS Overview*," IEEE and CIGRE joint publication 95 TP 108, April 1995.
13. CIGRE Working Group 14-05, "*Commutation failures - causes and consequences*," ELECTRA, No. 165, April 1996.
14. J. Reeve, J.A. Baron and G.A. Hanley, "*A Technical Assessment of Artificial Commutation of HVDC Converters*," IEEE Trans. PAS, Vol. PAS-87, No. 10, 1830-1840, October 1968.

15. D.A. Woodford, "*Solving the Ferroresonance Problem when Compensating a DC Converter Station with a Series Capacitor*," IEEE Trans. Power Systems, Vol. 3, No. 2, 1325-1331, August 1996.

16. T. Jonnson and P. Bjorklund, "*Capacitor Commutated Converters for HVdc*," Stockholm Power Tech, June 1995, Proceedings; Power Electronics, pp 44-51.

17. K. Sadek, M. Pereira, D.P. Brandt, A.M. Gole, A. Daneshpooy, "*Capacitor Commutated Circuit Configurations for DC Transmission*," IEEE Transactions of Power Delivery, Vol 13, No.4, October 1998, pp 1257 – 1264.

EXERCISES

6.1 Load *Lessson6_1.psc* in Lesson 6_1. A simple monopole DC link is modeled rated at + 500 kV, 2 kA and 50 Hz. Based on the model parameters for transformer leakage reactance, determine the reactive power demand at both the inverter and rectifier when operating at rated DC voltage and current. The desired extinction angle γ at the inverter is 15 degrees and the desired firing angle α at the rectifier is also 15 degrees.

6.2 With the same DC model as Exercise 6.1, calculate the converter transformer secondary voltage required to operate the DC link at 450 kV and 2.222 kA and with both α and γ in steady state at 15 degrees.

6.3 Run case *Lesson6_1.psc* and take a snapshot at TIME = 0.5 seconds. Run from snapshot in steady state for 0.1 seconds and observe the AC voltage waveshapes at both the rectifier and inverter commutating busbars. How would you improve the waveshape? See if you are successful in doing so.

6.4 Apply a single phase to ground fault at the inverter bus at TIME = 0.51 for a duration of 0.08 seconds. Run from snapshot and observe the resulting commutation failure. Observe the magnitude of any AC and DC temporary overvoltages. Increase the impedance of the receiving end AC equivalent system by 50%. Is the case stable and is it possible to reach steady state at rated current? Why does a commutation failure occur? How can a start-up be accomplished and steady state operation be reached without a commutation failure occurring? If not, reduce the current order and re-take a snapshot at 0.5 seconds. What are the AC and DC temporary overvoltages observed during and after the AC fault and commutation failure? Are they acceptable? What is the Effective Short Circuit Ratio of the DC system?

Chapter 7:

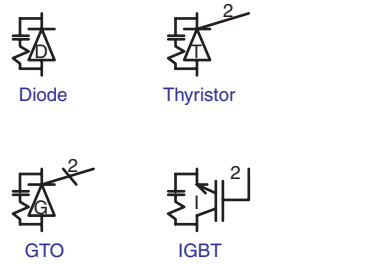
STATCOM Controls

A STATCOM is a power electronic controller constructed from Voltage Sourced Converters (VSCs). The solid state switches of VSCs, unlike the thyristor, can force current off against forward voltage through application of a negative gate pulse. Insulated Gate Bipolar junction Transistors (IGBTs) and Gate Turn-Off thyristors (GTOs) are two solid state switching devices being applied. New devices are under development and it is likely VSC technology will revolutionize distribution and transmission systems.

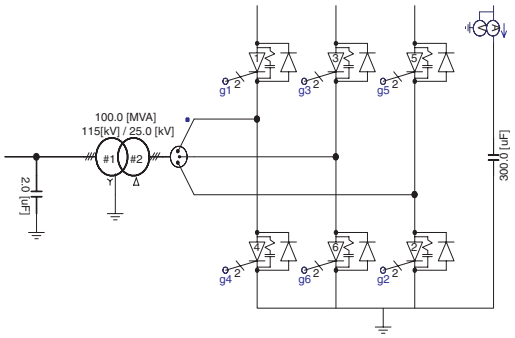
There are many possible configurations of VSCs and consequently many different configurations of STATCOMs and Distribution STATCOMs. The terms often applied to configurations are:

- Six and twelve pulse
- Two level
- Multilevel
- Pulse Width Modulation (PWM)

For understanding how to simulate, control and apply STATCOMs, simpler configurations will be covered in this section.



Switching device components in the Master Library. Note the 2 dimensional array for gate signal.



Basic configuration of a two level STATCOM. It may operate as a six pulse VSC and require significant filtering on the AC system side of the transformer, or with PWM; in which case only high frequency harmonics need be filtered, which can be achieved easily with a simple high pass filter or small capacitor bank. This is the "two level" converter configuration.

The converter transformer of a STATCOM or VSC is not subjected to the onerous duty of a DC transmission converter transformer. There is no short circuiting commutation process and mechanical stresses are no different than any other AC transformer application. In fact, in some VSC configurations, an air cored reactor is used instead of a converter transformer.

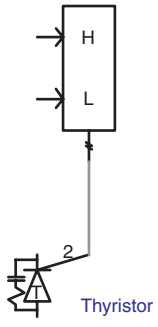
The DC side capacitor can be very large in microfarads. Being a DC capacitor (its polarity cannot be reversed), it is possible to achieve low cost and size because the dielectric can be thinner because there is no residual space charge when polarity reverses. Designing the value of the capacitor is one of the challenges of STATCOM design.

INTERPOLATED SWITCHING

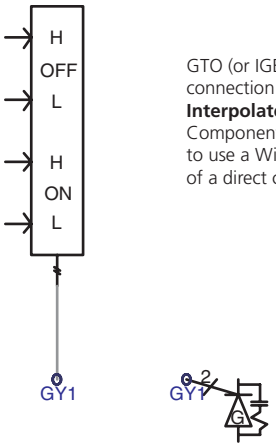
To avoid waiting until the end of a calculation time step before initiating the switching action of a solid state device, such as a thyristor or IGBT, interpolated switching is used in PSCAD/EMTDC. In many situations, such as a breaker tripping, a delay of one calculation time step (about 10 to 50 ¼sec) is of little consequence. However, in power electronic circuit simulation, such a delay can produce inaccurate results (50 ¼sec at 50 or 60Hz is approximately 1 degree phase angle). For example, simulation of VSC circuits involving GTO's with back diodes may be impossible without interpolation, very small calculation time steps or oversized snubber circuits.

EMTDC interpolates the solution between two time steps to find the solution at the exact instant of the event. This is much faster and just as accurate as reducing the time step.

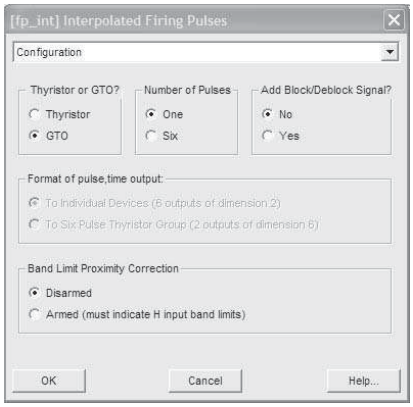
Interpolated Firing Pulse components are located in the ***CSMF*** page of the Master Library that generate the two dimensional firing pulse array as output for switching solid state devices. These components return the firing pulse and the interpolation time required for switching on and switching off for the GTO and IGBT. In other words, the output signal is a two element real array, first element is the firing pulse and the second is the time between the current



Thyristor gate connection with Interpolated Firing Pulse Component.



GTO (or IGBT) gate connection with **Interpolated Firing Pulse** Component, and the option to use a Wire Label instead of a direct connection.



Data entry sheet for **Interpolated Firing Pulse** Component. This component is expandable and can provide the gating pulse from one switching device to six switching devices in two level bridge formation.

Professor Ani Gole at the University of Manitoba has this interesting way to help understand how a STATCOM operates:

Consider a warehouse with three loading docks and trucks bringing loads into and out of the warehouse. If the trucks are coming and going on an evenly based schedule, as one truck unloads, it may be able to load directly into another truck without storing goods in the warehouse. Under such balanced conditions, the warehouse is not needed, but the loading docks are.

If the schedule is uneven and poor, the warehouse storage facilities are required until the correct truck arrives to take the goods out.

A STATCOM operates similarly. The DC side storage capacitor serves as the warehouse. With a nicely balanced AC system, the capacitor is theoretically not required. As the voltage is unbalanced for one reason or another, the capacitor storage is required to continue satisfactory operation of the compensating function of the STATCOM.

computing instant and the firing pulse transition for interpolated turn-on of the thyristors/GTOs.

The Interpolated Firing Pulse component returns the firing pulse and the interpolation time required for interpolated switching. It also uses a zero-crossing detector to detect when the signal **H**IGH goes above the signal **L**OW. The turn-on transition of the firing pulses is synchronized to the input **ON** signal (**H**IGH-**L**OW) while the turn-off transition is synchronized to the input **OFF** signal (**H**IGH-**L**OW). The transition of the pulse happens in the time step following the zero-crossing of the corresponding signal.

USE OF PAGES

Since VSC configurations and controls can appear visually complex, there is provision in PSCAD to embed them in their own Page Modules, which for controls, is not unlike grouping functions onto one printed circuit card. The procedure for doing this is covered in section 5 of the PSCAD User's Guide, or in the PSCAD on-line help.

STATCOM CONTROL STRATEGY

There is advantage to using pulse width modulation at VSC converters as two parameters can be independently controlled. These are the magnitude and the phase of the ac voltage generated on the VSC side of the interfacing reactor or transformer to the AC system.

Any voltage sourced converter, such as a STATCOM with PWM, has two independent parameters it can control. These are:

1. The magnitude of the fundamental frequency component of the AC voltage on the converter side of the converter transformer or reactor.

2. The phase angle of the fundamental frequency component of the AC voltage on the converter side of the converter transformer or reactor.

With a STATCOM, there are many ways to control the magnitude and phase quantities. In simple terms, the magnitude control can be used to control the voltage of the AC system, and the phase angle control can be applied to control the DC capacitor volts. It is straight forward to understand how the magnitude control can effect AC system voltage. Phase angle control is less easy to understand. As the phase angle of the voltage on the converter side of the converter transformer or reactor is changed with respect to the phase of the AC system volts, it will attempt to generate or absorb real power from the AC system. If real power is brought in from the AC system, it has to go somewhere, and it ends up charging up the DC side capacitor. Likewise, if the STATCOM sends power to the AC system, it can only come from the DC side capacitor, and so it discharges. In this way, phase angle control

is the means to regulate the DC capacitor voltage. This is the "direct" control used in *Exercise 7.3* below.

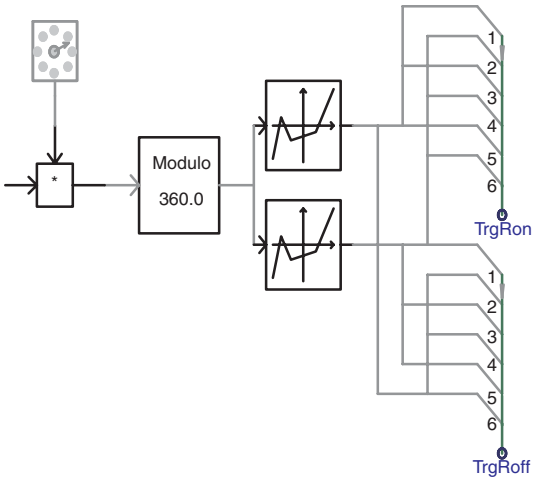
The "indirect" control approach, applied in *Exercise 7.2* below is to leave the DC side capacitor voltage uncontrolled, and apply just phase angle control for AC voltage control.

Just control of reactive power is accomplished in *Exercise 7.1* below. PWM is not applied.

There is a wide range of control strategies that can be applied to a STATCOM in terms of adjusting the effective magnitude and phase of the voltage created on the converter side of the converter transformer or reactor. These may contain considerations for:

- Use of q-axis current as a controlled parameter
- Multi-pulse converters
- Multi-level converters

The detailed assessment of all control and configurations possible is outside the scope of this introductory course.



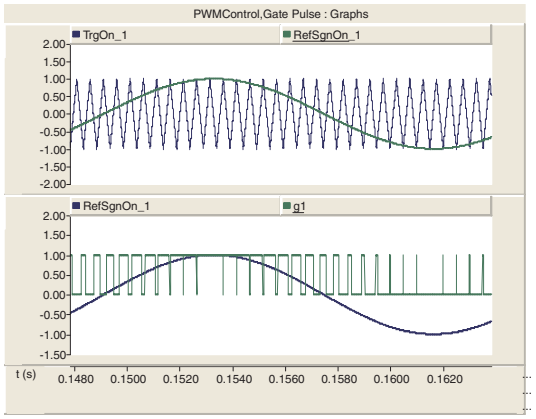
Phase A 0-360° ramp converted to PWM frequency, triangular signal between -1 to +1 and allocated to each valve for both interpolated switching turn-on and turn-off.

COMPONENTS OF CONTROLS

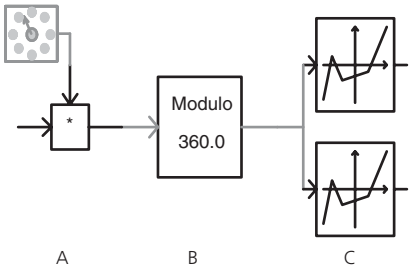
PWM applied to the valves of the VSC causes the valves to switch at high frequency, which practically may reach 2000 Hz or even greater.

Phase Locked Oscillator

The phase locked oscillator (PLL) plays a key role in synchronizing the valve switching to AC system volts. In the STATCOM example case provided with *Example 7.3* below, there are two PLL functions.



First, there is a PLL with a single 0-360 degrees ramp locked to phase A at fundamental frequency that is used to generate the PWM triangular carrier signal. Its frequency is multiplied to the PWM switching frequency, and converted to a triangular signal whose amplitude is fixed between –1 to +1. If the PWM frequency is divisible by three, it can be applied to each IGBT valve in the two level converter.

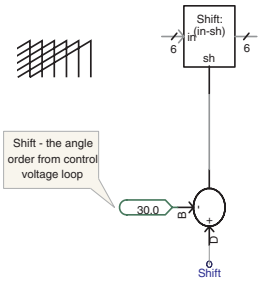


Carrier signal generation:

A. Increase PLL ramp slope to that required by carrier frequency.
B. Restrains ramps to between 0 and 360° at carrier frequency.
C. Converts carrier ramps to carrier signals.

Secondly, the 0-360 degrees ramp signals generated by the six pulse PLL are applied to generate Sin curves at the designated fundamental frequency. The two degrees of freedom for "direct" control are achieved by:

1. Phase shifting the ramp signals which in turn phase shift the Sin curves (signal "Shft"), and
2. Varying the magnitude of the Sine Curves (signal "mr" or "mi").



The input ramp array signals from the PLL are phase shifted 30 (for the star-delta phase shift of the interface transformer), as well as by control input signal "Shft."

It is the control of signals "Shft" and "mr" (or "mi") that define the performance of a voltage sourced converter connected to an active AC system.

Generating the Firing Pulses

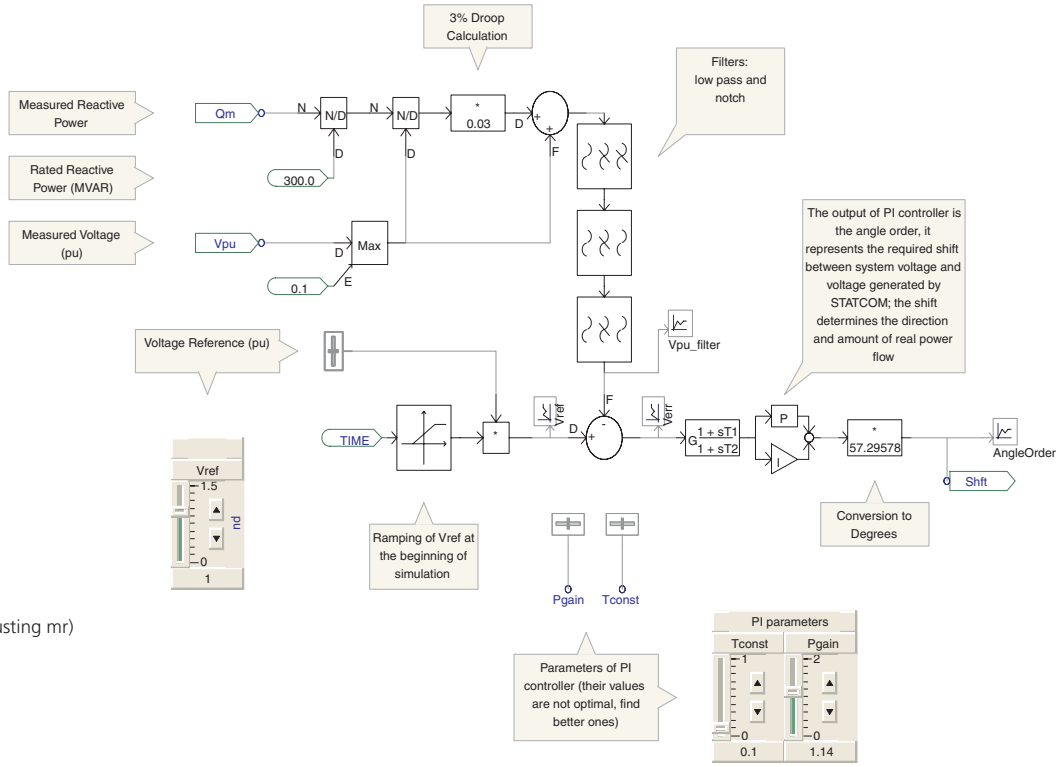
The PWM technique requires the mixing of the carrier signal with the fundamental frequency signal defining AC wave shape. In this example, a Sin wave is used being the simplest signal to apply. In reality, more efficient switching for optimum harmonic cancellation can be used but requires increased complexity in defining times to switch gate pulses and is not included here.

With GTO or IGBT valves, gate pulses are applied to switch off as well as switch on. In PSCAD/EMTDC, it is preferable to model both switch-on and switch-off pulses with interpolated firing so that the exact instance of switching between calculation steps is achieved. Greater precision is therefore possible without resorting to very short calculation time steps (and long simulation times).

The PWM carrier signal is compared with the Sin wave signals and both turn-on and turn-off pulses are generated for interpolated switching. Care is required to ensure pulsing and sequencing of the turn-on and turn-off pulses are correct.

Control of AC Voltage or Reactive Power

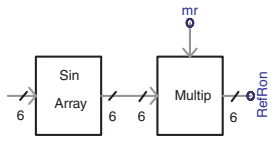
A simple proportional-integral (PI) controller can be applied to regulate AC side voltage or alternatively, reactive power into or out of the voltage sourced converter. The output of the PI controller adjusts the "mr" signal to achieve this controlling function. The signal "mr" or "mi" is known as the "modulation index."



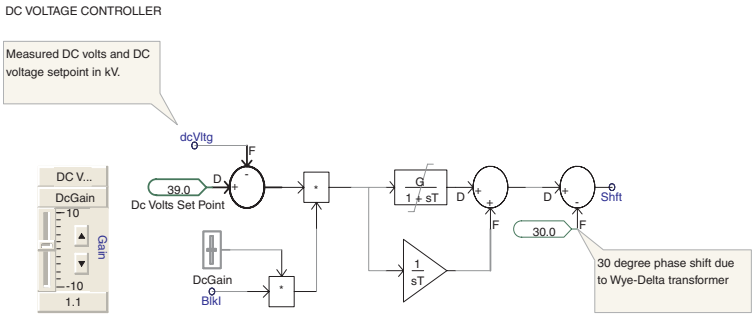
AC voltage direct control (adjusting mr)

Control of DC Side Volts

Maintaining the DC side volts of a STATCOM for "direct" control is achieved by controlling charge on the large storage capacitor located on the DC side of the voltage sourced converters. A simple PI controller can control power flow by adjusting phase shift angle "Shft." This is demonstrated from the example case in *Exercise 7.3* below.



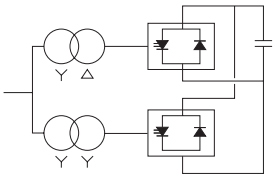
The ramps are converted to Sine waves and their magnitudes are controlled by "mr" input signal.



DC voltage control of STATCOM DC side capacitor

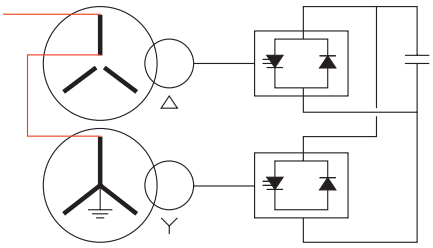
MULTIPULSE STATCOM

The model studied above has the converter configured in the basic 6 pulse bridge arrangement. Two 6 pulse bridges can be configured in the classical 12 pulse arrangement similar to what is done in 12 pulse HVDC converters. However, the DC side is connected in parallel rather than series to keep the voltage on the DC side as low as possible and to improve utilization of the DC side capacitor. The 5th and 7th harmonic currents are cancelled but do circulate in the windings adding to the winding and converter valve ratings. If PWM is also applied, the number of switchings per quarter cycle (chops) can be approximately halved for the same harmonic effect into the AC system.



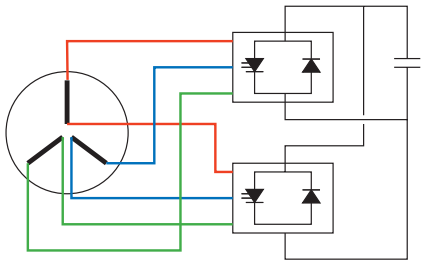
Conventional 12 pulse configuration

To eliminate the 5th and 7th harmonics on the transformer primary side and hence a reduced rating for the valve equipment, the primary side star windings are connected in series.



12 pulse transformer configuration with primary star windings connected in series to cancel 5th and 7th harmonics and preventing them from circulating in the secondary side and valves.

The transformer is used to create the necessary phase shifts of the 6 pulse converter bridges to eliminate harmonics. A "quasi multi-pulse arrangement" can approximate the phase shift by delaying the firing pulses to one of the 6 pulse units by the appropriate delay angle. This does not completely eliminate the AC side harmonics but can considerably reduce them.



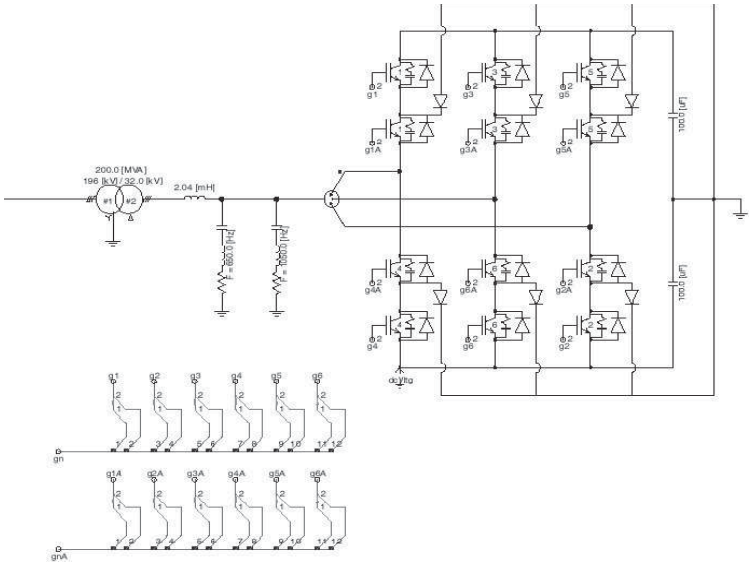
Quasi 12 pulse arrangement

Transformer connections are simplified for the quasi multi-pulse arrangement. The concept can be expanded for 24 and 48 pulse configurations. The higher the pulse configuration, the lower the frequency in PWM needed. Indeed for 48 pulse and possibly 24 pulse as well, PWM may not be required at all for acceptable AC side harmonic performance. This saves in valve switching losses but increases the complexity of the transformers (magnetics).

THREE LEVEL STATCOM

In the multi-level converter, the DC bus is split into intermediate levels. The three level voltage sourced converter arrangement is a practical configuration. Harmonic reduction is achieved without any special transformer connections. However, not all valves see the same duty and some are underutilized.

Three level converters can also be configured in multi-pulse arrangement to minimize the PWM switching frequency for equivalent harmonic cancellation. For comparison, a two level, 6 pulse converter with PWM will require about twice the switching frequency to achieve the same level of harmonic effect as a three level converter.

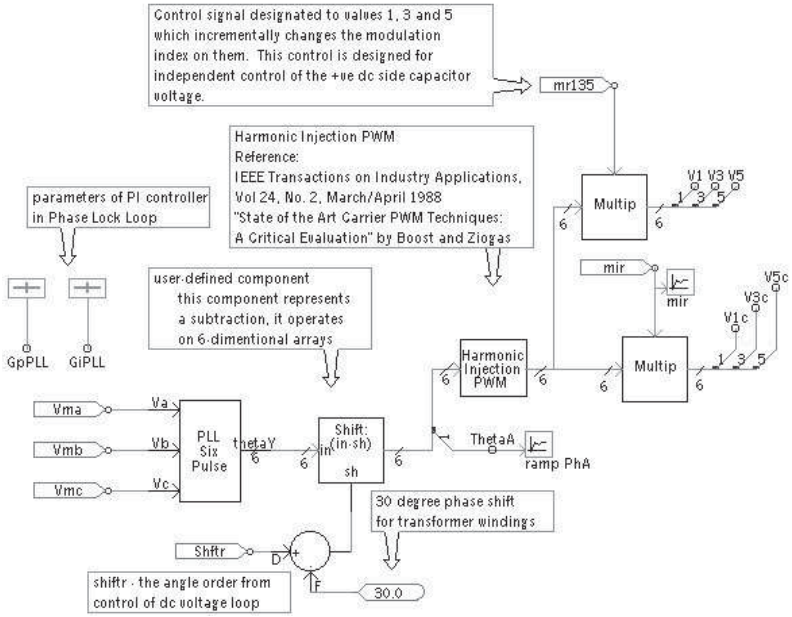


Three level voltage sourced converter for a STATCOM. Interpolated firing pulses are also shown.

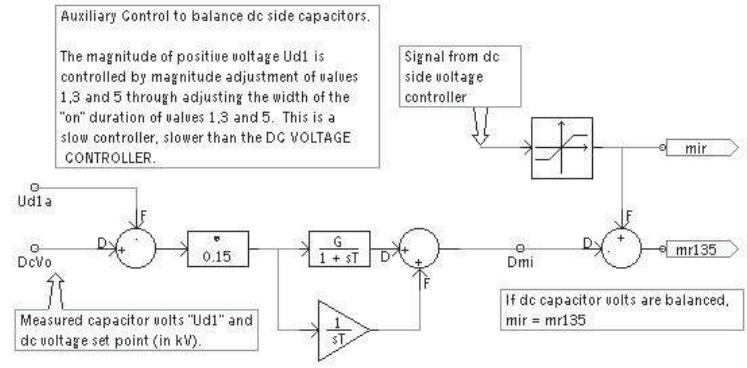
For the case where the PWM switching frequency is at the 21st harmonic, some minimal filtering at that harmonic and twice that harmonic may be required to achieve an acceptable level of performance. The step up transformer can be located between the valves and the filters, but the filters would then be connected at a higher voltage. The transformer may or may not be applied to replace the air cored inductor also located between the valves and the filters.

It is important to note that for the multi-level configuration, the secondary side transformer winding cannot be grounded (as can the two level converter in some instances). An undesired circulating current between the valves and the converter may result.

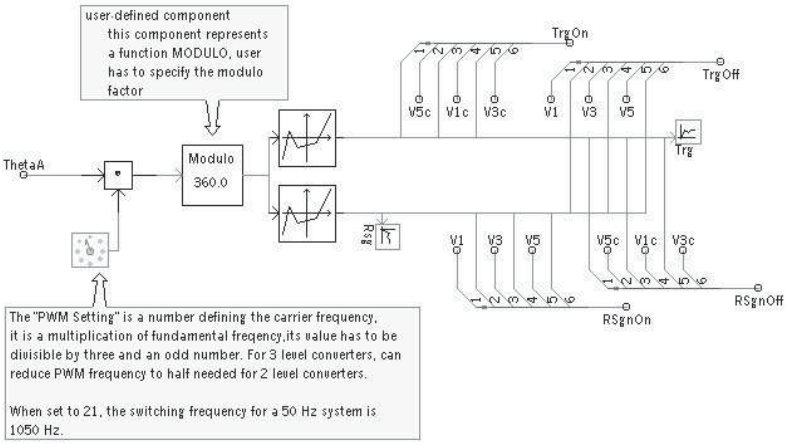
In a practical three level converter, the DC side capacitors are grounded at the mid-point. It is important to implement controls that balance the voltage on each capacitor. This is accomplished by a judicious valve firing arrangement. The valve firing logic is a difficult exercise to set up.



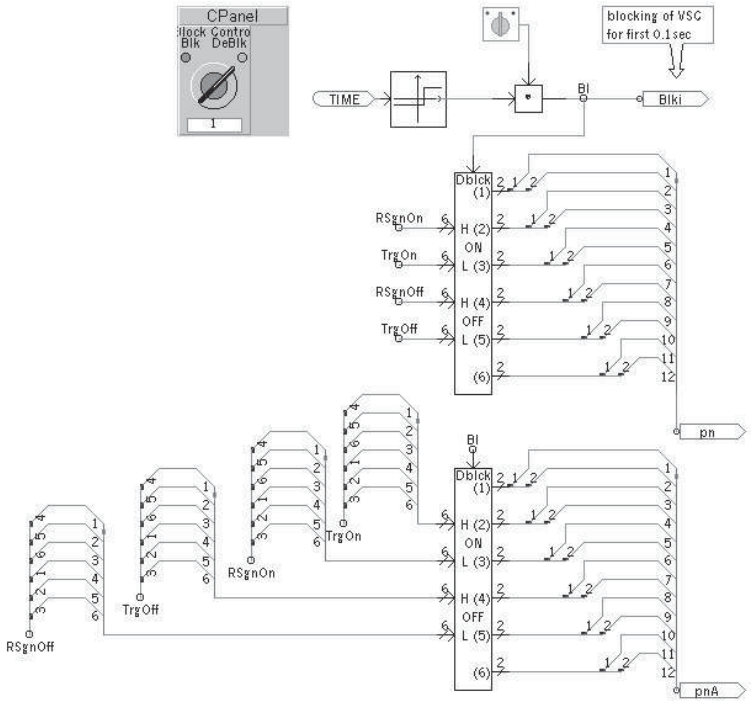
Phase locked loop, harmonic injection PWM and capacitance voltage balancing control for three level voltage sourced converter. Inputs include modulation index signals mir and mr135, phase shift signal Shftr and the three phase voltages of the phase locked oscillator.



Auxilliary control to balance DC side capacitors



Interpolated firing pulse coordination. Input signal ThetaA is derived from the phase locked loop. The triangular wave carrier signal is generated to formulate the TrgOn, TrgOff, RsgnOn and RsgnOff triangular wave signals, modified by the DC capacitor balancing signals V1, V3 and V5.



Pulse firing logic for three level voltage sourced converter.

Improved Harmonic Performance

It is possible to improve the efficiency of pulse width modulation by optimally ordering the valve switching to minimize the number of switchings for maximum harmonic elimination. A number of different methods are available. A simple method is the Third Harmonic Injection PWM. This is the injection of a 17% third harmonic component into the original fundamental frequency sin reference waveform. The analytical expression for the reference waveform is:

$$Y = 1.15 \sin(\omega t) + 0.19 \sin(3\omega t)$$

Another method is the Harmonic Injection PWM Technique which is very similar to the third harmonic injection technique. The analytical expression is:

$$Y = 1.15 \sin(\omega t) + 0.27 \sin(3\omega t) - 0.029 \sin(9\omega t)$$

Both these methods although easy to implement, do generate DC side third harmonic currents.

A more complex method is to determine the exact instant of switching for each chop. This is a complex process requiring advanced calculations and interpolated look-up tables to implement practically.

REFERENCES

1. N.G. Hingorani and L. Gyugyi, "*Understanding FACTS – Concepts and Technology of Flexible AC Transmission Systems*," IEEE Press, New York, 2000.

2. A.M. Gole, M. Reformat, "*Topology and Control of STATCOM Devices in Power Systems*," (Contact A. Gole at gole@ee.umanitoba.ca).

3. Boost and Ziogas, "*State of the Art Carrier PWM Techniques: A Critical Evaluation*," IEEE Transactions on Industry Applications,Vol 24, No. 2, March/April 1988.

EXERCISES

7.1 Load *Lessson7_1.psc* in Lesson 7_1 which a 12 pulse STATCOM example. It has a balanced 3 phase fault applied at 1.5 seconds which lasts for 0.5 seconds. This case maintains constant reactive power. Determine that it is operating without PWM. Examine the waveshape of the terminal voltage. Add the on-line Fourier component and measure the harmonics of the terminal voltage while running in steady state. Are the observed harmonics as expected?

7.2 Load *Lesson7_2.psc* in Lesson 7_2 which is a 6 pulse STATCOM operating with PWM with the same fault as Exercise 7.1 above. Run the case and observe the terminal voltage waveshape and compare with the terminal voltage waveshape from Lesson7_1.psc. Note the differences. Observe the response of the AC voltage control. Observe the maximum DC voltage when the fault is cleared. Apply a low impedance 1L-G fault instead of the three phase fault and observe performance. What happens if the DC side capacitor is increased 5 times?

7.3 Load *Lesson7_3.psc* in Lesson 7_3 which is similar to Lesson7_2.psc but there is DC voltage control added. Adjust some of the gains and time constants in the controls by trial and error and see if improved voltage control performance of both the AC and DC voltages can be achieved. Can the peak DC voltage on clearing of the three phase fault be improved?

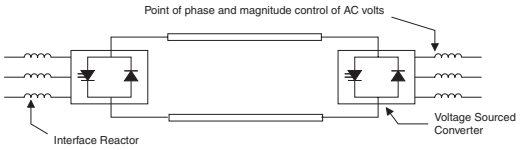
Chapter 8:

VSC Transmission

Voltage Sourced Converter Transmission (VSC Transmission) became a reality when ABB introduced their "HVDC Light" transmission concept. IEEE and CIGRE have designated that the generic term VSC Transmission be applied. It can be used in back-to back configuration (the Eagle Pass 36 MW interconnection between Mexico and Texas) or point-to-point 180 MW transmission (the "DirectLink" interconnection between Queensland and New South Wales). Siemens have now introduced HVDCPLUS as a VSC Transmission product.

G. Asplund, G. Ericksoon, K. Svensson, "*DC Transmission based on Voltage Source Converters*," CIGRE SC14 Colloquium in South Africa, 1997.

The benefits of VSC Transmission are indeed significant. Each converter can independently control AC voltage, and there is no need for any existing short circuit capacity in the receiving end AC network. The DC side voltage can never reverse polarity and so significant benefits are achieved if the underground or undersea cables are used since the cable size can be quite small, and hence lower cost, comparatively speaking.



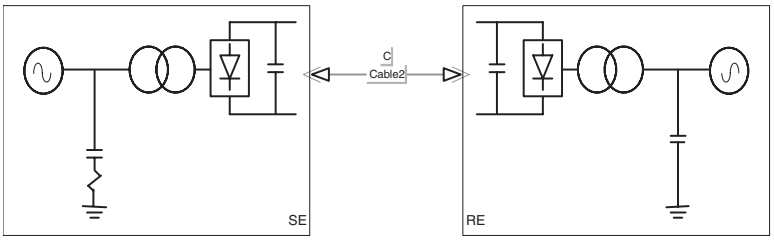
Simplified diagram of VSC Transmission

VSC TRANSMISSION CONTROL STRATEGY

There is advantage to using pulse width modulation at VSC converters that have two parameters to be independently controlled. These are the magnitude and the phase of the AC voltage generated on the VSC side of the interfacing reactor or transformer to the AC system. One successful control strategy for VSC transmission when located in a system with AC voltage at each terminal is proposed by controlling the VSC side AC voltage at each converter as follows:

At one VSC with pulse width modulation (PWM):

- DC link power is controlled by phase shift control.
- AC system voltage is controlled by magnitude control.



Voltage sourced converter for VSC Transmission. Six-pulse, two level bridge with PWM

At the other VSC with PWM:

- DC link voltage is controlled by phase shift control.
- AC system voltage is controlled by magnitude control.

COMPONENTS OF THE CONTROLS

The key factor with any VSC is the control of the magnitude and phase of the AC voltage on its AC terminals. PWM applied to the valves of the VSC causes the valves to switch at high frequency, which practically may reach 2000 Hz or even greater. The PSCAD example cases low_vltg_hvdc.psc and VSCTran.psc are used for demonstration.

Note: Case low_vltg_hvdc.psc feeds to a dead load and its receiving end converter has to provide frequency and voltage to that load which could be an isolated load with no operating source of generation. Case VSCTran.psc transmits electric power between two active AC systems, such as an interconncection.

Phase Locked Oscillator
The phase locked oscillator (PLL) plays a key role in synchronizing the valve switching to AC system voltage. For the controls applied to the example case VSCTran.psc, two PLLs are applied at each converter.

The PLL with the single 0-360 degrees ramp locked to phase A at fundamental frequency is used to generate the PWM triangular carrier signal. First, its frequency is multiplied to the PWM switching frequency, and converted to a triangular signal whose amplitude varies between –1 to +1. If the PWM frequency is divisible by three, it can be applied to each IGBT valve in the 6-pulse converter.

The ramp signals generated by the 6-pulse PLL are applied to generate Sin curves at the designated fundamental frequency. Two degrees of freedom in control are achieved by:

1. Phase shifting the ramp signals which in turn phase shift the Sin curves (signal "Shft"), and
2. Varying the magnitude of the Sine Curves (signal "mr").

It is the control of signals "Shft" and "mr" that define the performance of a voltage sourced converter connected to an active AC system.

When Receiving End is a Passive AC System
When the receiving end AC system is passive with no generators defining voltage and frequency, these functions must be performed by the Voltage Sourced Converter. The phase locked loop must be synchronized to an oscillator defining fundamental frequency instead of from the AC bus voltage. It is meaningless to change the phase of the load AC voltage through the "Shft" signal, so it is not used. However, the "mr" magnitude signal can be used to control the magnitude of the AC load voltage.

The sending end voltage sourced converter for this case functions as a rectifier. Here, the "mr" signal can be used to control AC bus volts at the rectifier, and the "Shft" signal to control DC side volts (see example case *low_vltg_hvdc.psc*).

Generating the Firing Pulses

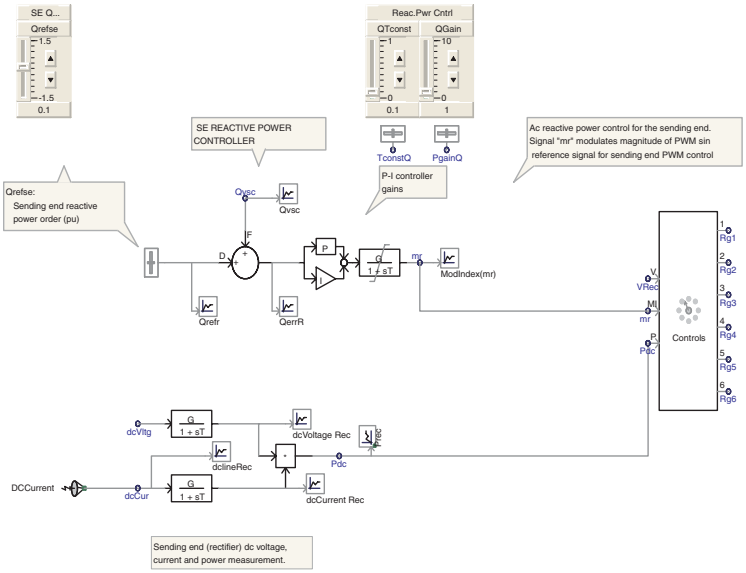
The PWM technique requires the mixing of the carrier signal with the fundamental frequency signal defining AC wave shape. In this example a Sin wave is used being the simplest signal to apply. In reality, more efficient switching for optimum harmonic cancellation can be used but requires increased complexity in defining times to switch gate pulses and is not included here.

With GTO or IGBT valves, gate pulses are applied to switch off, as well as switch on. In PSCAD/EMTDC, it is preferable to model both turn-on and turn-off pulses with interpolated firing so that the exact instance of switching between calculation steps is achieved. Greater precision is therefore possible without resorting to very short calculation time steps (and long simulation times).

The PWM carrier signal is compared with the Sin wave signals and both turn-on and turn-off pulses are generated for interpolated switching. Care is required to ensure pulsing and sequencing of the turn-on and turn-off pulses are correct.

Control of AC Voltage or Reactive Power

A simple proportional-integral (PI) controller can be applied to regulate AC side voltage or alternatively, reactive power into or out of the voltage sourced converter. The output of the PI controller adjusts the "mr" signal to achieve its controlling function.

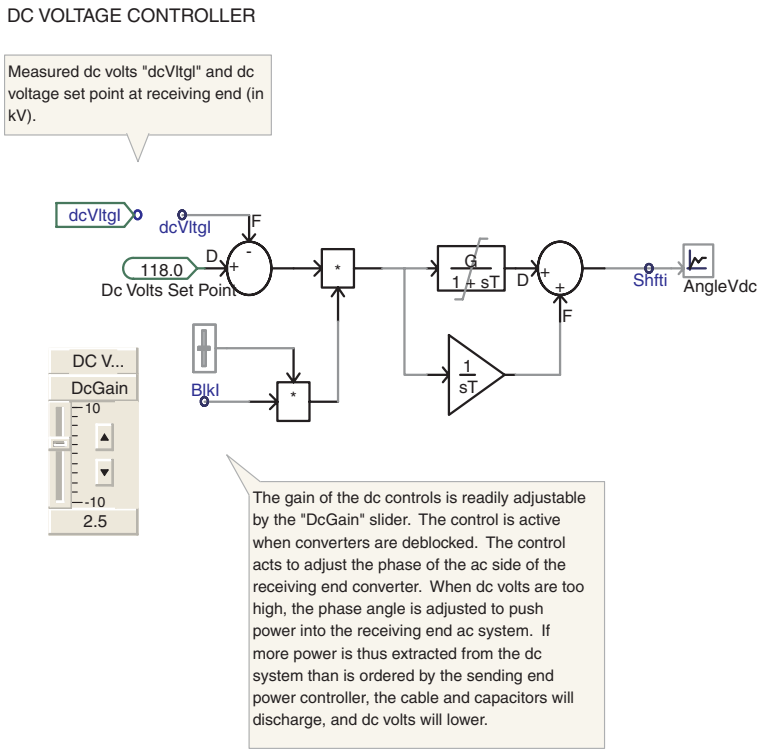


In this example, the PI controller is responding to measured reactive power and is adjusting the "mr" signal to achieve the set reactive power. Such a control might be used where AC voltage is being controlled by other means (eg, a voltage regulator).

Control of DC Side Volts

Maintaining the DC side volts of VSC Transmission is achieved by controlling charge on the large capacitors which are located on each side of the voltage sourced converters. At one of the converters, power flow into or out of the converter can be regulated to keep DC voltage constant on the capacitors. A simple PI controller can control power flow by adjusting phase shift angle

"Shft" which for the inverter is renamed "Shfti." This is demonstrated from example case VSCTran.psc as follows:



Power Control

If the "Shfti" phase shift signal is used to control DC voltage by controlling power into or out of the receiving end inverter, the other available "Shft" signal at the sending end VSC can be applied to control total power flow. Each of these controls varies the phase difference of the AC voltage across the interface transformer using the AC system side voltage as the reference through its PLL.

The receiving end phase shift control maintains charge on the DC side capacitors by adding to or subtracting from the power ordered through the VSC Transmission from the sending end phase shift control.

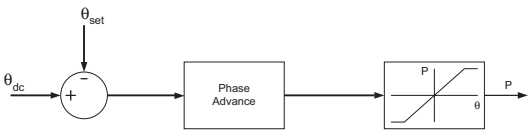
If the receiving end VSC feeds a passive load, the load itself determines the power flow through the VSC Transmission. This is accomplished simply by applying the DC voltage control at the sending end converter. Then, any load demanded at the receiving end will automatically be available.

Note: If the VSC Transmission line is bi-directional, there is no need to change the various control functions from one end to the other.

P_o = Power order to DC controls

θ_{set} = Phase angle setting

θ_{dc} = AC phase angle across DC line



Concept of DC transmission synchronizing controls. Power flow control through VSC Transmission is achieved through adjustment of phase angle setting θ_{set}.

VSC TRANSMISSION WITH AC CHARACTERISTICS

DC transmission systems usually operate asynchronously. By adding an enhancement to controls, power through VSC Transmission can be made to respond to AC system phase angle, thereby emulating an AC transmission line.

The relative phase angle of the AC voltage at each end of the VSC Transmission must be measured and the effective angle across the line θ_{dc} must be computed. Modern telecommunication systems are required to compare the AC voltage phase angles at each end. It is beneficial to have high speed telecommunications with minimum transmission delay to reduce the degree of phase advance needed.

Example case *VSCTran.psc* incorporates controls to emulate AC transmission characteristics.

Phase Angle Measurement

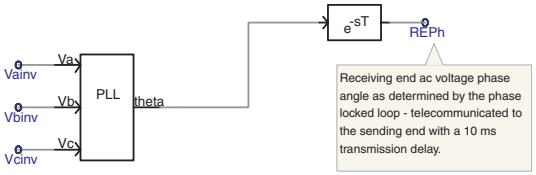
To effect power control as a function of AC phase difference across the VSC Transmission, the first step is to measure and compare the difference in phase angles.

The phase angle with respect to phase A is derived from the PLL at each end. Now the power controller would be physically located at one end, so there would be a transmission delay to receive the phase angle signal measured from the other end. In this example, a ten millisecond transmission delay is assumed.

A component in the main library of PSCAD measures phase angle between two sets of three phase signals. Its limitation is that once the range of ±180° is exceeded, the measured phase is discontinuous. For a more rugged controller, continuous measurement beyond ±180° is needed.

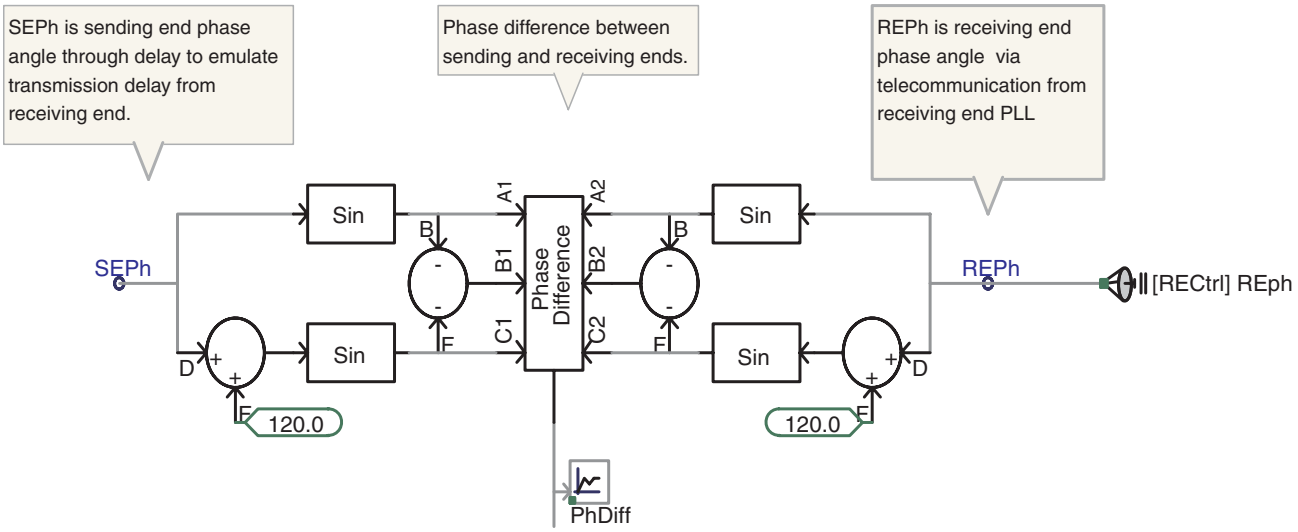
References on DC transmission with AC characteristics:

- D.A. Woodford, Wang X., M. Reformat, A. Gole, "*Enhancement of Power System Stability with Synchronous DC Links*," Paper 230-6, Proceedings of CIGRE Symposium Kuala Lumpur 1999.
- Wang, X., D.A. Woodford, "*Long Distance DC Transmission with AC Transmission Characteristics*," Proceedings of the International Conference on Power System Technology, October 18-21, 1994, Beijing.
- D.A. Woodford, Wang, X., "*Synchronous Operation of Adjacent Power Systems*," Proceedings of the International Conference on Power System Technology pp 914-917, August 18-21, 1998, Beijing.



AC phase angle measurement undertaken similarly at the sending end.

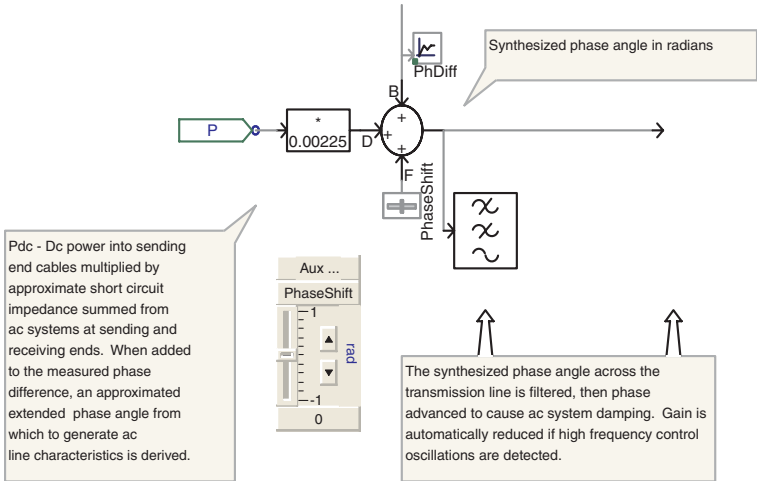
Open Loop Power Flow Controller



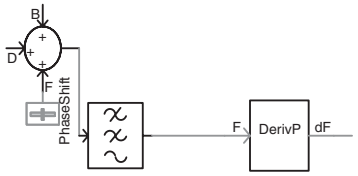
Measuring phase angle difference of AC voltages at sending and receiving ends.

To achieve a stable phase angle to use for power control, the measured phase angle difference is supplemented by an estimate of the extended phase angle taking into account the power flow out of and into the AC systems at each end.

Measured DC power (MW) at the sending end is multiplied by a factor of the approximate short circuit impedance summed from AC systems at sending and receiving ends divided by AC voltage squared (Ω/kV^2). When added to the measured phase difference, an approximate synthesized phase angle from which to generate AC line characteristics is derived.



Summation of measured phase angle difference plus the extension approximated by the product of measured DC power and AC short circuit capacity, plus any desired manual phase shift adjustment.

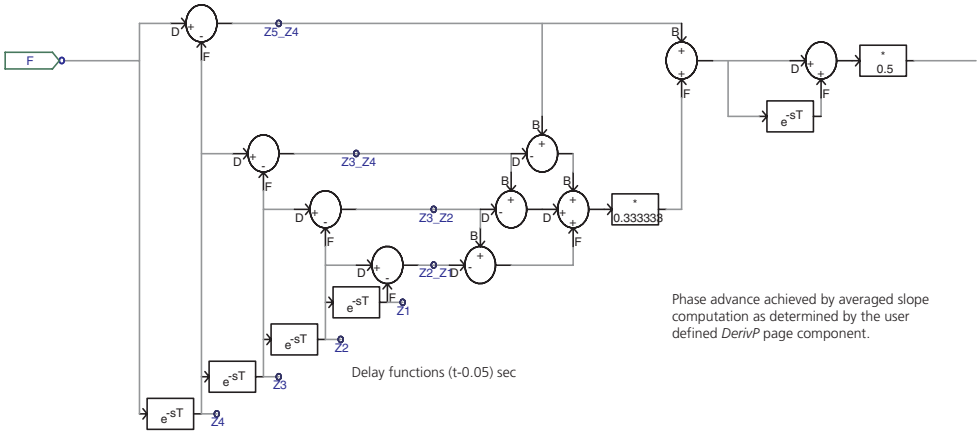


Synthesized phase angle difference is first filtered with a low pass 2nd order filter, then phase advanced once or twice with the *DerivP* page component.

Phase Advance of Synthesized Phase Angle

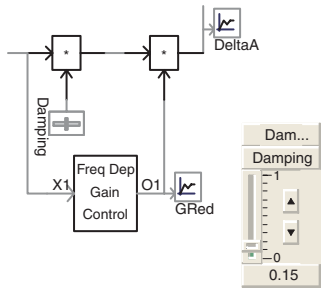
It is necessary to add phase advance to the synthesized phase angle difference to compensate measurement and transmission delays. If phase advance is not added, electromechanical system swings will become unstable.

Since it is the relatively slow electromechanical swings (0.1 to 2 Hz) that must be damped, a special phase advance component was designed to do this. It is represented by PSCAD page components *DerivP*. If the *DerivP* page component is opened, the phase advance can be observed:



One problem evident with the phase advance, is that negative damping may be exhibited at higher frequencies (10 Hz or greater). A control is devised which detects such oscillations and applies an automatic gain reduction. The user defined page component *Freq Dep Gain Control* is used.

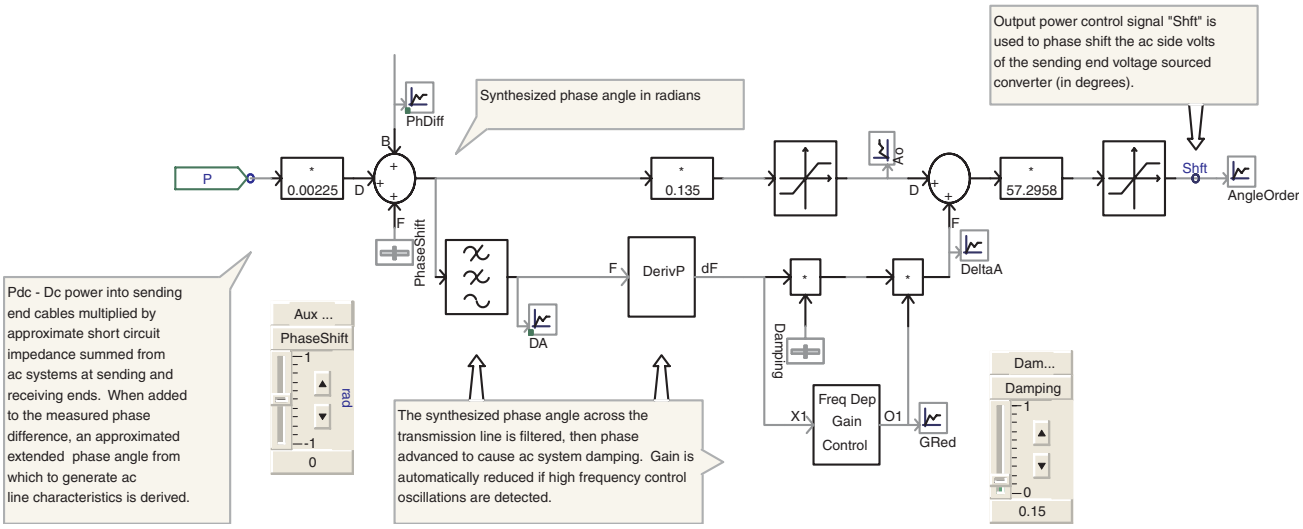
For very low electromechanical frequencies (less than 2 Hz), the frequency dependent gain control multiplier is 1 or near 1. For the higher less damped frequencies, the frequency dependent gain control multiplier approaches or equals 0.0.



Automatic gain reduction if frequency of input signal becomes large and exhibits negative system damping.

Controlling Power from Synthesized Phase Angle

Power flow through the VSC Transmission is generated from the synthesized phase angle if AC transmission characteristics are desired. To achieve fastest power order response, an open loop control is used where phase angle "Shft" is varied proportionally with the synthesized phase angle. A suitable gain is needed, which in this example is selected at 0.135. This means that for every radian change in synthesized phase angle, the voltage phase angle across the interface transformer at the sending end converter "Shft" changes 0.135 radian. This gain can be set by trial and error to reflect the rating of the VSC Transmission and the AC line characteristic desired.

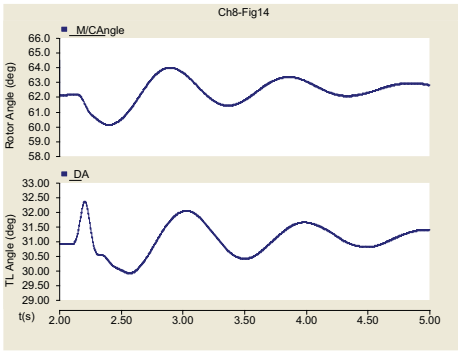


VSC Transmission control to emulate AC line characteristics

Example Fault Case

A single line-to-ground fault is applied in the receiving end AC system near the VSC inverter for example case VSCTran.psc.

Note: Two DerivP page components instead of one will increase damping of electromechanical oscillations.



EXERCISES

8.1 For the single-line-to-ground fault applied in the receiving end AC system for example case *VSCTran.psc*, explain why the sending end generator rotor angle first swings negative on application of the fault.

8.2 For example case *VSCTran.psc*, delete the VSC Transmission controller used to emulate AC transmission line characteristics. Add a manual power controller to control power. This can be done using a "Slider" component from the CSMF functions in the Main library of PSCAD. An appropriate gain must be calibrated so that the power ordered by the "Slider" adjusts the "Shft" signal to provide approximately the same power flow as ordered. Observe how effectively and quickly power can be reversed from full one way to full the other way.

Example case VSCTran.psc is selected to take a snapshot at two seconds. Restart from the snapshot in steady state. Note,the receiving end single line-to-ground fault is applied at 2.1 seconds (or 0.1 second after the snapshot). This can be changed if desired.

8.3 For example case *low_vltg_hvdc.psc*, there is no provision for DC voltage control. Determine how this can be achieved and add it in and test it. Apply a single-line-to-ground fault at the receiving end load and determine how effective the added DC voltage controller is.

8.4 Design a protection system against a fault to ground on one phase of the valve side terminal of the interface transformer.

Chapter 9:

Model Verification

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Even if the best simulation software is adopted in a study, simulation results are only as good as the data that was used. This chapter is an extension of the PSCAD Sources section in Chapter 2, and addresses methods to verify correctness of the data used to compile a network model for an Electromagnetic Transient (EMT) study.

Normally, network studies are performed in the following order:

As a start, a load flow study is done to solve a network's steady state requirements. The load flow models and solutions are verified against measured load flow data typically available from the utility.

Secondly, a short circuit analysis of the network is performed to determine the equipment's current withstand and control requirements. Some utilities have transient fault recordings available that can be used to verify the results of short circuit analysis.

When required, a frequency analysis of the network is conducted to determine the power quality, harmonic stresses on equipment, or possible resonance conditions. Harmonic voltage and current measurements in the network can be performed to verify the frequency analysis results.

Lastly, EMT studies are performed to calculate possible switching and lightning stresses that the network can impose on equipment and visa versa.

Utilities spend a lot of effort verifying their system load flow and short circuit data, as this is an important consideration for planning, operation and protection of the system.

EMT MODEL VERIFICATION METHODS

For an EMT study, it is usually not necessary to model the complete network. For lightning transients, only the substation busbar and a few spans of the connecting power lines are required. When performing switching transient studies, only the portion between the point of interest and say one or two busbars away need to be modeled, since the transient will propagate for only short distances into the network. In contrast with switching transients, slow transients and power swings can propagate far into the network. Furthermore, it is important to understand the effect that network loading has on transient simulation results. For example, if voltage stresses on a surge arrester are calculated, load flow conditions do

not have a material impact. On the other hand, if the Transient Recovery Voltage stresses on a breaker are calculated, the current flowing through the breaker is very important. The type of study that is to be performed and the required accuracy level determine the minimum information that needs to be included in the network model.

The following steps are suggested in building and verifying a network in PSCAD:

- Determine the composition of the network that will be simulated in PSCAD and calculate parameters of the equivalent Thevenin sources that will represent 'extraneous' parts of the network not explicitly included in the network model.
- Compile the network in PSCAD and check for healthy network voltages at various busbars to avoid short circuits, open circuits and gross parameter errors.
- Run PSCAD to steady state condition and compare the results with measured load flow, voltage magnitude and angle values and/or simulation results obtained with other load flow programs.
- Determine the three-phase as well as single-phase short circuit currents at various busbars in the network and compare them with existing values.

Alternatively, a frequency scan at different busbars of the network can be done to determine the corresponding impedances (driving-point impedances). The fundamental frequency values can then be compared to existing short circuit values. Note that in a weak network the impedances do not always correspond 100% with short circuit values.

If your network passed the above verification tests, it is ready for EMT simulations.

The following sections elaborate on how to build a network and perform all the above tests. The advantage of using one network for all the tests is that it reduces testing time and the possibility of introducing data errors.

NETWORK COMPILATION

The reader is recommended to follow a section-by-section approach while building the network and to regularly test (run) the network to ensure that the network solves and that the data is entered correctly. There is nothing more frustrating than building a big interconnected network in one-step and finding at the end that something is incorrect or not working. The frustration is that it is very difficult to locate a problem or to distinguish between a decimal error in the data entered. Similarly, it is very difficult to find a line transposition error, which can cause voltage collapse on one or all phases. By using the section-by-section approach, the

reader can not only resolve problems as soon as they arise, but can also get a good feel for the characteristics and behavior of different parts of the network.

Most of the study cases found in handbooks consist of only one or two sources and loads that are inter-connected with minimum number of power lines. This is a good approach when trying to convey a specific concept or simulation technique. However, a simple network as the one described above is in reality quite rare, since most networks are heavily interconnected on various voltage levels and/or along different corridors. It is therefore important to establish the correct cut-off, or equivalence points in the network in order to produce results that accurately reflect behavior of the real network. For example, when studying power swings that result in over voltages on series capacitor banks, it is important to model both the series compensated power line and any parallel path(s) that might exist in order to get the correct flow of power. The reason for this is that the voltage across the series capacitor is directly related to the power flowing through the bank. If the parallel paths are not modeled, the simulations could give unrealistic results, i.e. the results can be either too high or too low.

As a rule of thumb, it is a good approach to terminate the network at a single generator, at a bus where there is a pool of generators, or at a busbar that acts as a node in the network without any parallel path. When terminating the network at a generator, the approach is easy and the actual generator and generator transformer data can be entered in the PSCAD case file. When the network is terminated in such a fashion that an equivalent source is required, two methods can be used to determine the equivalent Thevenin impedance:

1) Use a Load Flow program (the equivalencing function) to automatically calculate network impedance and interconnected impedance values between different termination points, or

2) In the load flow, switch out all those lines that will be modeled explicitly in PSCAD, i.e. all the lines that will be retained in PSCAD. Then, obtain the short-circuit currents at all the termination points in the network and calculate the equivalent Thevenin impedance values from the short-circuit currents that were obtained. Note that this option does not accurately represent any interconnections that may exist between different termination points, however, in most cases it gives a good, adequate equivalent network.

Example

From the network shown in Figure 1, consider the line between BUS2 and BUS4 to be series compensated (see also Figure 2 below). The study to be conducted includes both switching and fault analysis. The data of the complete network is listed in Table 2 at the end of this chapter.

Step 1: Determine the points where the network will be terminated (equivalanced). To perform switching studies, we need to include frequency dependant models for the lines up to at least one busbar position away from the line of interest. Therefore, BUS1, BUS2, BUS4 and BUS7 (see Figure 1) must be included as a minimum. When considering the strong parallel path through BUS5, BUS5 should also be included together with the associated lines that comprise the parallel path, i.e. the lines to BUS1 and BUS7. We select the network termination points to be BUS1, BUS5 and BUS7. The generator at BUS1 will therefore have to be modeled explicitly while equivalent Thevinin sources are to be connected at BUS1, BUS5 and BUS7.

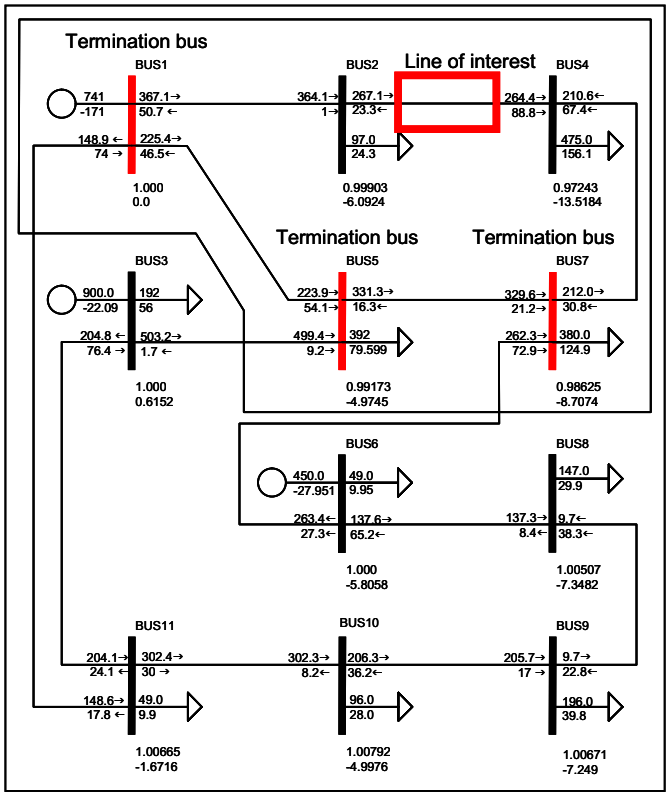


Figure 1 - Complete network

Step 2: Determine the equivalent network impedances at BUS1, BUS5 and BUS7. PSSE has an equivalencing routine (SCEQ) that can be used to calculate the equivalent generator, load, shunt impedance and interconnected line values at the various busbars where the network is to be terminated (equivalenced), as shown in Figure 2. At BUS1, the original generator and the equivalent generator can be represented with one generator by calculating the parallel impedance. Table 3 lists the network data after applying the SCEQ equivalencing routine in PSSE.

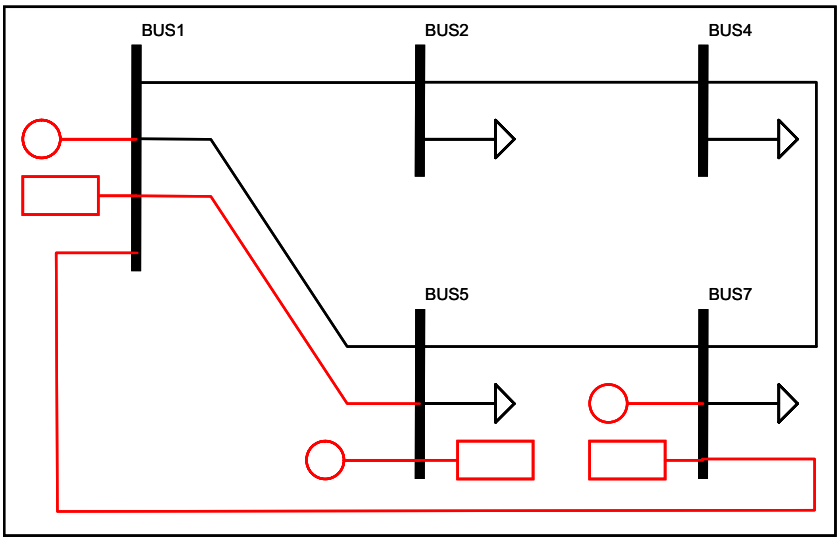


Figure 2 - Equivalent network

If the SCEQ equivalencing routine is not available, a simple equivalent network, as shown in Figure 3, can be manually approximated from the short circuit data. Using the load flow program, the user can switch out all the lines and generators that will be explicitly modeled in PSCAD; for example, LINE12, LINE15, LINE24, LINE47 and LINE57 and perform the short circuits at buses BUS1, BUS5 and BUS7. The short-circuit values at these busbars will represent the fault current contributions from the equivalence parts of the network, and are represented as Thevenin generators with corresponding source impedance values in the PSCAD case. This approach does not always produce 100% correct results in PSCAD as short-circuit currents are limited to individual sources and might need some adjustment of the source impedance values.

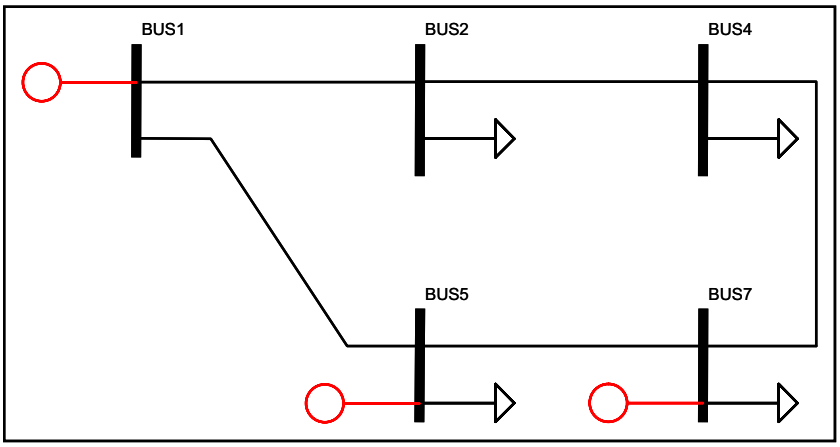


Figure 3 - Simple equivalent network

LOAD FLOW

It is easy to build a network using the section-by-section approach and to test it with a load flow simulation. The section-by-section approach involves construction of the network by starting at a source and adding small sections of the network at a time. After a small section is added each time, the network should be compiled and solved to ensure that voltage waveforms and power flows are correct. If the voltage on one or more phases is depressed outside normal line coupling unbalance, the network should be investigated for a short circuit analysis. To simplify the building of networks in PSCAD, a custom Model Verification library is provided, including components like Source Controllers, Voltage magnitude and angle displays, Power Flow displays and Loads. As shown in Figure 4, a load component can be connected at the end of a line, and the real and reactive power flowing through the line can be monitored and compared to pre-set target values during the run. This is achieved through application of the source controllers that adjust voltage magnitude and angle of each source.

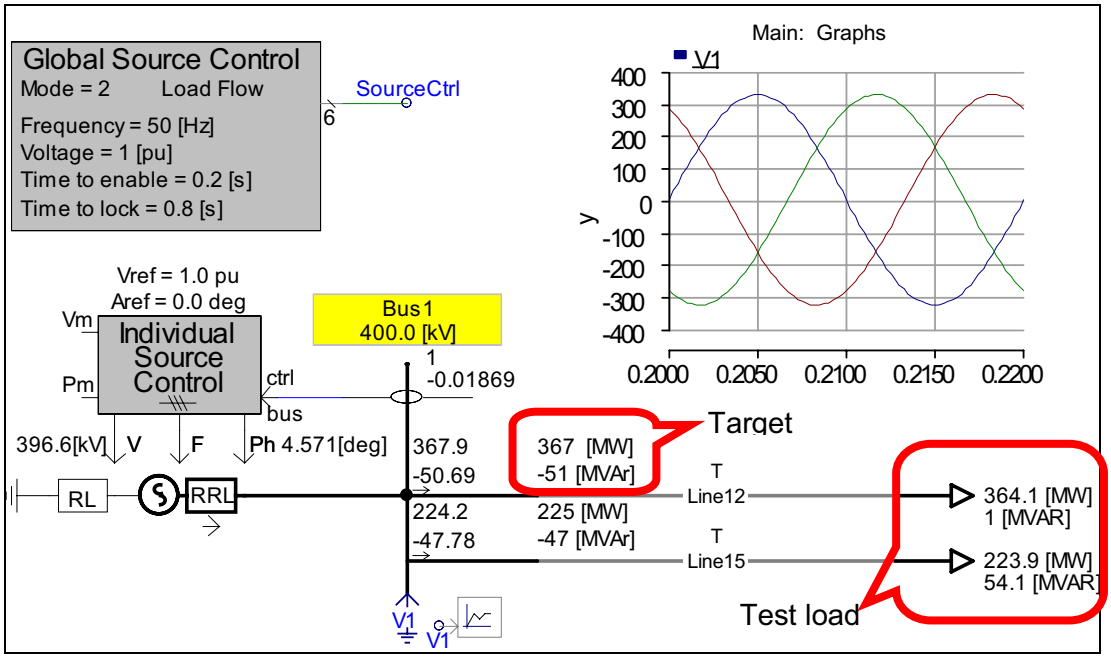
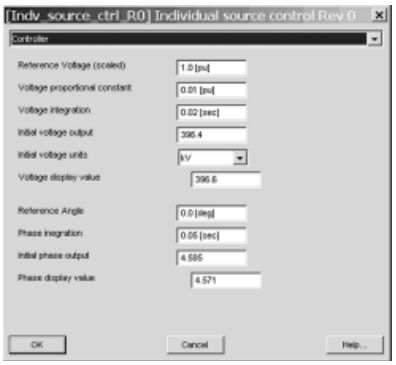


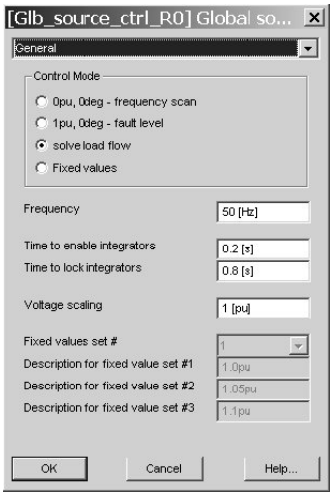
Figure 4 - Section-by-section network building

Source Control

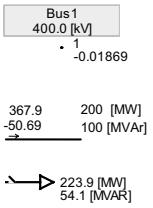
The Individual Source Control manipulates voltage magnitude and angle of a standard source. It has the same function as the built-in automatic voltage control of a source, but offers more control modes. After a simulation run, voltage and angle values that are displayed can be copied and used as the initial values for the next run. This allows the source to start with correct magnitude and angle.



The Global Source Control block manipulates the outputs of the Individual Source Control blocks. If the Global Source Control is set to Frequency Scan, the magnitude and angle of all the sources are set to zero. In this way, only the source impedance remains in circuit and a harmonic current injection simulation can be done. The Fault level mode sets voltage magnitude of all the sources to 1.0 pu and the angle to 0 deg. This is suitable to perform short-circuit current calculations. When the Global Source Control is set to Solve Load Flow, all the sources will automatically match the magnitude and angle from the load flow (e.g. done beforehand in PSSE) that is entered in the Individual Source Control. The automatic calculation utilizes an integrator that requires time to reach a solution. While the sources ramp-up, the integrators are locked and are only released when the network reaches the steady-state condition. In most cases, a time of 0.2 s is sufficient. Depending on the network configurations, the integrators can be locked once they match the load flow magnitude and angle values. A network event like a fault must be performed with locked integrators. A voltage-scaling variable can be used to change the voltage magnitude of all the sources simultaneously. The Fixed Value Set allows the voltage magnitude and angle of up to three different load flows stored in the Individual Source Control blocks. By selecting a fixed value of 1 to 3, the sources can be set to the corresponding voltage magnitude and angle.



The Busbar label component has the functionality to measure and display RMS values of voltage and angle at a busbar.



The Power Flow display incorporates a target value and a margin together with color coding index to identify problem areas in a network. If the measured real or reactive power is outside the specified margin, it will be highlighted as follows: red, if it is too high and green if it is too low.

The fixed load component consists of a series connected resistor together with an inductor or a capacitor. The component parameters are calculated from the power flow values entered. The fixed load can be switched out of circuit while it is still displayed on the graphical interface. The direct scaling function can be used to easily change the rating of the load on a percentage basis. The load can also be scaled according to voltage level where the load rating is available at the actual voltage; for example, 1.02 p.u.

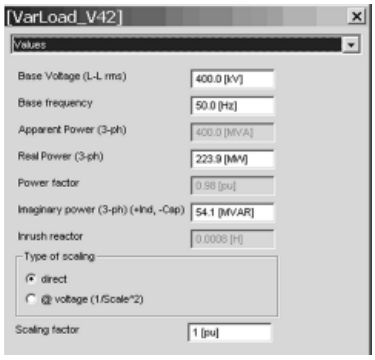


Figure 5 shows how the Model verification components are incorporated into the network (also see Figure 3).

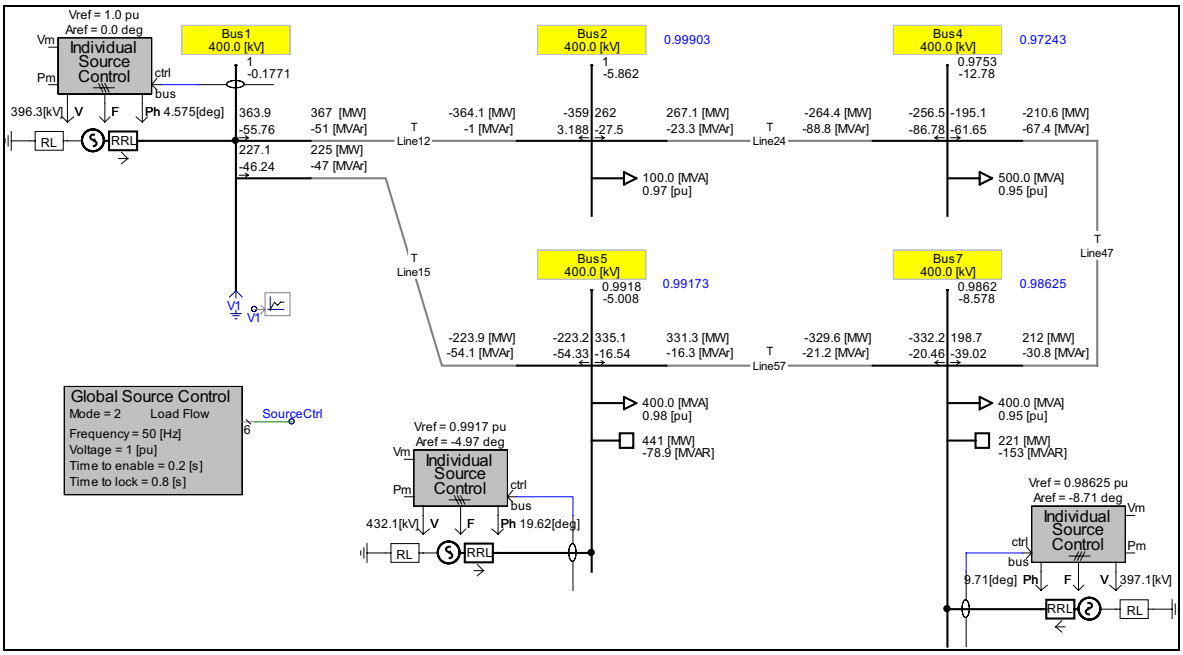
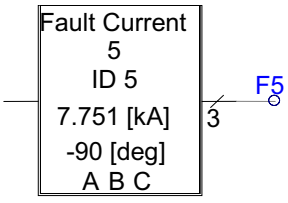


Figure 5 - Simplified network in PSCAD

SHORT CIRCUIT

Care should be taken when comparing the short-circuit data of different simulation software programs as there are different initial states for the network. As an example, PSSE offers two options when calculating fault currents: (1) fault current calculations take into consideration the pre-fault voltage conditions in the network, and (2) FLAT START function can be used where all the sources are set to 1 p.u. voltage and zero deg angle and the transformers are on nominal tap position. For comparison purposes, the author prefers the FLAT START method, as this method eliminates the differences that can be observed in load flow results. It should be noted that the FLAT START in PSSE ignores phase shift across a transformer.



The Model verification library offers a custom component that measures fault currents through the application of three breakers to ground according to its control variables. Individual phase currents or three phase values can be measured and displayed. The current through the breakers is measured and the On-Line FFT function is used to calculate RMS values of fault currents. When a three-phase fault is applied, the positive sequence current is calculated. When the Fault Current component is used in a multiple run application shown in Figure 6, the single-phase and three-phase short-circuit currents can be determined at any number of locations, up to a maximum value of 10.

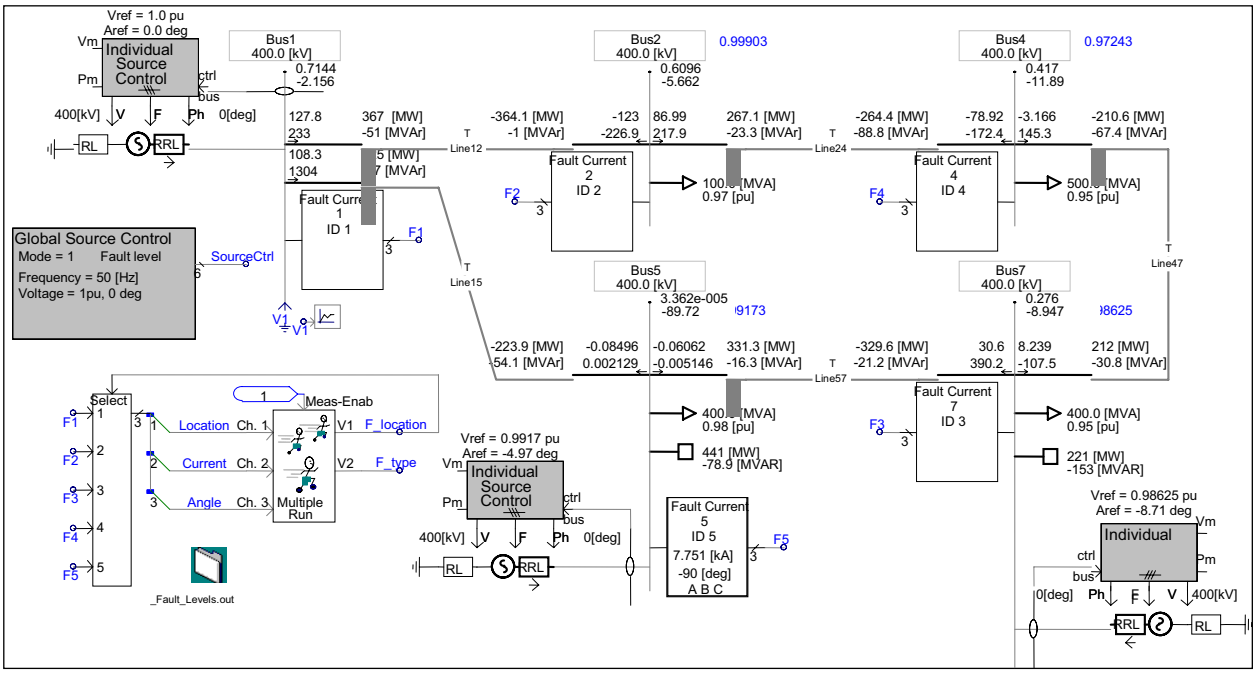


Figure 6 - Short circuit analysis

For the sample case, the fault currents are obtained with different simulation tools and listed in Table 1 for comparison:

- Currents for the complete network shown in Figure 1 as calculated with PSSE
- Currents for the SCEQ network equivalent shown in Figure 2 as calculated by PSCAD.
- Currents for the Simple network equivalent shown in Figure 3 as calculated by PSCAD.
- Currents for the Simple network equivalent shown in Figure 3 with adjusted source impedance values as calculated by PSCAD.

In most cases, the source impedance can be scaled through a manual iteration process. The X/R ratio of the source impedance is kept constant and the magnitude of the impedance is scaled according to the ratio by which the fault current obtained in PSCAD compared to PSSE is too big or too small. Care should be taken when short-circuit data is compared for networks that employ series compensation. The Metal Oxide Varistor (MOV) that is normally installed across the terminals of a Series Capacitor Bank reduces the magnitude of the short-circuit current through the bank and, consequently, the short-circuit current flowing through the line it is connected to is also reduced. Although PSCAD can model the Metal Oxide Varistor (MOV) across a Series Capacitor, it is not safe to assume that other software programs have the same modeling capability.

Table 1 - Short circuit data

Busbar	PSSE complete network 3-ph current [A]	PSSE complete network 1-ph current [A]	PSCAD SCEQ network 3-ph current [kA]	PSCAD SCEQ network 1-ph current [kA]	PSCAD Simple network 3-ph current [kA]	PSCAD Simple network 1-ph current [kA]	PSCAD Simple adjusted network 3-ph current [kA]	PSCAD Simple adjusted network 1-ph current [kA]
1	13374.9	12619.4	13.288	12.506	14.917	13.53	13.301	12.369
2	4555.5	2915.9	4.518	3.007	4.802	3.108	4.610	3.034
3	9548.8	8372.1						
4	3592.1	2237.9	3.625	2.666	3.865	2.767	3.700	2.684
5	7584.1	5399.7	7.576	5.636	8.855	6.172	7.750	5.500
6	6020.8	4965.3						
7	6151	4333.6	6.175	4.693	6.984	5.045	6.254	4.53
8	4488	3083.8						
9	4269.3	2776.3						
10	4991.8	3243.8						
11	8257.3	5934.4						

FREQUENCY ANALYSIS

The first check to be done on the frequency analysis results is to compare the fundamental frequency impedance value with the fault current values obtained from PSCAD, PSSE or field measurements.

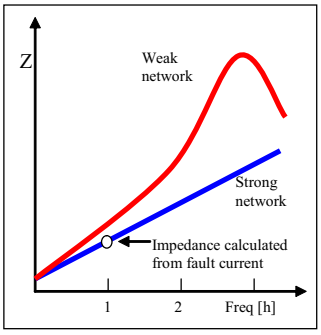


Figure 7 - Network impendance

As shown in Figure 7, in a strong network, the impedance back to the source is much lower than the shunt impedance at the busbar of concern. In this case, the shunt impedance does not have an impact on the short circuit impedance and a good correlation will exist between the impedance at fundamental frequency (blue curve) and the fault current (black circle). In a weak network, this will not always be the case, since the fault current represents the system impedance back to the sources, and it excludes shunt devices to ground that may be connected to the faulted busbar. In those instances where the shunt devices, connected to the busbar of interest, cause a low order parallel resonance with the source impedance, the network impedance from the frequency scan (red curve) will give a higher value than the value obtained from the short circuit analysis.

In PSCAD, both the current injection and the frequency scan component determine the network impedance independent of the voltage across the shunt devices. While, when the network impedance at fundamental frequency is calculated from the fault current, the effect from shunt devices close to the short circuit is eliminated.

As a rule of thumb, the harmonic number of the frequency of a low order parallel resonance between shunt capacitors and the source impedance can be calculated as:

$$h = \sqrt{\frac{S_{sc}}{Q}}$$

where S_{sc} is the Short Circuit capacity in MW and Q is the shunt capacitor rating in MVAr at the busbar. Example: A 100MVAr shunt capacitor will resonate at the 5th harmonic in a network with a short circuit level of 2500MVA.

When the frequency analysis results are compared with field measurements, note that the measurement obtained from a CVT (Capacitive coupled Voltage Transformer) should not be considered as accurate because of inevitable voltage distortions. CVTs are tuned with a resonant-burden circuit to only give accurate measurements at fundamental frequency. CVTs are often installed at EHV voltage levels to reduce cost.

SUMMARY

There is nothing as good as your engineering gut-feel to verify results. The reader is urged to gain as much practical experience as possible to get a feel for what results to expect before doing a simulation. If the reader is modeling a network for the first time, it is encouraged to "play around" with the network once it is completed and ready for simulations to get familiar with the network behavior. Open breakers, create faults and change the set points of dynamic devices like SVCs or HVDC systems. Observe the changes that occur in the flow of power, voltage magnitudes and the current flows. This should assist the reader in setting up the simulation and to evaluate the results that he needs to investigate.

REFERENCES

PSS/E-29 PROGRAM APPLICATION GUIDE: VOLUME I, Network Reduction for Fault Analysis, Activity SCEQ.

DATA LISTING

Table 2: PSSE data for the complete network

Busbars

Busbar	Voltage [kV]	Load [MW]	Load [MVAr]
1	400	-	-
2	400	97.0	24.3
3	400	192.0	56.0
4	400	475.0	156.1
5	400	392.0	79.6
6	400	49.0	9.95
7	400	380.0	124.9
8	400	147.0	29.9
9	400	196.0	39.8
10	400	96.0	28.0
11	400	49.0	9.9

Generators

Busbar	Voltage [kV]	Sbase [MVA]	R pos [pu]	X pos [pu]	R zero [pu]	X zero [pu]
1	400	2000	0.003	0.3	0.003	0.3
3	400	1000	0.003	0.3	0.003	0.3
6	400	500	0.003	0.3	0.003	0.3

Lines

From bus	To bus	R pos [pu]	X pos [pu]	B pos [pu]	R zero [pu]	X zero [pu]	B zero [pu]	Length [km]
1	2	0.00222	0.02885	0.90702	0.02978	0.09425	0.61452	150
1	5	0.00294	0.03834	1.21140	0.03907	0.12483	0.82239	200
1	11	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100
2	4	0.00363	0.04772	1.51754	0.04783	0.15472	1.03290	250
3	5	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100
3	11	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100
4	7	0.00294	0.03834	1.21140	0.03907	0.12483	0.82239	200
5	7	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100
6	7	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100
6	8	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100
8	9	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100
9	10	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100
10	11	0.00149	0.01928	0.60396	0.02008	0.063126	0.40861	100

Table 3: PSSE SCEQ network data

Generators

Busbar	Voltage [kV]	Sbase [MVA]	R pos [pu]	X pos [pu]	R zero [pu]	X zero [pu]
1	400	100	0.000144	0.01333	0.000149	0.01395
5	400	100	0.00192	0.06342	0.02044	0.10701
7	400	100	0.00217	0.08381	0.02095	0.12849

Lines

From bus	To bus	R pos [pu]	X pos [pu]	R zero [pu]	X zero [pu]
1	5	0.00908	0.09321	0.25535	0.48443
1	7	0.02103	0.22172	0.55318	1.0934
5	7	0.06517	0.58513	2.98271	4.13603

Table 4: PSSE network data for simple equivalent

Generators

Busbar	Voltage [kV]	Sbase [MVA]	R pos [pu]	X pos [pu]	R zero [pu]	X zero [pu]
1	400	100	0.00022	0.01181	0.00047	0.01358
5	400	100	0.00203	0.03756	0.02156	0.08762
7	400	100	0.00271	0.05643	0.02293	0.11356

Table 5: Adjusted network data for simple equivalent

Generators

Busbar	Voltage [kV]	Sbase [MVA]	R pos [pu]	X pos [pu]	R zero [pu]	X zero [pu]
1	400	100	0.000246	0.000246	0.000483	0.000483
5	400	100	0.002615	0.002615	0.026741	0.026741
7	400	100	0.003314	0.003314	0.030927	0.030927

Chapter 10:

Using PSCAD/EMTDC Waveforms for Real Time Testing (RTP)

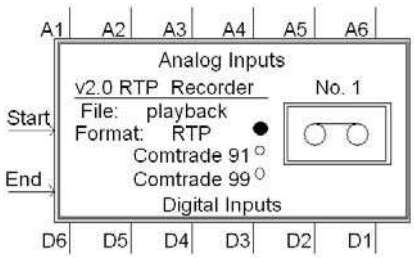
Any waveform that is generated by PSCAD/EMTDC can be converted into an analog or digital signal, and used for testing real equipment in both laboratory and field. The Real Time Playback or RTP system developed by Manitoba HVDC Research Centre Inc. is a powerful open-loop real time playback system specially designed to take full advantage of PSCAD software. The following describes the procedure for using PSCAD to prepare a data file for RTP playback. More information on the RTP system can be found at our website http://www.hvdc.ca.

- Friendly graphical user interface.
- Easy set-up and calibration.
- Playback 12 analog channels in real time.
- 16 logic inputs and outputs.
- Ethernet connectivity for high speed data transfer.
- Batch mode for automated processing.
- GPS feature and master/slave mode to synchronize multiple RTP units.
- View and adjust signal levels from simulation to final output.
- Intrinsic connectors for ensured safety.

PSCAD RTP RECORDER

Any data signal available in PSCAD/EMTDC can be recorded and saved as a RTP playback data file. The RTP Recorder Component is located in the External Data Recorders & Readers section of the Master Library. The user can configure the START and STOP times for the playback record, as well as define analog and digital signals for future RTP playback. Each recorder can save up to 12 analog channels and 16 digital outputs to match the RTP hardware. If more signals are required, then multiple RTP Recorders can be used in the simulation. The RTP Recorder has options to record signals in COMTRADE format, as well.

PT or CT models can be used in a PSCAD simulation to more accurately simulate the effect that these devices will have on waveforms seen by protection relays. Optionally, inside the recorder properties, simple PT or CT ratios can be programmed. The CT/PT ratios are transferred to the RTP Playback program to assist the user in tracking signal levels during real time testing. The digital outputs are useful during real time testing to function as trigger signals.



COMTRADE/RTP Recorder

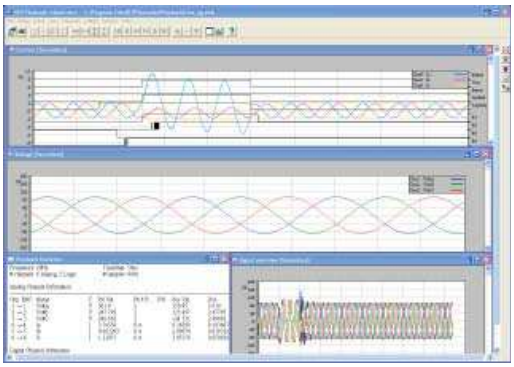
OUTPUT FILE LOCATION

Once a simulation case is compiled, PSCAD/EMTDC will automatically create a subdirectory with the case name appended by *.emt. This directory holds the temporary files created by PSCAD, including any output file. The RTP recorder file *.pbk will also be created in this subdirectory.

If the same case is repeated and the playback file name in the RTP Recorder is not changed, the RTP playback file *.pbk will be overwritten.

MULTIPLE RUN CAPABILITY

In order to perform repeated cases where parameters vary from run to run, a multiple run component is typically used. It is possible to



RTP Application:

Relay Protection
- Verify relay settings with accurate transient waveforms.
- Use GPS feature for end-to-end testing of protection systems.
- Increase confidence by thoroughly testing algorithms and relay settings with comprehensive simulation runs.

HVDC/Power Electronics/AC Filters
- Test protection and controls using realistic and complex waveforms found in power electronic circuits.
- Test all possible contingencies with simulated waveforms.

Power Quality Measurement Devices
- Calibrate PQ measurement systems using known waveforms.
- Confirm the results of PQ system with known sags, swells and transients.
- Verify measurement set-up and understand limitations of PQ test equipment.

create multiple playback files using the multiple run component of PSCAD, as described in Section 2. The playback file names generated with RTP Recorder are automatically truncated to the first 8 characters and then appended with the run number. The *.pbk data files can now be used in the RTP PLAYBACK program, which is available for download from our website or any PSCAD installation CD.

RTP PLAYBACK PROGRAM

Predefined waveforms from either PSCAD or COMTRADE files can be viewed, scaled, measured and played with RTP Playback program. The first and last cycles of the waveforms can be used to create PRE and POST fault waveforms with their duration defined by the user. When the playback file is first loaded, the signals will be opened in separate windows in PLAYBACK with Digital, Current, Voltage and Others signals each in their own windows. Inside PLAYBACK, the signals displayed in any window can be changed by Setup>Change dialogue.

In addition to the ability to play PSCAD/EMTDC waveforms, RTP program can also play COMTRADE waveforms and generate STATE waveforms with individual signal magnitude, frequency, duration, offset and harmonics. Multiple End-to-End testing can be performed using GPS Synchronization.

EXERCISES

10.1 Load the example case. Assign a playback file name in the RTP recorder. Disable the Multiple Run Component and run the simulation case. Observe the fault waveforms and generated RTP playback file. Enable the multiple run components and re-run the case. Verify that multiple playback files are generated. Repeat the above test with the COMTRADE format selected in the RTP Recorder.

10.2 Start the RTP PLAYBACK program and Load the playback file you created (RTP software is available at www.hvdc.ca or any PSCAD installation CDROM). Verify the waveform in RTP Playback program is the same as generated by PSCAD.

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