

VESA Coordinated Video Timings (CVT) Standard

Version 2.0

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vesa.org

Purpose

The VESA Coordinated Video Timings (CVT) Standard is a method for generating a consistent and coordinated set of timing specifications for computer display products. The intention of this Standard is to provide Source and display device manufacturers a common set of tools to enable new timings to be developed in a consistent manner that ensures greater compatibility.

Summary

CVT v2.0 defines mandates and methods for new timings. *CVT* restricts some aspects of the generated timings, including pixel clock precision and blanking parameters. This Standard specifies an equation-based method for developing timings designed for use with non-CRT display devices that can accommodate reduced horizontal blanking times.

Companion Documents

The companion spreadsheet for *CVT Standard* may be downloaded from vesa.org/vesa-standards/.

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Preface

Intellectual Property

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Support for this Standard

Clarifications and application notes to support this Standard may have been written. To obtain the latest Standard and any supporting documentation, contact VESA[®].

If you have a product that incorporates Coordinated Video Timings (CVT), ask the company that manufactured your product for assistance. If you are a manufacturer, VESA may assist you with any clarification you might need.

Submit all comments or reported errors to support@vesa.org.

Patents

VESA draws attention to the fact that it is claimed that compliance with this Standard might involve the use of a patent or other intellectual property right (collectively, “IPR”) concerning CVT. VESA takes no position concerning the evidence, validity, and scope of this IPR.

Attention is drawn to the possibility that some of the elements of this VESA Standard might be the subject of IPR other than those identified above. VESA shall not be held responsible for identifying any or all such IPR, and has made no inquiry into the possible existence of any such IPR.

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Acknowledgments

This Standard would not have been possible without the efforts of the VESA DisplayID Task Group. In particular, the following individuals and their companies contributed significant time and knowledge to this version of the Standard.

Table 1-1: Main Contributors to CVT v2.0

Company	Name	Contribution
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MediaTek, Inc.	Tung-Sheng Lin	Technical Content
NVIDIA Corp.	Kai Chen	Technical Content
Parade Technologies, Ltd.	Craig Wiley	Technical Content
Realtek Semiconductor Corp.	Jay Lin	Technical Content
Samsung Electronics Co., Ltd.	Frank Seto	Technical Content
Teledyne LeCroy	Jeff Stenhouse	Technical Content

Revision History

Table 1-2: Revision History

Date	Version	Description
September 27, 2021	2.0	<ul style="list-style-type: none"> Added mandate that Source devices support 80 to 200 pixels of horizontal blanking, and 460 to 705 us of vertical blanking Removed information related to Standard CRT-based and Reduced Blanking Timing version 1 generation (see CVT v1.2 for these timings) Simplified and reorganized Specification around requirements for Reduced Blanking Timing versions 2 and 3 Added changes from the following CVT v1.2 SCR: <i>Reduced blank v3 timing support to facilitate Adaptive-Sync operation and guarantee attainment of target refresh rate</i> Applied current VESA template style changes
February 8, 2013	1.2	<ul style="list-style-type: none"> Added section defining the timing generation rules for Reduced Blanking Timing v2 rules Updated Sections 3.3.1, 3.4.3, and 5.4 to clarify the refresh rate error calculation and timing generation for video optimized vs. non-video-optimized refresh rate
September 10, 2003	1.1	<ul style="list-style-type: none"> Section 3.4.1, points 6 and 7 revised to correct mistake (minimum Vertical Sync and Vertical Back Porch time is 550 us not 500 us) Rounding errors in VESA Standard Names corrected in Table 3 and 7 Missing Constants and Variables added to Table 9 and 10
March 26, 2003	1.0	<ul style="list-style-type: none"> Initial release

1 Introduction (Informative)

1.1 Background

This Standard defines an equation-based method for creating reduced blanking timings for display devices, such as LCDs, that do not require as much horizontal blanking as traditional CRTs. Timing generation mandates are also specified to control the number of possible CVT-compliant formats in existence.

1.2 Objectives

The purpose of CVT is to define a method of generating timings so that new timings can be created simply and easily that meet the requirements of display devices with different resolutions and refresh rates, and that support new variable refresh rate technologies such as VESA Adaptive-Sync. CVT provides a coordinated approach so that timing source generators and display devices know what the requirements for producing new timings will be and can take advantage of opportunities for forward compatibility with new devices and video formats.

In addition, because CVT uses common formulas to generate timings, it allows timing descriptors in capability structures such as *DisplayID* to be much smaller than comparable detailed timing descriptors that are designed to be completely flexible and independently describe every timing parameter.

1.3 Document Organization

This Standard is organized as follows:

- [Section 1 – Introduction \(Informative\)](#)

This section provides a definition of this Standard. This section also includes a list of acronyms and glossary of terms that are used within this Standard and references to related Specifications/Standards.

- [Section 2 – Timing Generation Mandates](#)

This section defines the mandates for generating timing.

- [Section 3 – Inputs, Constants, Variables, and Outputs](#)

This section defines the input and output timing parameters, constants, and variables that are used in the [Section 4](#) equations, and in the VESA CVT companion spreadsheet (available in Microsoft Excel format from vesa.org/vesa-standards/).

- [Section 4 – Calculation of Timing Parameters](#)

This section details how to calculate the timing parameters.

- [Appendix A – Main Contributor History \(Previous Versions\)](#)

This appendix lists the contributors to past releases of this Standard.

1.4 Document Conventions

1.4.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

1.4.2 Keywords

[Table 1-1](#) lists keywords that differentiate between the levels of mandates and options within this Standard.

Table 1-1: Keywords

Keyword	Definition
informative	Information that discusses and clarifies mandates and features.
may	Indicates a choice that does not have an implied preference.
N/A	Indicates that a field or value is not applicable, does not have a defined value, and shall not be checked or used by the recipient.
normative	Features that are mandated by this Standard.
optional	Features that are not mandated by this Standard. However, if an optional feature is implemented, the feature shall be implemented as defined by this Standard (optional normative).
shall	Indicates a mandate. Designers shall implement all such mandates to ensure interoperability with other compliant devices.
should	Indicates flexibility of choice with a preferred alternative. Equivalent to the phrases “is recommended” and “it is recommended that.”

1.4.3 Unit of Measure Symbols

[Table 1-2](#) lists unit of measure symbols that are used throughout this Standard.

Table 1-2: Unit of Measure Symbols

Symbol	Unit of Measure
Hz	hertz
kHz	kilohertz
us	microsecond
MHz	megahertz
ppm	parts per million

1.4.4 Acronyms and Abbreviations

Table 1-3 lists acronyms and abbreviations that are used throughout this Standard. Capitalization is applied in the definition to indicate the letters used in acronyms and abbreviations.

Table 1-3: Acronyms and Abbreviations

Term	Definition
CVT	Coordinated Video Timings (this Standard)
DisplayID	Display IDentification (<i>DisplayID Standard</i>)
HActive	Horizontal Active
HBlank	Horizontal Blank
HSync	Horizontal Sync
RB	Reduced Blanking
VBlank	Vertical Blank
VSynC	Vertical Sync

1.5 Reference Documents

Table 1-4: Reference Documents

Document	Version/Revision	Date	Referenced As
<i>VESA Coordinated Video Timings (CVT) Standard (legacy version)^a</i>	Version 1.2 + Errata E1	April 14, 2021	<i>CVT v1.2</i>
<i>VESA DisplayID Standard^a</i>	Version 2.1	TBD	<i>DisplayID Standard</i> <i>DisplayID</i>
<i>VESA Enhanced Extended Display Identification Standard (E-EDID)^a</i>	Release A.2	September 25, 2006	<i>E-EDID Standard</i> <i>E-EDID</i> <i>EDID</i>
<i>VESA E-EDID Implementation Guide^a</i>	Version 1.0	June 2, 2001	<i>E-EDID</i> <i>Implementation Guide</i>
<i>VESA Enhanced Display Data Channel (E-DDC) Standard^a</i>	Version 1.3	September 11, 2017	<i>E-DDC Standard</i> <i>E-DDC</i>

a. See vesa.org/vesa-standards/.

2 Timing Generation Mandates

This section defines the mandates for generating a timing.

Note: See [Section 4](#) for details regarding the computational steps that are involved in using these mandates to generate a timing for a given format.

2.1 Standard CRT-based Timing

The standard CRT-based timing formula has been removed from CVT v2.0. Implementers that need to use this formula can refer to the definition in [CVT v1.2](#).

2.2 Reduced Blanking Timing Version 1 (RB Timing v1)

The RB Timing v1 formula has been removed from CVT v2.0. Implementers that need to use this formula can refer to the definition in [CVT v1.2](#).

2.3 Reduced Blanking Timing Version 2 (RB Timing v2)

The following items define the mandates for the RB Timing v2 formula. The RB Timing v2 formula supports only progressive (i.e., non-interlaced) video timings.

1 Pixel Clock Selection

RB Timing v2 shall support a pixel clock precision of 0.001 MHz.

The following lists the steps taken to calculate the pixel clock for a given target refresh rate and active horizontal and vertical resolution:

- a The nominal refresh rate is used to calculate the horizontal and vertical blank (HBlank and VBlank) parameters.
- b The required pixel clock is then calculated based on the HBlank and VBlank parameters, along with the target refresh rate (which is adjusted from the nominal rate by including an **optional** 1,000/1,001 factor if a video-optimized rate is requested).
- c The resulting pixel clock value is then rounded down to the nearest 0.001 pixel clock.

Using the nominal value in step [a](#) guarantees that the only difference in timing between a video-optimized timing vs. a non-video-optimized timing for a given refresh rate is the pixel clock frequency (i.e., all other horizontal and vertical parameters are the same). The result from step [c](#) will often cause the actual refresh rate to be lower than the target refresh rate by a small amount.

2 Vertical Refresh Rate

The default nominal refresh rate for RB Timing v2 is 60 Hz. However, other progressive refresh rates may be specified depending on the application. A pixel clock precision of 0.001 MHz allows video-optimized refresh rates (e.g., $60 * 1,000/1,001 \approx 59.94$ Hz, $30 * 1,000/1,001 \approx 29.97$ Hz) to be supported with the RB Timing v2 formula. A factor of 1,000/1,001 is applied to the nominal refresh rate if a video-optimized target refresh rate is requested.

3 Horizontal Counts

The number of horizontal active (HActive) pixels has a precision of 1 pixel.

The (HActive) width of generated timings may be any positive integer value.

4 HBlank Period

The HBlank period shall be fixed at 80 pixels.

5 Horizontal Sync Pulse Duration and Position

The horizontal sync (HSync) pulse duration shall be fixed at 32 pixels.

The horizontal front porch shall be fixed at 8 pixels.

The horizontal back porch shall be fixed at 40 pixels.

6 VBlank Period

The VBlank period shall be the first integer multiple of horizontal lines that results in a VBlank duration that exceeds 460 us.

7 Vertical Sync Pulse Duration and Position

The vertical sync (VSync) pulse duration shall be 8 lines.

The vertical back porch shall be 6 lines.

The vertical front porch shall be the remainder of the VBlank period.

2.4

Reduced Blanking Timing Version 3 (RB Timing v3)

The following items define the mandates for the RB Timing v3 formula. The RB Timing v3 formula supports only progressive (i.e., non-interlaced) video timings. RB Timing v3 is intended to work in conjunction with VESA Adaptive-Sync operation (or other similar variable refresh rate methodology).

1 Pixel Clock Selection

RB Timing v3 shall support a pixel clock precision of 0.001 MHz.

The following lists the steps taken to calculate the pixel clock for a given target refresh rate and active horizontal and vertical resolution:

- a The target refresh rate is determined by adding +350 ppm to the nominal refresh rate, and is used to calculate the HBlank and VBlank parameters.
- b The required pixel clock is then calculated based on the HBlank and VBlank blanking parameters along with the target refresh rate.
- c The resulting pixel clock value is then rounded up to the nearest 0.001 pixel clock.

The result from step c will often cause the actual refresh rate to be higher than the target refresh rate by a small amount.

2 Vertical Refresh Rate

The default nominal refresh rate for RB Timing v3 is 60 Hz. However, other progressive refresh rates may be specified depending on the application. An offset of +350 ppm is applied to the nominal refresh rate to ensure that variable refresh rate systems, such as VESA Adaptive-Sync, are able to provide an average frame rate that matches the nominal rate. Because RB Timing v3 is optimized for variable refresh rate systems that continually adjust the frame rate to match the expected nominal rate, a video-optimized target refresh rate option is **not** necessary. For applications that need a fixed, video-optimized target refresh rate, RB Timing v2 should be used instead.

3 Horizontal Counts

The number of HActive pixels has a precision of 8 pixels.

The HActive width of generated timings may be any positive integer value that is a multiple of 8.

4 HBlank Period

The default HBlank period is 80 pixels. Additional horizontal blanking may be **optionally** specified to accommodate different device characteristics. The additional blanking shall be between 0 and 120 pixels, and must be a multiple of 8 pixels. Hence, allowable HBlank periods are 80, 88, 96, ..., 192, 200 pixels. Source devices that claim compatibility with RB Timing v3 at a given resolution and refresh rate shall support all timing versions with any of the allowable HBlank periods between 80 and 200 pixels, inclusive.

5 HSync Pulse Duration and Position

The HSync pulse duration shall be fixed at 32 pixels.

The horizontal front porch shall be fixed at 8 pixels.

The horizontal back porch shall be the HBlank period reduced by 40 pixels. Hence, allowable horizontal back porch durations are 40, 48, ..., 152, 160 pixels.

6 VBlank Period

The default VBlank period shall be the first integer multiple of horizontal lines that results in a VBlank duration that exceeds 460 us. The VBlank time may **optionally** be extended beyond 460 us. Source devices that claim compatibility with RB Timing v3 at a given resolution and refresh rate shall support all timing versions with vertical blanking durations that are greater than 460 us, and less than or equal to 705 us plus the duration of one horizontal line.

7 VSync Pulse Duration and Position

The VSync pulse duration shall be 8 lines.

The default vertical back porch shall be 6 lines. If an early VSync pulse position is requested, the vertical back porch is calculated by dividing the total VBlank duration by 2 and rounding down to the nearest integer.

The vertical front porch shall be the remainder of the VBlank period.

3 Inputs, Constants, Variables, and Outputs

This section defines the input and output timing parameters, constants, and variables that are used in the [Section 4](#) equations, and in the VESA CVT companion spreadsheet (available in Microsoft Excel format from vesa.org/vesa-standards/).

Table 3-1: Input Parameters

Input Parameter	Definition	RB Timing Valid Values	
		v2	v3
I_RED_BLANK_VER	Version of the reduced blanking timing formula to be used.	2	3
I_H_PIXELS	Desired active (visible) horizontal pixels per line (will be rounded to the nearest integer number of character cells).	Any positive integer	
I_V_LINES	Desired active (visible) vertical lines per frame.	Any positive integer	
I_IP_FREQ_RQD	Target vertical refresh rate.	Any positive real number	
I_VIDEO_OPT	Indicates whether to apply a 1,000/1,001 factor to the target vertical refresh rate to generate a “video-optimized” timing variant.	“Y” or “N”	“N”
I_ADDITIONAL_HBLANK	Desired additional number of pixels to add to the base HBlank duration.	0	0 or any integer multiple of 8 between 8 and 120, inclusive
I_VBLANK	Desired VBlank time (in us).	460	460 or greater ^a
I_EARLY_VSYNC_RQD	Indicates whether the VSync location is early (near the middle of the VBlank period) –or– late (near the end of the VBlank period).	“N”	“Y” or “N”

*a. VBlank times greater than 705 us might **not** be supported by all RB Timing v3-compliant Source devices.*

Table 3-2: Constants^a

Constant	Definition	RB Timing v2	RB Timing v3
C_CLOCK_STEP	Pixel clock precision.	0.001	0.001
C_CELL_GRAN_RND	Character cell width.	1	8
C_H_FRONT_PORCH	Number of pixels in the horizontal front porch period.	8	8
C_RB_H_BLANK	Minimum HBlank duration (in pixels) for RB timings. Measured as the number of pixels between the last active (visible) pixel of one line and the first active (visible) pixel of the next line.	80	80
C_RB_H_SYNC	HSync duration (in pixels) for RB timings.	32	32
C_RB_MIN_V_BLANK	Minimum VBlank period (in us) for RB timings. Measured as the number of lines between the last line of active (visible) video of one frame and the first line of active (visible) video of the next frame.	460	460
C_RB_V_FPORCH	Minimum vertical front porch duration (in lines).	1	1
C_V_SYNC_RND	VSyn duration (in lines).	8	8
C_MIN_V_BPORCH	Minimum vertical back porch.	6	6
C_V_FIELD_RATE_PPM_ADJ	Additional ppm offset adjustment to be added to the requested refresh rate.	0	+350 ppm

*a. The values listed are required for CVT compliance. If other values are used for these constants, the resulting timing will **not** be CVT-compliant.*

Table 3-3: Variables

Variable	Definition
ACT_H_FREQ	Actual horizontal frequency.
ACT_V_BLANK_TIME	Actual total VBlank time (in us).
VBI_LINES	Number of VBlank lines required to meet the minimum VBlank period.
V_BLANK	Actual number of VBlank lines in the VBlank period (VBI_LINES is adjusted to ensure that it is more than the minimum number of lines required).
H_PERIOD_EST	Used as an intermediary variable to estimate the horizontal period so that critical parameters such as the required pixel clock frequency, VBlank interval, etc., can be determined.
RB_MIN_VBI	Minimum allowable VBlank Interval (in lines).
REFRESH_MULTIPLIER	Refresh rate multiplier factor. For RB Timing v2, the factor is set to 1,000/1,001 if a video-optimized refresh rate is requested. In all other cases, the factor is set to 1.
TOTAL_PIXELS	Total number of pixel clock cycles per horizontal line.
TOTAL_V_LINES	Total number of vertical lines per field. For interlaced timing, this value has a half line added. For progressive scan timing, the value is always an integer.
V_FIELD_RATE_RQD	Specifies the required vertical field rate. This value represents the target vertical refresh rate adjusted by the required ppm offset.

Table 3-4: Output Timing Parameters

Parameter	Definition
ACT_PIXEL_FREQ	Pixel clock frequency.
TOTAL_ACTIVE_PIXELS	Total number of active (visible) pixels per line.
V_LINES_RND	Total number of active (visible) vertical lines per frame.
C_H_FRONT_PORCH	Number of pixels in the horizontal front porch period.
C_RB_H_SYNC	Number of pixels in the HSync period.
H_BACK_PORCH	Number of pixels in the horizontal back porch period.
V_FRONT_PORCH	Number of lines in the vertical front porch period.
C_V_SYNC_RND	Number of lines in the VSync period.
V_BACK_PORCH	Number of lines in the vertical back porch period.
ACT_FRAME_RATE	Frame rate.

4 Calculation of Timing Parameters

This section details how to calculate the timing parameters. These calculations are used in the VESA CVT companion spreadsheet, which is available in Microsoft Excel format from vesa.org/vesa-standards/.

4.1 Explanation of Terms

Table 4-1 defines the terms and operators used in the following equations:

Table 4-1: Equation Terms and Operations

Term / Operator	Description
+	Addition
–	Subtraction
*	Multiplication
/	Division
ROUNDDOWN(<i>value</i> , <i>decimal_places</i>)	Returns <i>value</i> rounded down to the number of decimal places specified by <i>decimal_places</i> . If <i>decimal_places</i> is 0, the value is rounded down to the nearest integer.
ROUNDUP(<i>value</i> , <i>decimal_places</i>)	Returns <i>value</i> rounded up to the number of decimal places specified by <i>decimal_places</i> . If <i>decimal_places</i> is 0, the value is rounded up to the nearest integer.
AND(<i>logic_test_1</i> , <i>logic_test_2</i>)	Returns true if both <i>logic_test_1</i> and <i>logic_test_2</i> evaluate to true, and returns false if <i>logic_test_1</i> and/or <i>logic_test_2</i> evaluate to false.
IF(<i>logic_test</i> , <i>value_if_true</i> , <i>value_if_false</i>)	If-then statement that returns <i>value_if_true</i> when the <i>logic_test</i> expression evaluates to true, and returns <i>value_if_false</i> when the <i>logic_test</i> expression evaluates to false.

4.2 Computation of Parameters

Formula Inputs, Constants and Variables are defined in [Section 3](#).

4.2.1 Assign Constants Based on Formula Version

- 1 Character Cell Boundary

$$C_CELL_GRAN_RND = IF((I_RED_BLANK_VER=3), 8, 1)$$

- 2 Field Rate Adjustment

$$C_V_FIELD_RATE_PPM_ADJ = IF((I_RED_BLANK_VER=3), 350, 0)$$

4.2.2 Evaluate Variables and Determine Calculated Timing Parameters

- 1 Calculate the required field refresh rate (Hz):

$$V_FIELD_RATE_RQD = I_IP_FREQ_RQD * (1 + C_V_FIELD_RATE_PPM_ADJ / 1000000)$$

- 2 Round the desired number of horizontal pixels down to the nearest character cell boundary:

$$TOTAL_ACTIVE_PIXELS = ROUNDDOWN(I_H_PIXELS / C_CELL_GRAN_RND, 0) * C_CELL_GRAN_RND$$

- 3 Round the number of vertical lines down to the nearest integer:

$$V_LINES_RND = ROUNDDOWN(I_V_LINES, 0)$$

- 4 Calculate the estimated Horizontal Period (kHz):

$$H_PERIOD_EST = ((1000000 / (V_FIELD_RATE_RQD)) - C_RB_MIN_V_BLANK) / V_LINES_RND$$

- 5 Calculate the total VBlank time:

$$ACT_V_BLANK_TIME = IF(I_VBLANK < C_RB_MIN_V_BLANK, C_RB_MIN_V_BLANK, I_VBLANK)$$

- 6 Calculate the number of idealized lines in the VBlank interval:

$$VBI_LINES = ROUNDUP(ACT_V_BLANK_TIME / H_PERIOD_EST, 0)$$

- 7 Determine whether idealized VBlank is sufficient and calculate the actual number of lines in the VBlank period:

$$RB_MIN_VBI = C_RB_V_FPORCH + C_V_SYNC_RND + C_MIN_V_BPORCH$$

$$V_BLANK = IF(VBI_LINES < RB_MIN_VBI, RB_MIN_VBI, VBI_LINES)$$

- 8 Calculate the total number of vertical lines:

$$TOTAL_V_LINES = V_BLANK + V_LINES_RND$$

- 9 Calculate the vertical back porch:

$$V_BACK_PORCH = IF(AND(I_RED_BLANK_VER=3, I_EARLY_VSYNC_RQD?="Y"), ROUNDDOWN(VBI_LINES / 2, 0), C_MIN_V_BPORCH)$$

- 10 Calculate the vertical front porch:

$$\mathbf{V_FRONT_PORCH} = \mathbf{V_BLANK} - \mathbf{V_BACK_PORCH} - \mathbf{C_V_SYNC_RND}$$

- 11 Calculate the total number of pixels per line:

$$\mathbf{TOTAL_PIXELS} = \mathbf{TOTAL_ACTIVE_PIXELS} + \mathbf{C_RB_H_BLANK} + \mathbf{IF(I_RED_BLANK_VER=3, I_ADDITIONAL_HBLANK, 0)}$$

- 12 Calculate the horizontal back porch:

$$\mathbf{H_BACK_PORCH} = \mathbf{C_RB_H_BLANK} + \mathbf{IF(I_RED_BLANK_VER=3, I_ADDITIONAL_HBLANK, 0)} - \mathbf{C_H_FRONT_PORCH} - \mathbf{C_RB_H_SYNC}$$

- 13 Calculate the pixel clock frequency to the nearest C_CLOCK_STEP (MHz):

$$\mathbf{REFRESH_MULTIPLIER} = \mathbf{IF(AND(I_RED_BLANK_VER=2, I_VIDEO_OPT?="Y"), 1000/1001, 1)}$$

$$\mathbf{ACT_PIXEL_FREQ} = \mathbf{C_CLOCK_STEP} * \mathbf{IF(I_RED_BLANK_VER=2, ROUNDDOWN((V_FIELD_RATE_RQD * TOTAL_V_LINES * TOTAL_PIXELS / 1000000 * REFRESH_MULTIPLIER) / C_CLOCK_STEP, 0), ROUNDUP((V_FIELD_RATE_RQD * TOTAL_V_LINES * TOTAL_PIXELS / 1000000 * REFRESH_MULTIPLIER) / C_CLOCK_STEP, 0))}$$

- 14 Find actual Horizontal Frequency (kHz):

$$\mathbf{ACT_H_FREQ} = 1000 * \mathbf{ACT_PIXEL_FREQ} / \mathbf{TOTAL_PIXELS}$$

- 15 Find actual Vertical Refresh Rate (Hz):

$$\mathbf{ACT_FRAME_RATE} = 1000 * \mathbf{ACT_H_FREQ} / \mathbf{TOTAL_V_LINES}$$

A Main Contributor History (Previous Versions)

Table A-1: Main Contributor History (Previous Versions)

Company	Name	Contribution	Version
Advanced Micro Devices, Inc.	David Glen	Technical Content	1.1, 1.2
	Syed A. Hussain	Document Editor, Technical Content	1.2
Advanced Micro Devices, Inc. (formerly known as ATI Technologies, Inc.)	Quinn Carter	Technical Content	1.2
Analogix Semiconductor, Inc.	Greg Stewart	Technical Content	1.2
Apple, Inc.	Colin Whitby-Stevens	Technical Content	1.2
Dell, Inc.	Joe Goodart	Technical Content	1.1
EIZO NANAIO Corp.	Shiro Makino	Technical Content	1.1
Genesis Microchip	Graham Loveridge	Work Group Leader, Technical Content	1.1
	Jim Webb	Technical Content	1.1
Hitachi Ltd.	Youichi Igarashi	Technical Content	1.1
InFocus	Jory Olson	Technical Content	1.1
Intel Corp.	Mrinalini Attaluri	Technical Content	1.2
	Jamie Johnston	Technical Content	1.2
International Display Tech.	Hiroshi Yamashita	Technical Content	1.1
Matrox Graphics, Inc.	Jean-Jacques Ostiguy	Technical Content	1.2
NVIDIA Corp.	Keita Kitahama	Technical Content	1.1
	David Stears	Technical Content	1.2
Parade Technologies, Ltd.	Craig Wiley	Technical Content	1.2
Pioneer Corp.	Nozomu Kikuchi	Technical Content	1.1
Quantum Data, Inc.	Mark Stockfisch	Technical Content	1.2
Sony Corp.	Steve Hasegawa	Technical Content	1.1
STMicroelectronics, Inc.	Alan Kobayashi	Task Group Chair, Technical Content	1.2
Sun Microsystems	Joe Miseli	Technical Content	1.1
Synaptics, Inc.	Prashant Shamarao	Technical Content	1.2
Total Technologies Ltd.	Don Chambers	Technical Content	1.1