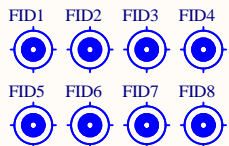
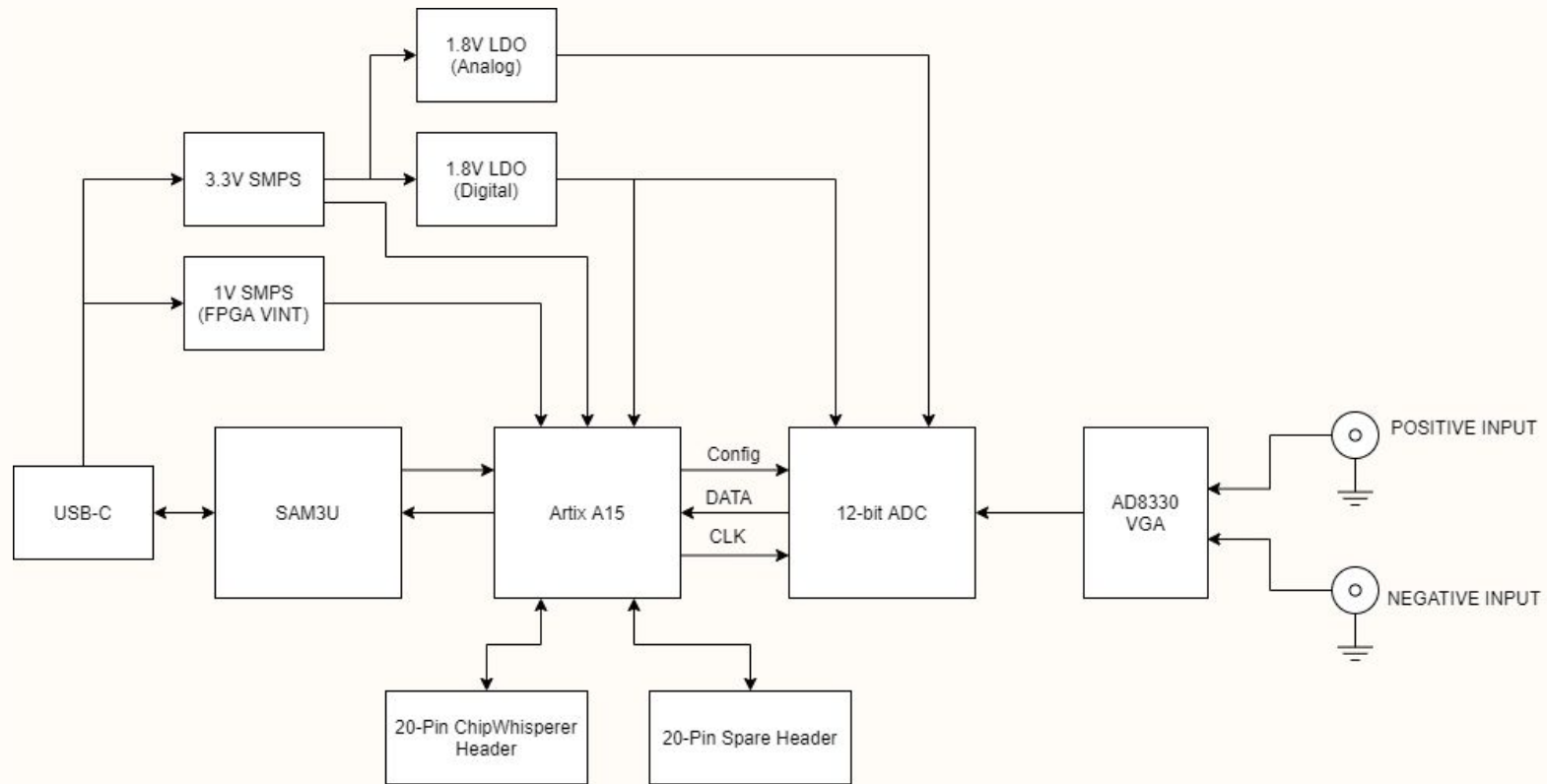


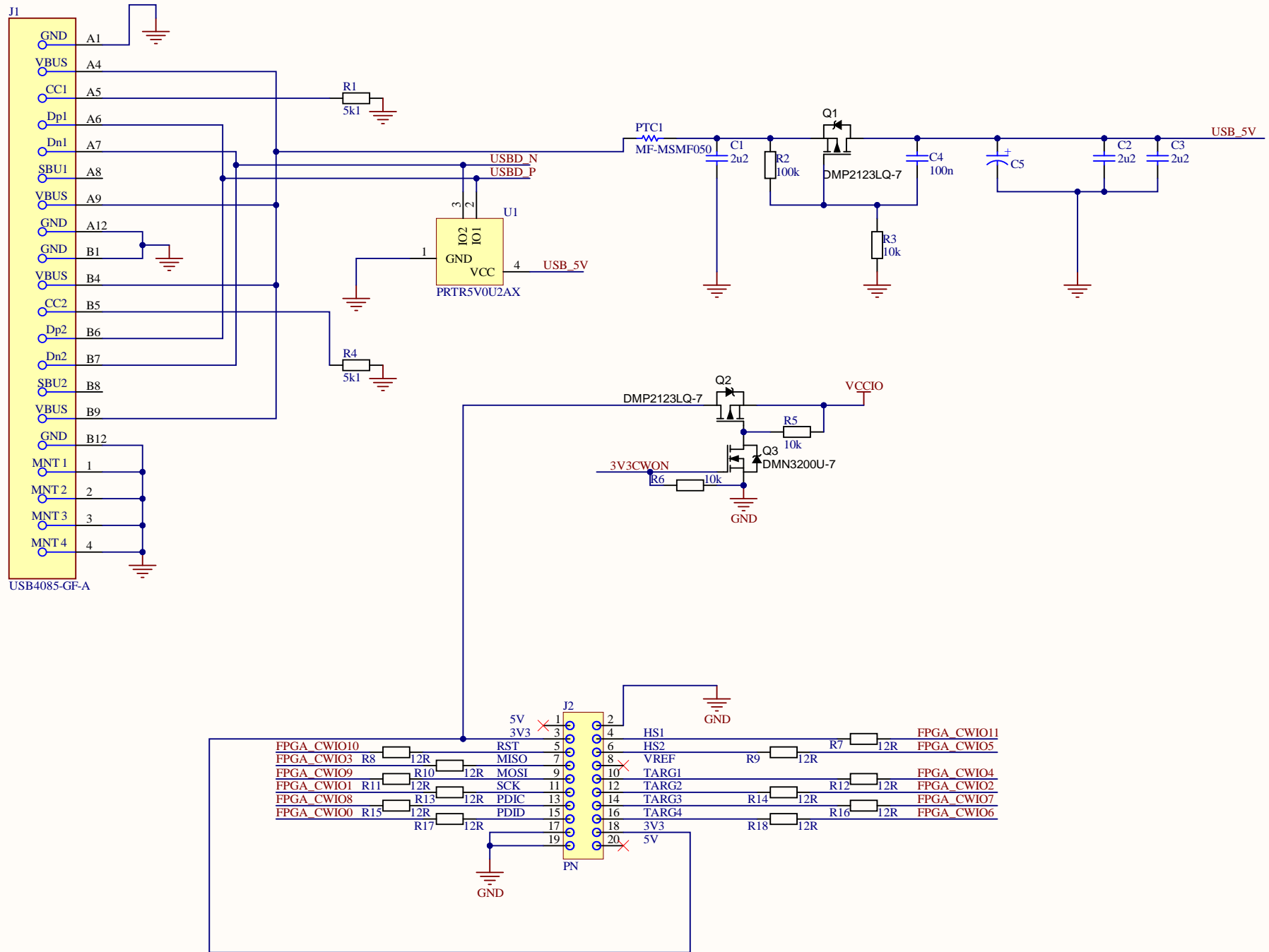


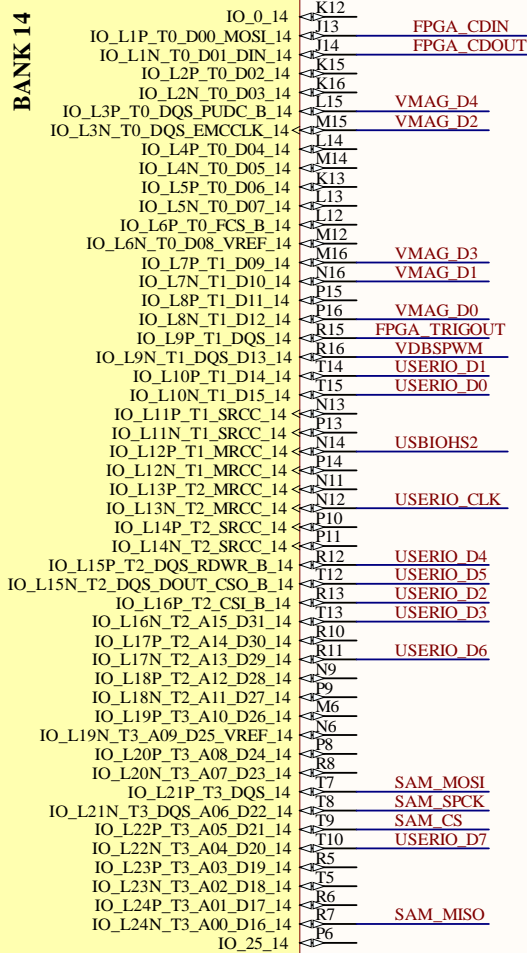
# ChipWhisperer-Husky



Title: <b>Info &amp; Block Diagram</b>			 Approved: YES	
Rev: 02	Project: <b>CW-Husky</b>	License: TBD		
Date: <a href="#">2021-04-05</a>	Time: <a href="#">9:39:04 AM</a>	Sheet <a href="#">1</a> of <a href="#">9</a>	Copyright © NewAE Technology Inc.	
File: <a href="#">cwh_frontpage.SchDoc</a>			<a href="#">NewAE.com</a>	

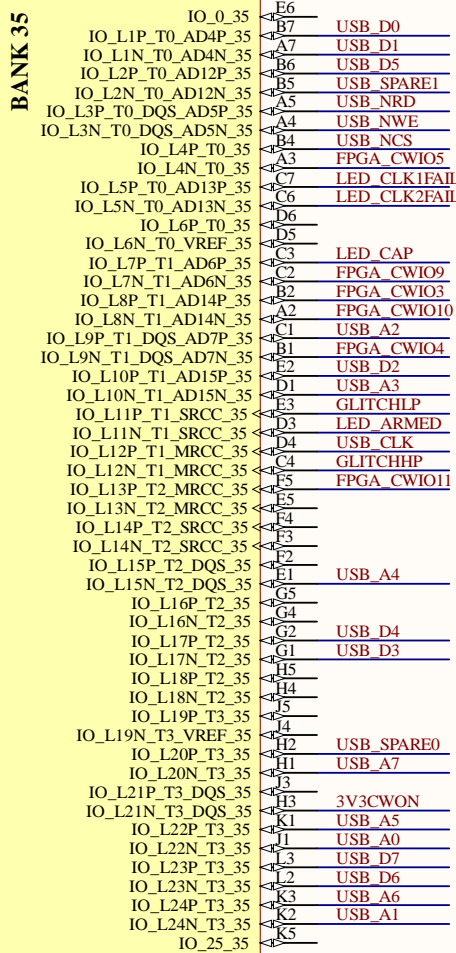


U2A



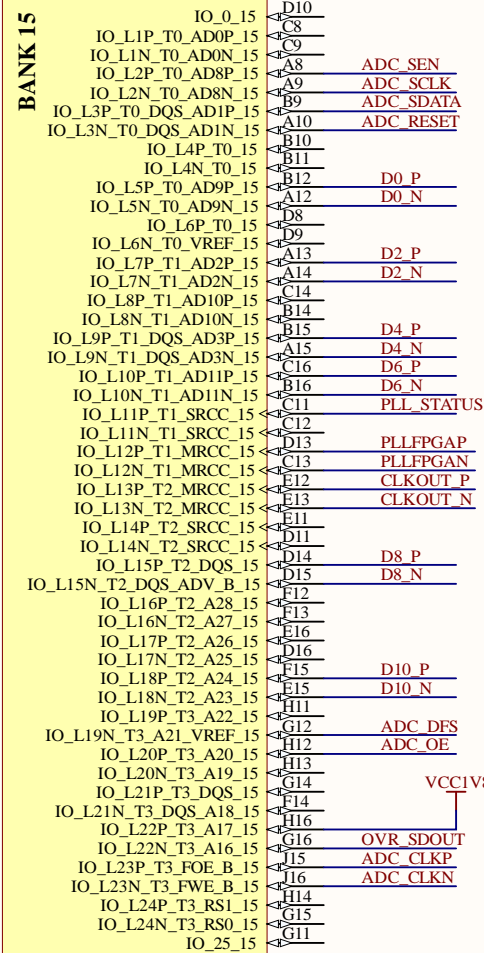
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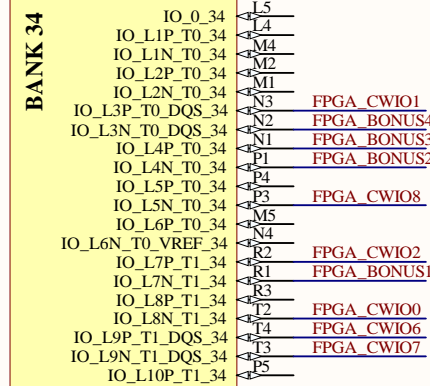
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U2B



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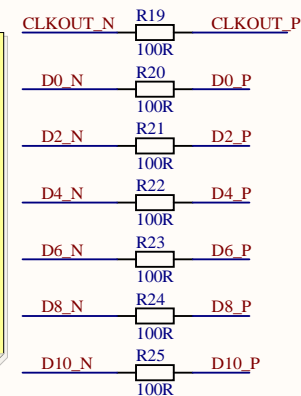


XC7A35T-1FTG256C

VCCIO=1.8V for this bank.

LVDS on A7 requires VCC=2.5, but ADC I/O is at 1.8V, so need to use VCC=1.8V. LVDS should work according to refs at VCCIO=1.8V, but it's marginal.

ADC supports LVC MOS18 in case LVDS doesn't work - depopulate LVDS term if required.

Title: **FPGA I/O**

Approved: YES

Rev: 02

Project: CW-Husky

License: TBD

Date: 2021-04-05

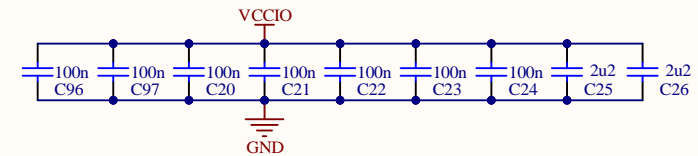
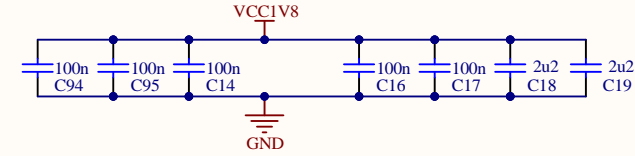
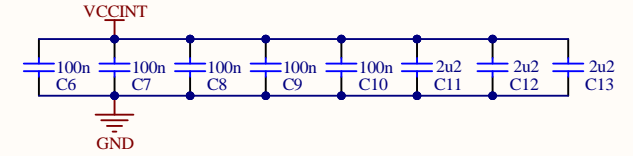
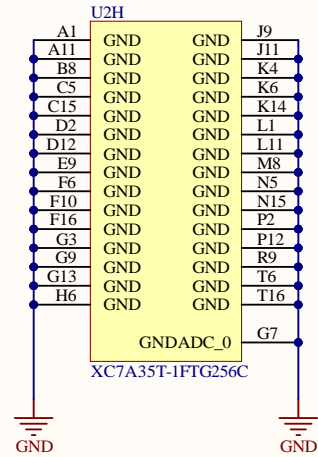
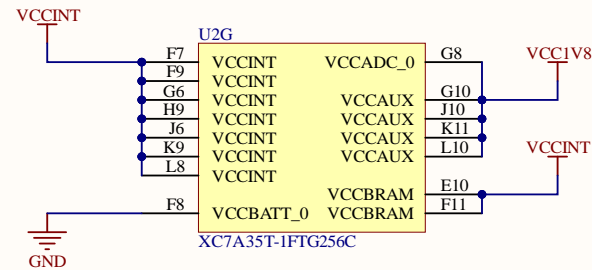
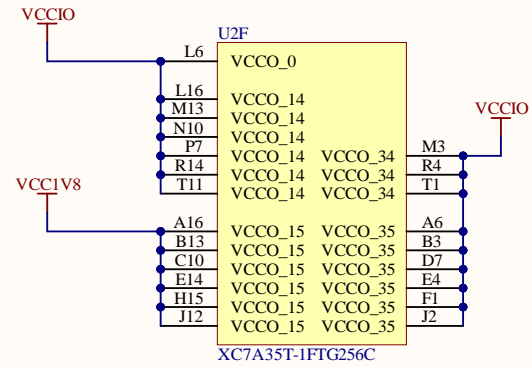
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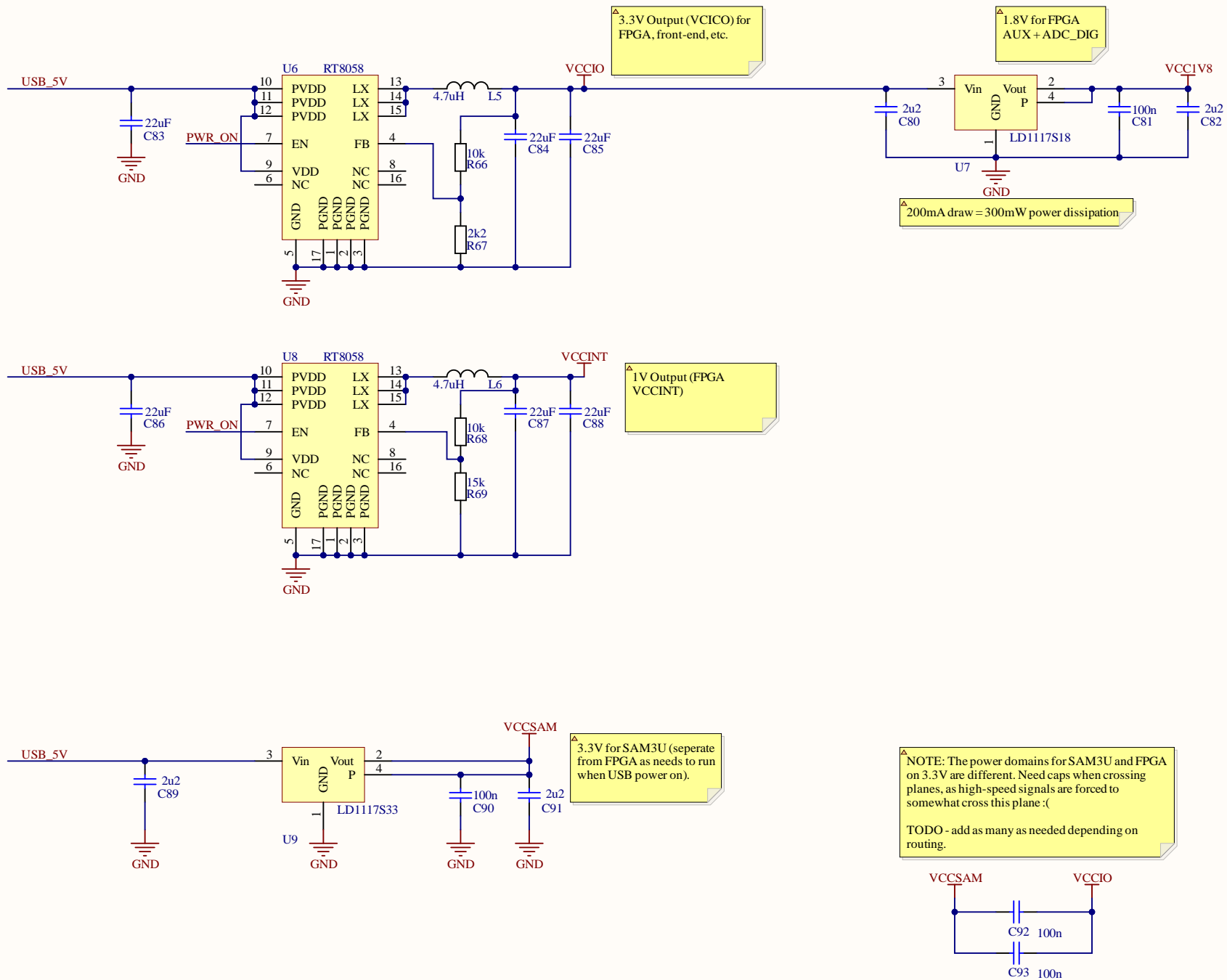
Sheet 3 of 9

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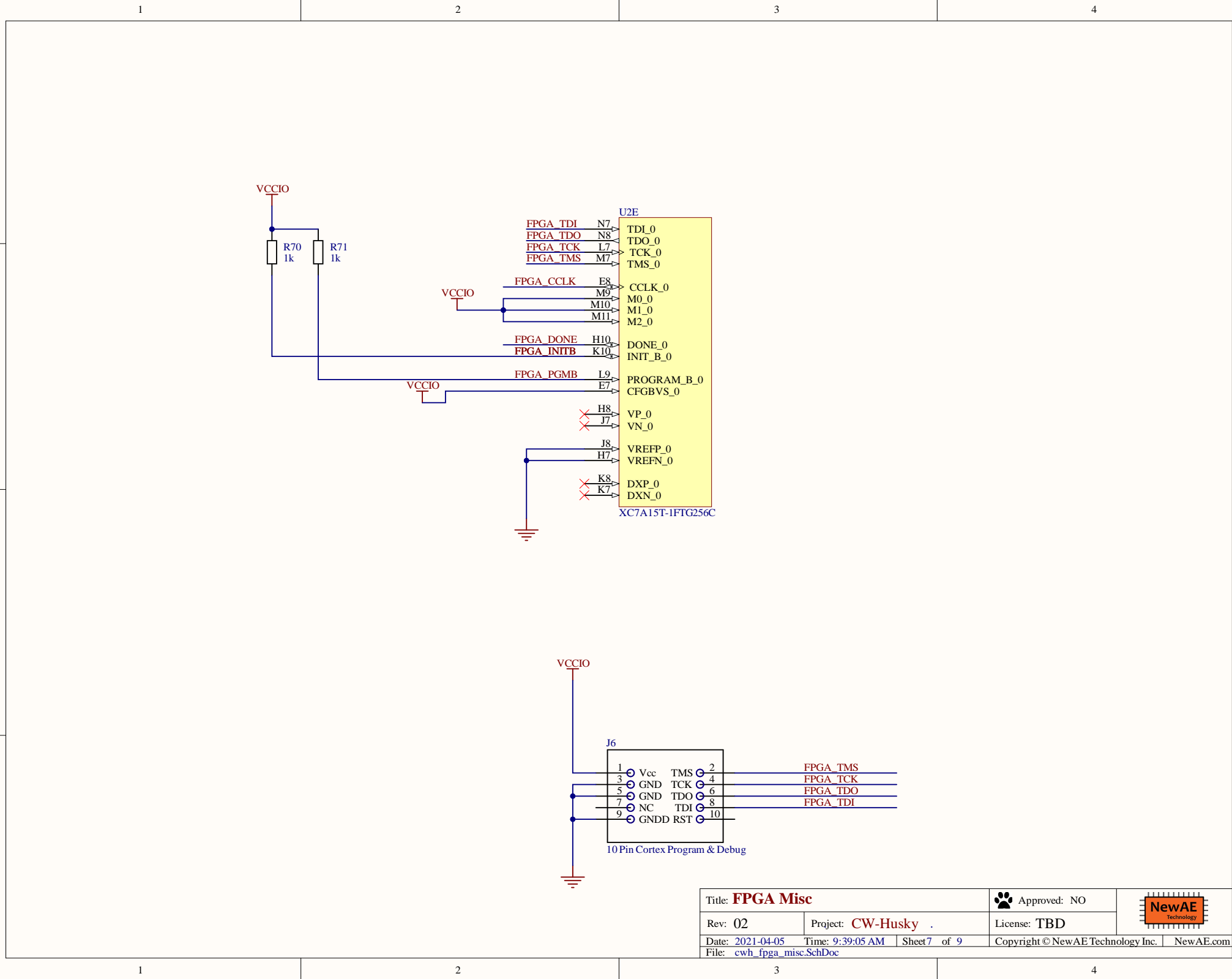
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Title: **FPGA Misc**

Approved: NO

Rev: 02

Project: CW-Husky

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Date: 2021-04-05

Time: 9:39:05 AM

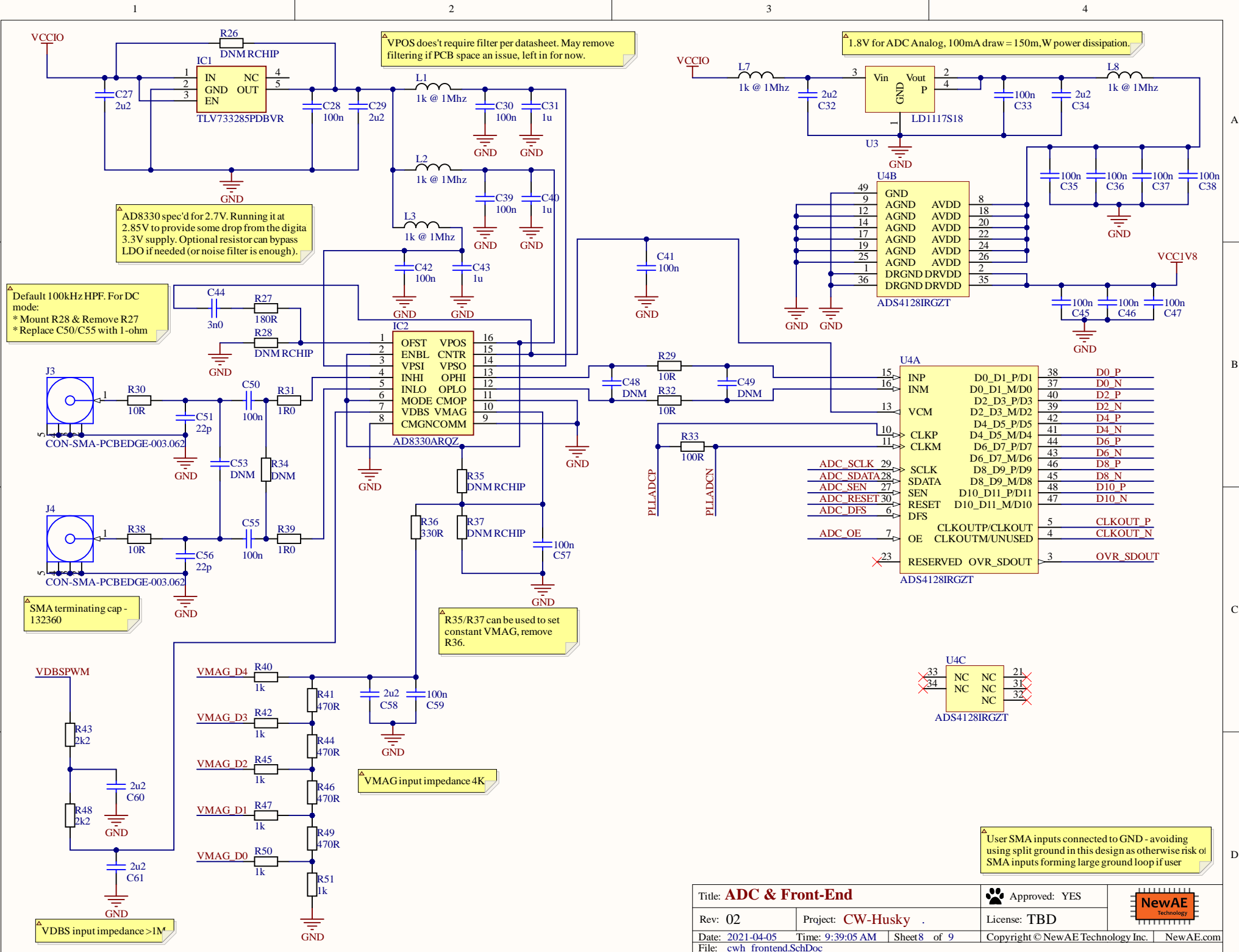
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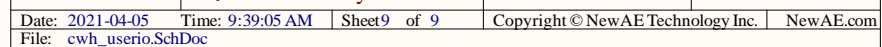
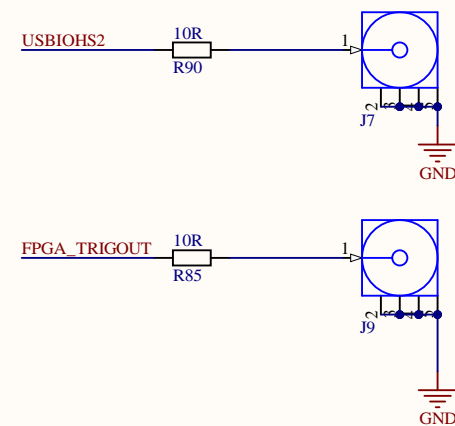
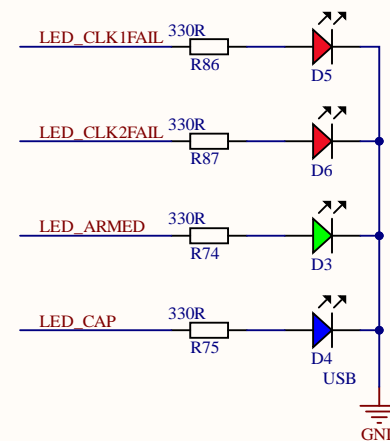
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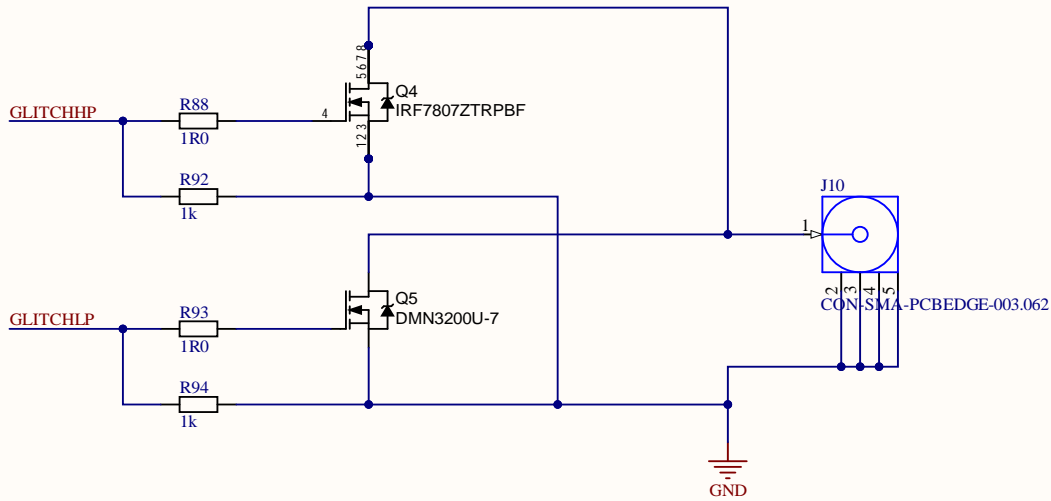
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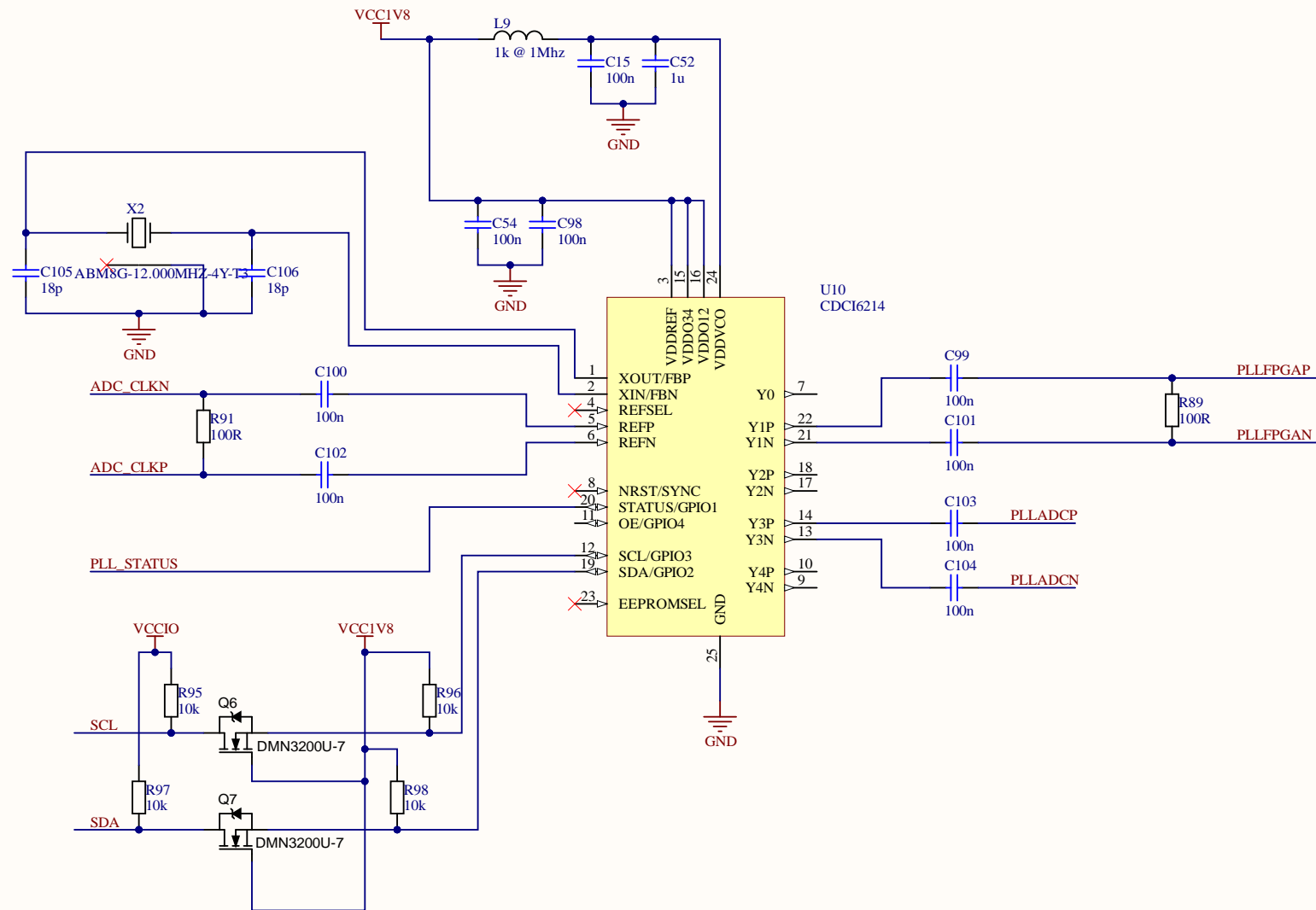












See  
<https://www.nxp.com/docs/en/application-note/AN10441.pdf>  
 for level shifting details.

Title: **PLL for ADC**

Approved: NO

Rev: 02

Project: CW-Husky

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Time: 9:39:05 AM

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