Large-scale RTL System

Higher scales of Interconnects, on- and off-chip, are envisaged. Never a grid though: Always hierarchical. Hosted algorithms must be fitted to this constraint. Internal inputs/outputs address all plugboards, and also "unconnected plugboards", used as block RAM.
MSBs of address lines have protection for zero page,
to protect any self-modifying configurations from overwriting themselves.
Selectable via internal inputs, with external jumper override.
Prebuilt POST blocks allow reading of selected address ranges,
from external ROM/Flash, negating the need for a CPLD for intialisation.
This design requires no complex external software to setup nor operate it.
External access is via the Internal inputs/outputs, controlled externally.
External control is enabled via internal flags, overridden by jumpers.
Standard JTAG and USB-JTAG interfaces should be provided "on top".
Some data-capture logging points and other custom blocks, may be added.
Intended as a parameterisable system, at the pre-synthesis stage.