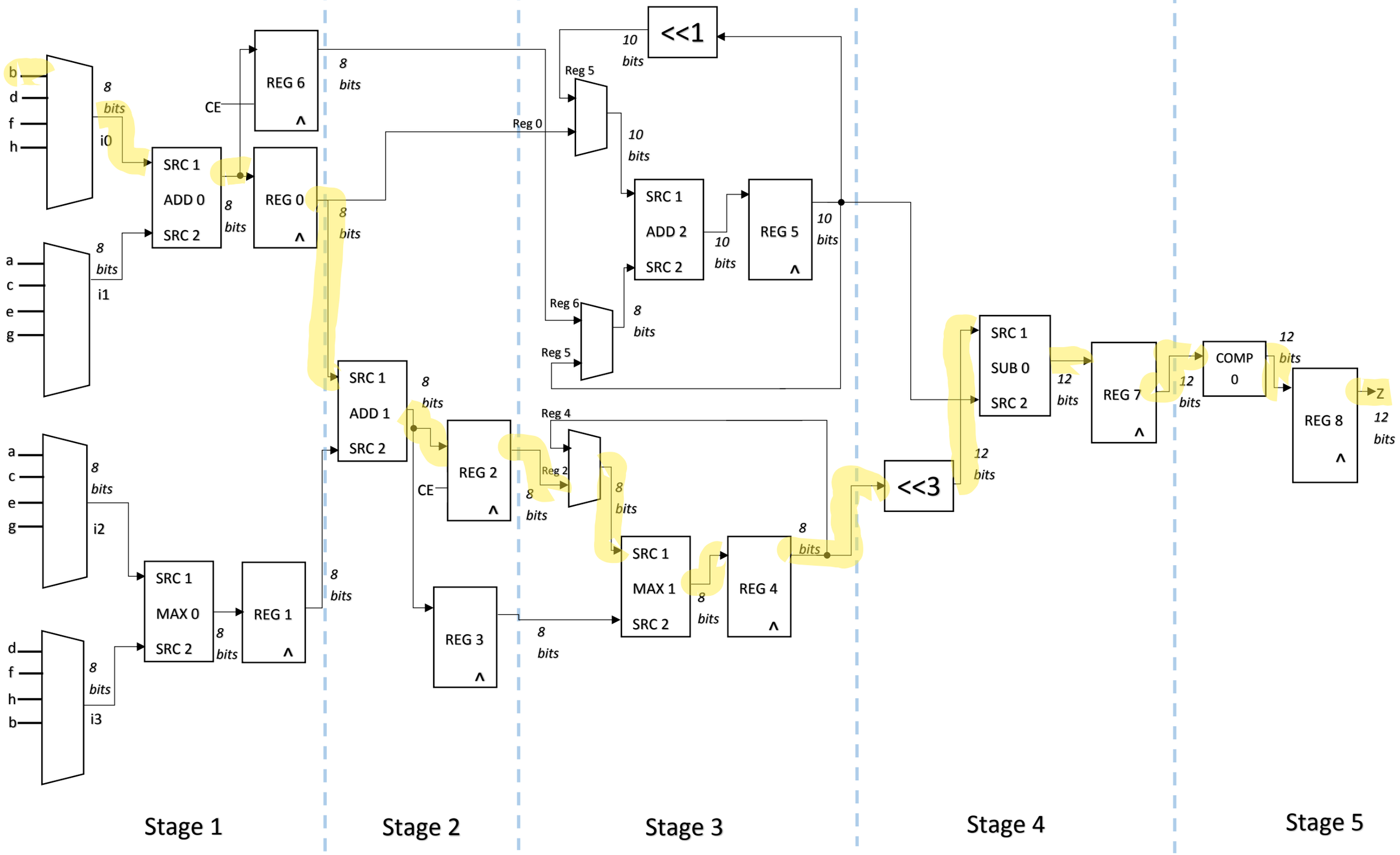
b
d
f
h
8 bits
i0
a
c
e
g
8 bits
i1
a
c
e
g
8 bits
i2
d
f
h
b
8 bits
i3
SRC 1
ADD 0
SRC 2
8 bits
REG 0
CE
REG 6
8 bits
SRC 1
MAX 0
SRC 2
8 bits
REG 1
8 bits
SRC 1
ADD 1
SRC 2
8 bits
CE
REG 2
REG 3
8 bits
Reg 0
Reg 5
10 bits
<<1
10 bits
SRC 1
ADD 2
SRC 2
10 bits
REG 5
10 bits
Reg 6
Reg 5
8 bits
Reg 4
Reg 2
8 bits
8 bits
SRC 1
MAX 1
SRC 2
8 bits
REG 4
8 bits
<<3
12 bits
SRC 1
SUB 0
SRC 2
12 bits
REG 7
12 bits
COMP
0
12 bits
REG 8
Z
12 bits
Stage 1
Stage 2
Stage 3
Stage 4
Stage 5

The equation to calculate the derivative out of all directions can be manipulated to:
MaxDeriv = max ((b + c + max(a, d)), (d + e + max(e, f)), (f + g + max(e, h)), (h + a + max(g, b)))

Scheduling Tables

Complete Table

The complete table below includes the values of all inputs, outputs, data-path components and registers that are being used, along with whether the components and registers need multiplexers/chip-enable or not:

	i/o schedule					stage 1										stage 2						stage 3								stage 4				stage 5		
clk	i0	i1	i2	i3	z	add0		max0		reg0		reg1		reg6		add1		reg2		reg3		max1		reg4		add2		reg5		sub0		reg7		comp0	reg8	
						src1	src2	src1	src2	CE	D	CE	D	CE	D	src1	src2	CE	D	CE	D	src1	src2	CE	D	src1	src2	CE	D	src1	src2	CE	D	src1	CE	D
0	b	c	a	d	-	i0	i1	i2	i3	1	add0	1	max0	1	add0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1	d	e	c	f	-	i0	i1	i2	i3	1	add0	1	max0	0	-	reg0	reg1	1	add1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2	f	g	e	h	-	i0	i1	i2	i3	1	add0	1	max0	-	-	reg0	reg1	0	-	1	add1	-	-	-	-	reg0	reg6	1	add2	-	-	-	-	-	-	-
3	h	a	g	b	-	i0	i1	i2	i3	1	add0	1	max0	-	-	reg0	reg1	-	-	1	add1	reg2	reg3	1	max1	reg0	reg5	1	add2	-	-	-	-	-	-	-
4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	reg0	reg1	-	-	1	add1	reg4	reg3	1	max1	reg0	reg5	1	add2	-	-	-	-	-	-	-
5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	reg4	reg3	1	max1	reg5 << 1	reg5	1	add2	-	-	-	-	-	-	-
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	reg4<<3	reg5	1	sub0	-	-	-
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	reg7	1	comp0
8	-	-	-	-	reg8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
MUX	Y	Y	Y	Y																		Y				Y	Y									
CE														Y				Y																		

I/O Table

The table below is just for the I/O schedule:

clk	i0	i1	i2	i3	z
0	b	c	a	d	-
1	d	e	c	f	-
2	f	g	e	h	-
3	h	a	g	b	-
4	-	-	-	-	-
5	-	-	-	-	-
6	-	-	-	-	-
7	-	-	-	-	-
8	-	-	-	-	reg8
MUX	Y	Y	Y	Y	

Register Table

The table below is just for register schedule:

clk	reg0		reg1		reg6		reg2		reg3		reg4		reg5		reg7		reg8	
	CE	D	CE	D	CE	D	CE	D	CE	D	CE	D	CE	D	CE	D	CE	D
0	1	add0	1	max0	1	add0	-	-	-	-	-	-	-	-	-	-	-	-
1	1	add0	1	max0	0	-	1	add1	-	-	-	-	-	-	-	-	-	-
2	1	add0	1	max0	-	-	0	-	1	add1	-	-	1	add2	-	-	-	-
3	1	add0	1	max0	-	-	-	-	1	add1	1	max1	1	add2	-	-	-	-
4	-	-	-	-	-	-	-	-	1	add1	1	max1	1	add2	-	-	-	-
5	-	-	-	-	-	-	-	-	-	-	1	max1	1	add2	-	-	-	-
6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	sub0	-	-
7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	comp0
8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
MUX																		
CE					Y		Y											

Component Table

The table below is just for the data-path components, which are the operators:

	stage 1				stage 2		stage 3				stage 4		stage 5
clk	add0		max0		add1		max1		add2		sub0		comp0
	src1	src2	src1	src2	src1	src2	src1	src2	src1	src2	src1	src2	src1
0	i0	i1	i2	i3	-	-	-	-	-	-	-	-	-
1	i0	i1	i2	i3	reg0	reg1	-	-	-	-	-	-	-
2	i0	i1	i2	i3	reg0	reg1	-	-	reg0	reg6	-	-	-
3	i0	i1	i2	i3	reg0	reg1	reg2	reg3	reg0	reg5	-	-	-
4	-	-	-	-	reg0	reg1	reg4	reg3	reg0	reg5	-	-	-
5	-	-	-	-	-	-	reg4	reg3	reg5 << 1	reg5	-	-	-
6	-	-	-	-	-	-	-	-	-	-	reg4<<3	reg5	-
7	-	-	-	-	-	-	-	-	-	-	-	-	reg7
8	-	-	-	-	-	-	-	-	-	-	-	-	-
MUX							Y		Y	Y			

Area Analysis

The following table shows the resource count for all the hardware the components. The area in LUTs is calculated for each stage by summing up the area of each component in the stage, which is found using the table that was provided in the manual. The total area, which is 99 LUTs, is calculated by adding the area for each stage. (note that there is no cost for shifters so they were not included)

Component	stage 1	stage 2	stage 3	stage 4	stage 5	Total
8-bit Adders	1	1	-	-	-	2
10-bit Adders	-	-	1	-	-	1
8-bit Max Operators	1	-	1	-	-	2
12-bit Subtractors	-	-	-	1	-	1
12-bit Comparators	-	-	-	-	1	1
8-bit Registers	3	2	1	-	-	6
10-bit Registers	-	-	1	-	-	1
12-bit Registers	-	-	-	1	1	2
8-bit MUXes	4	-	2	-	-	6
10-bit MUXes	-	-	1	-	-	1
Area in LUTs	34	16	30	12	7	99

Stage and Timing Analysis

clk	stage 1	stage 2	stage 3	stage 4	stage 5
0	✓				
1	✓	✓			
2	✓	✓	✓		
3	✓	✓	✓		
4		✓	✓		
5			✓		
6				✓	
7					✓
Latency	4	4	4	1	1
Overlap	0	3	3	0	0
Throughput	0.25	0.25	0.25	1.00	1.00
Tclk in ns	2.77	2.77	2.94	2.54	1.82

- Total Latency = latency for each stage – total overlap = 4 + 4 + 4 + 1 + 1 – (3 + 3) = 8 clock cycles
- Throughput is minimum throughput from all stages = ¼
- The minimum possible clock period is the slowest of all the stages from the table, which is 2.94ns. Therefore, the maximum achievable clock speed is 1 / 2.94ns = 340 MHz.
- The critical path has been identified in the hardware schematic, calculated using the slowest path from each stage. The slowest path in each stage is the shown by the Tclk for each stage, which was calculated using the delays provided in the table in the project manual.