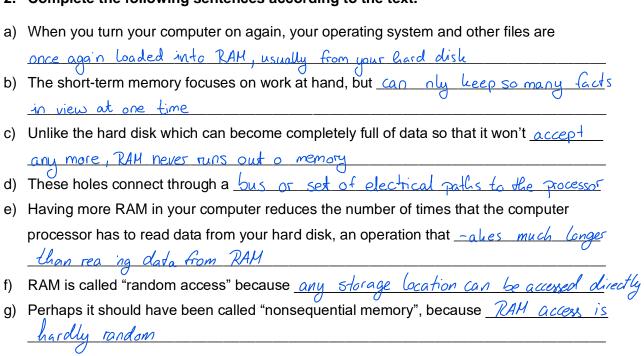
## **Working with RAM**

## 1. From which chapter do the following statements come from?

	ST	ATEMENTS
2	a)	RAM access time is expressed in nanoseconds;
4	b)	In RAM, this set of post-office boxes is known as an array and each box is a cell.
1	c)	RAM is much faster to read from and write to than the other kinds of storage in a computer.
5	d)	This address is sent to the RAM controller.
4	e)	A transistor acts as a gate in determining whether the value in the capacitor can be read or written.
1	f)	When you turn the computer off, RAM loses its data.
3	g)	RAM is organized and controlled in a way that enables data to be stored and retrieved directly to specific locations.
6	h)	Access time consists of latency and transer time.
5	i)	A capacitor with a charge over a certain voltage level represents the binary value of 1 and a capacitor with less than that charge represents a 0.
2	j)	RAM is small, both in physical size (it's stored in microchip modules) and in the amount of data it can hold.
4	k)	There is an address line for each row and each column in the set of boxes.
4	I)	To add memory to your computer, you simply add more RAM modules in a prescribed configuration.
2	m)	RAM comes in the form of "discrete" (meaning separate) microchip modules that plug into holes in the computer's motherboard.

## 2. Complete the following sentences according to the text.



h)	Every computer comes with a small amount of ROM that holds just enough programming		
	so that the operating system can be loaded into RAH each time the computer is turned on		
i)	In general, RAM is much like an arrangement of post-office boxes in which each box can hold a 0 or a 1		
j)	In describing a RAM chip or module, a notation such as 256Kx16 means 256 thousand		
	columns of cells standing 16 rows deep		
k)	In static RAM, instead of a capacitor-held charge, the transistor itself is <u>a positional</u>		
	-lip/flop switch, with one position meaning O and one position meaning 1		
l)	For dynamic RAM, before a capacitor is read, it must be power-refreshed to ensure that the		
	value read is valid.		
m)	The data that is read is transmitted along the data lines to the processor's nearby data buffer known as		
	level-1 cache and another copy may be held in level-2 cache or level-3 cache		
n)	The amount of time that RAM takes to write or to read it once the request has been		
	received from the processor is called the access time		
o)	Latency is the time to coordinate signal timing and refresh after reading it		
3.	Fill the gaps in the text with the correct word or expression from the box.		
<b>+</b> C	access + appropriate + based + bit + bitlines + bucket + capacitors  bircuitry + computer memory + counter + determines + directly + downside  etched + integrated circuit + leak + memory controller + rating + recharge  efresh operation + switch + wafer + wordlines		
Ra	indom access memory (RAM) is a form of <u>computer memory</u> . RAM is considered		
	indom access" because you can <u>a ccess</u> any memory cell		
	directly if you know the row and column that intersect at that cell.		
	AM data can be accessed in any order.		
Sir	milar to a microprocessor, a memory chip is an <u>integrated circuit</u> (IC) made		
of	millions of transistors andapacitorIn this form of computer		
	emory, dynamic random access memory (DRAM), a transistor and a capacitor are paired		
	create a memory cell, which represents a singlebit of data. The		
	pacitor holds the bit of information a 0 or a 1. The transistor acts as a		
_	<u>switch</u> that lets the control <u>circuit</u> on the		
	emory chip read the capacitor or change its state.		
	capacitor is like a small bucket that is able to store electrons. To store a 1		
in the memory cell, the bucket is filled with electrons. To store a 0, it is emptied. The problem			
****	th the capacitor's bucket is that it has aeak In a matter of a few		

Therefore, for dynamic memory to work, either the CPU or the memory controller has to
come along and <u>recharge</u> all of the capacitors holding a 1 before they
discharge. To do this, the <u>memory controller</u> reads the memory and then
writes it right back. This happens automatically
thousands of times per second.
This refresh operation is where dynamic RAM gets its name. Dynamic RAM has to be
dynamically refreshed all of the time or it forgets what it is holding. The
<u>downside</u> of all of this refreshing is that it takes time and slows down the
memory.
Memory cells are elded (= gentled) onto a silicon water in an array of
columns ( <u>biflines</u> ) and rows ( <u>wordlines</u> ). The
intersection of a bitline and wordline constitutes the address of the memory cell.
DRAM works by sending a charge through the column (CAS) to
activate the transistor at each bit in the column. When writing, the row lines contain the state
the capacitor should take on. When reading, the sense-amplifier <u>determines</u>
the level of charge in the capacitor. If it is more than 50 percent, it reads it as a 1; otherwise it
reads it as a 0. The tracks the refresh sequence
on which rows have been accessed in what order. The length of
time necessary to do all this is so short that it is expressed in nanoseconds (billionths of a
second). A memory chiprating of 70ns means that it takes 70
nanoseconds to completely read and recharge each cell.

