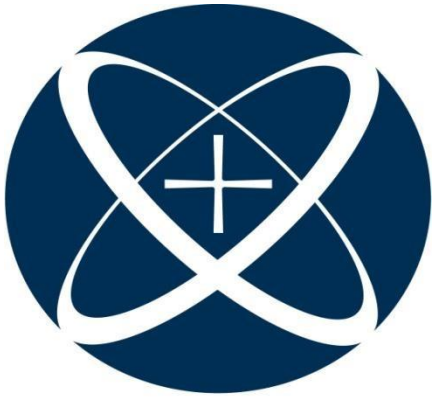
Instituto Tecnológico y de Estudios Superiores de Occidente – ITESO



ITESO

Universidad Jesuita de Guadalajara

Materia: Diseño y Verificación de sistemas digitales

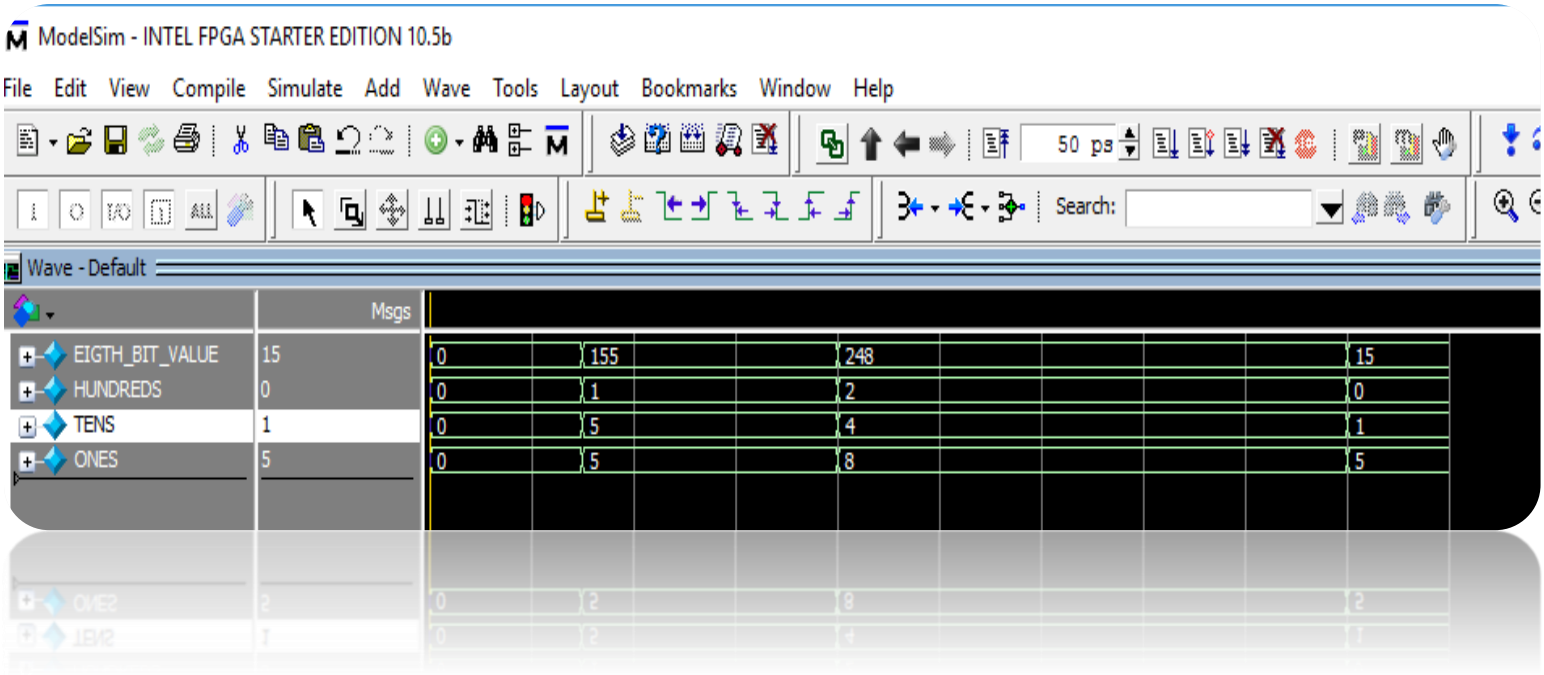
Maestro: Abasí Ramírez

Tarea#: 2

Fecha: 05/02/2019

Alumno: Robin Moisés Salgado de Anda- ie686481

Just as demostration of the functionality of the combinational binary_To_BCD module I simulate three differents values in the test bench 155,248 and 15.



Flow Summary

<<Filter>>

Flow Status	Successful - Tue Feb 12 20:38:58 2019
Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ Lite Edition
Revision Name	binary_to_BCD_Two
Top-level Entity Name	binary_to_BCD
Family	Cyclone IV E
Total logic elements	32
Total registers	0
Total pins	18
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0