EEE - 313 Electronic Circuit Design
Lab - 4

Robin Umut Kızıl
Section - 2
22003260

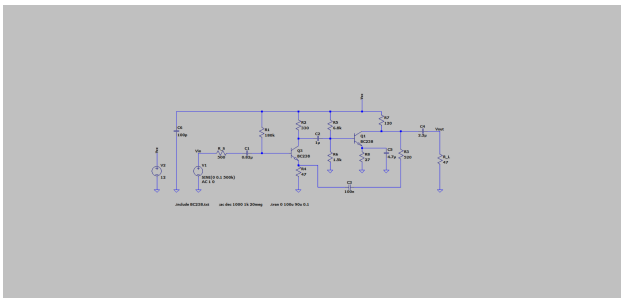

Fig. 1: Circuit

R4 and R8 values will be tested by selecting their voltages as 1V.
Then, the ratios were chosen so that the bias voltages of the BJTs were 1.7 V for R1. R5 values chosen for $(12 - 1.7V)/I_{R5} = 6.8k$ and R6 is chosen for correct it.
By testing R2 and R7 values, the gain was maximized by increasing them without disturbing the ACT state of the BJTs. Capacitor values were chosen according to DC-block and bypass status.

Specification 1: The Current Consumption is Less Than 70mA

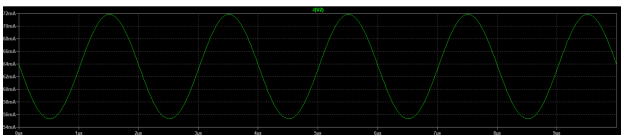

Fig. 2: $0.1V$ Sinusoidal Input Circuit

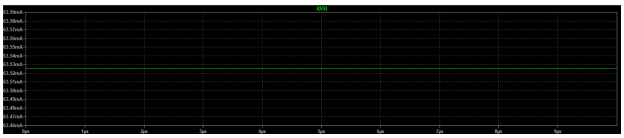

Fig. 3: Quiescent Condition Circuit

It can seen that, Vcc current is less then the 70mA.

Specification 2: The Small-Signal Bandwidth is at Least 5KHz-5MHz While the Mid-Band Gain is 20dB±0.5dB

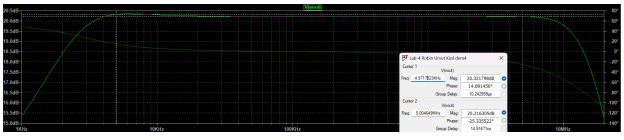

Fig. 4: 5kHz to 5mHz Measurement

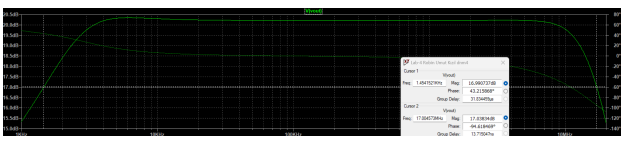

Fig. 5: -3dB Bounds

Circuit is give 20dB gain between 5kHz and 5Mhz and -3dB bounds are at least 5KHz-5MHz.

Specification 3: The Harmonic Content of the Output Voltage is Better Than 30dBc With 0.1V Peak Input signal at 500KHz

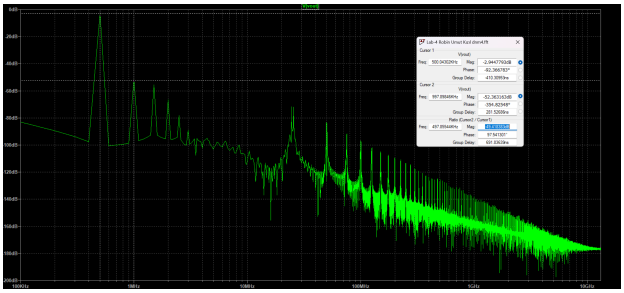

Fig. 6: Harmonics

with -49dBc, the harmonic content of the output voltage is better.

Specification 4: The Small-Signal Input Impedance of the Amplifier at 500KHz

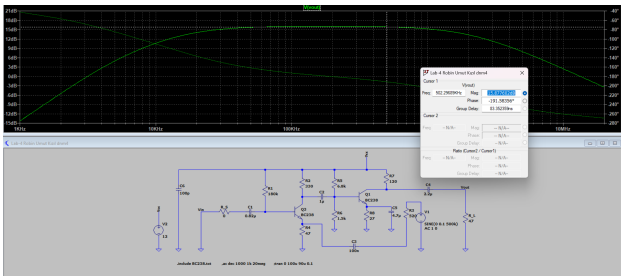

Fig. 7: Voltage gain of V_{out} at 500kHz with 0 input resistance

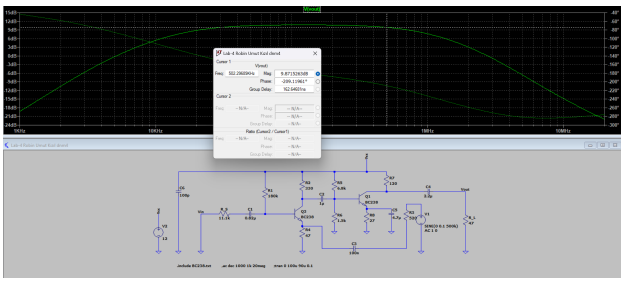

Fig. 8: Voltage gain of V_{out} at 500kHz with 0 input resistance 11.1k

The Small-Signal Input Impedance is 11.1k Ω.

Specification 5: The Small-Signal Output Impedance of the Amplifier at 500KHz

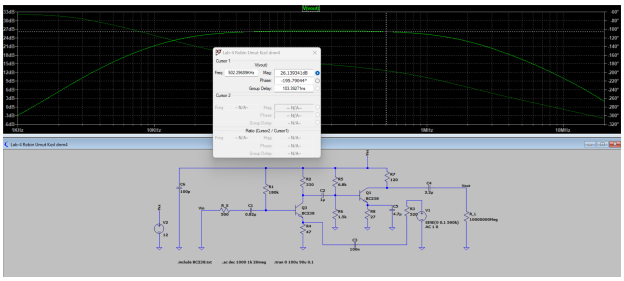

Fig. 9: Voltage gain of V_{out} at 500kHz with 0 Output resistance ∞ Ω

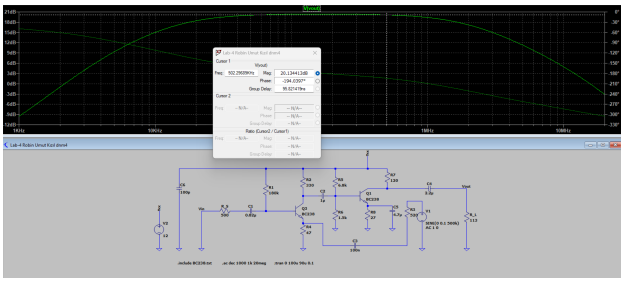

Fig. 10: Voltage gain of V_{out} at 500kHz with 0 Output resistance 113Ω

the small-signal output impedance is 113 Ω.

Specification 6: The Phase Margin of the Open-Loop System

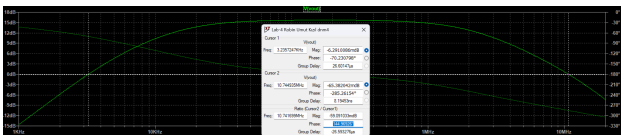

Fig. 11: phase of Output gain

The Phase Margin of the Open-Loop System is:

$$360 - 144.9692 = 215.0308$$

DipTrace

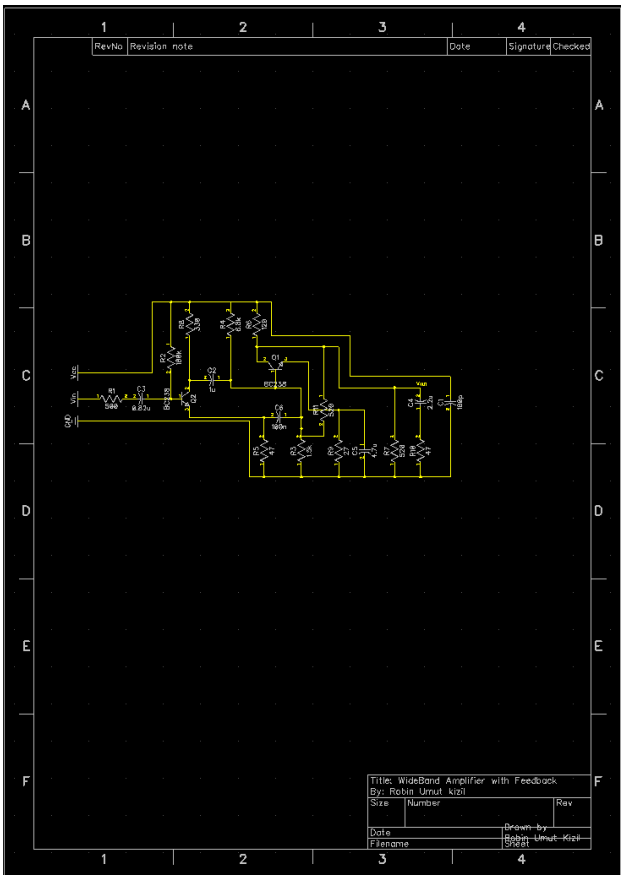

Fig. 12: DipTrace Circuit 1

#	RefDes	Value	Name	Pattern
1	C1	100p	CAP100	CAP-2.54/6.6x3
2	C2	1u	CAP100	CAP-2.54/6.6x3
3	C3	0.82u	CAP100	CAP-2.54/6.6x3
4	C4	2.2u	CAP100	CAP-2.54/6.6x3
5	C5	4.7u	CAP100	CAP-2.54/6.6x3
6	C6	100n	CAP100	CAP-2.54/6.6x3
7	Q1	BC238	FZT651TA	SOT223-4P230_700X165L95X70N
8	Q2	BC238	FZT651TA	SOT223-4P230_700X165L95X70N
9	R1	500	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
10	R2	180k	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
11	R3	1.5k	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
12	R4	6.8k	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
13	R5	47	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
14	R6	120	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
15	R7	520	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
16	R8	330	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
17	R9	27	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
18	R10	47	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
19	R11	520	CFR25SJR-52-100K	RESAD730W45L370D210_AD1

Fig. 13: DipTrace table 1

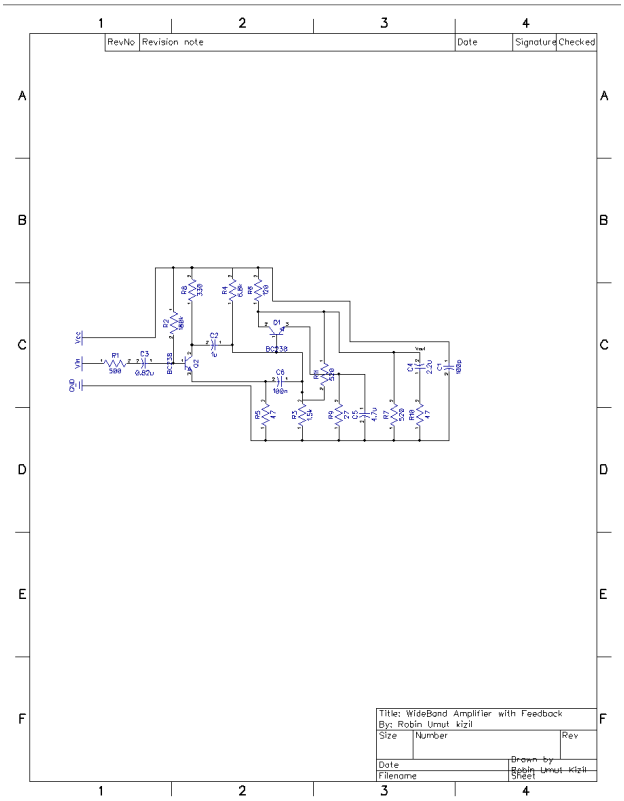

Fig. 14: DipTrace Circuit 2

#	RefDes	Value	Name	Pattern
1	C1	100p	CAP100	CAP-2.54/6.6x3
2	C2	1u	CAP100	CAP-2.54/6.6x3
3	C3	0.82u	CAP100	CAP-2.54/6.6x3
4	C4	2.2u	CAP100	CAP-2.54/6.6x3
5	C5	4.7u	CAP100	CAP-2.54/6.6x3
6	C6	100n	CAP100	CAP-2.54/6 6x3
7	Q1	BC238	FZT651TA	SOT223-4P230_700X165L95X70N
8	Q2	BC238	FZT651TA	SOT223-4P230_700X165L95X70N
9	R1	500	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
10	R2	180k	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
11	R3	1.5k	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
12	R4	6 8k	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
13	R5	47	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
14	R6	120	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
15	R7	520	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
16	R8	330	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
17	R9	27	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
18	R10	47	CFR25SJR-52-100K	RESAD730W45L370D210_AD1
19	R11	520	CFR25SJR-52-100K	RESAD730W45L370D210_AD1

Fig. 15: DipTrace table 2