EEE - 202 Circuit Theory
Lab - 5

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Section - 2
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I. Software Implementation

1) Introduction

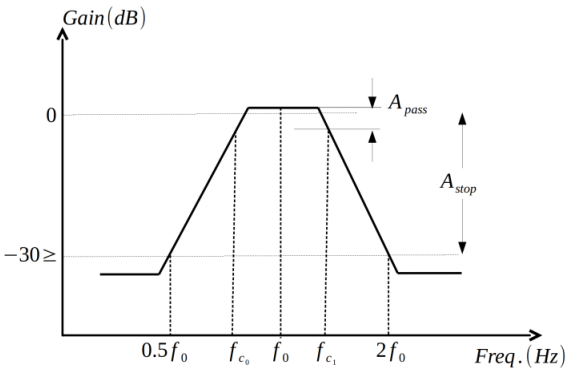


Fig. 1: Frequency response of the filter

In this lab, we are asked to design a circuit with the gain graphic in figure 1 on 50Ω resistance with these speculations;

- Central frequency: $2Mhz \leq f_0 \leq 5Mhz$
- Passband width: $f_{c_1} f_{c_0} = 0.05 * f_0$
- Gain variation in the passband: $A_{pass} \leq 3dB$
- Stopband attenuation: $A_{stop} \geq 30dB$

2) Analysis

The selected frequency value is 3 MHz and, a butterwortworth filter will be created using a 2nd order filter in order to make hardware implementation easier.

First of all, Δf must calculated;

$$\Delta f = 0.05 * f_0 = 0.05 * 3 * 10^6 = 150kHz$$

k	C_1	L_2	C_3	L_4	C_5
2	1.414	1.414			
3	1.000	2.000	1.000		
4	0.765	1.848	1.848	0.765	
5	0.618	1.618	2.000	1.618	0.618

Fig. 2: Low-Pass Butterwort Filter Coefficents table

Now the capacitor and inductor values of the low-pass filter of the butterworth filter should be calculated. 2 order line of the the Low-Pass Butterwort Filter coefficents table can be used for this.

$$C_1 = \frac{1.414}{2*\pi*R*\Delta f} = \frac{1.414}{2*\pi*50*150*10^3} = 3.10^{-8} = 30nF$$
$$L_1 = \frac{1.414*R}{2*\pi*\Delta f} = \frac{1.414*50}{2*\pi*150*10^3} = 7.5.10^{-5} = 75uH$$

With the values in the low pass filter, the remaining inductor and capacitor values in the butterworth filter can be calculated.

$$C_2 = \frac{1}{(2*\pi*f_0)^2*C_1} = \frac{1}{(2*\pi*3*10^6)^2*75*10^{-6}} = 37.5pH$$
$$L_2 = \frac{1}{(2*\pi*f_0)^2*L_1} = \frac{1}{(2*\pi*3*10^6)^2*3*10^{-8}} = 93.8nH$$

Using the values found, the following circuit is obtained.

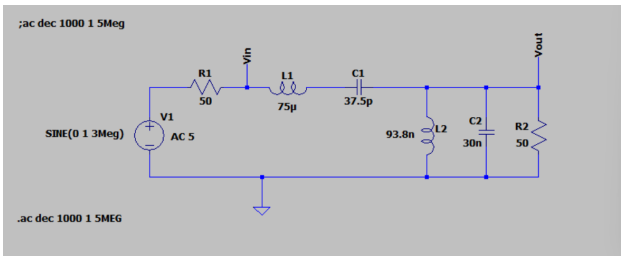


Fig. 3: 2. order butterworth circuit

3) Simulation

This section will show the simulation of the butterworth filter circuit.

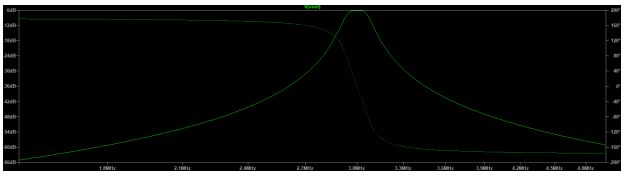


Fig. 4: Vout voltage of the butterworth circuit

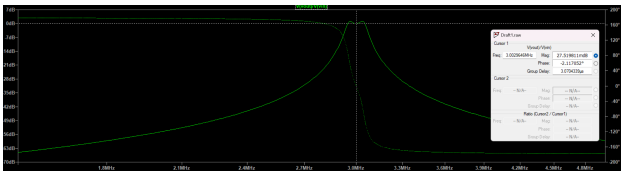


Fig. 5: gain of the butterworth circuit with center freq.

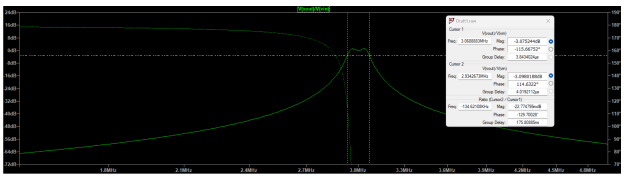


Fig. 6: Cut-off freq. the butterworth circuit

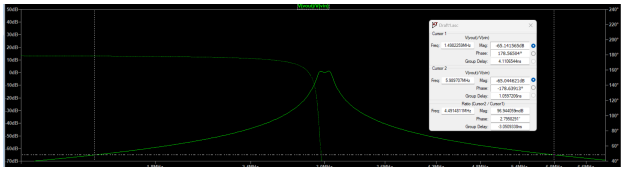


Fig. 7: A_{band} of the butterworth circuit

Frequency	Gain
1.5MHz	-65.14dB
2.93MHz	-3.1dB
3MHz	0dB
3.06MHz	-3.0.7dB
3MHz	-65dB

TABLE I: Table of freq.

component	calculation	simulation	error rate
Δf	150	135	10.6%

TABLE II: Error rate of Δf

II. Hardware implementation

In this section, hardware will be implemented with calculated circuit. yellow signal is input voltage and blue is output if no other specification.

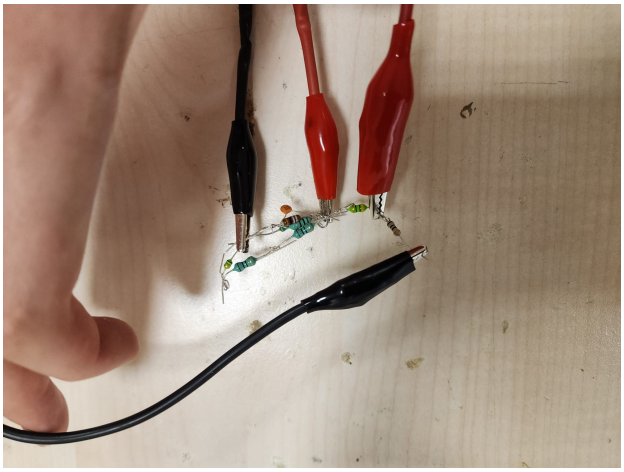


Fig. 8: Hardware implementation of the butterworth circuit

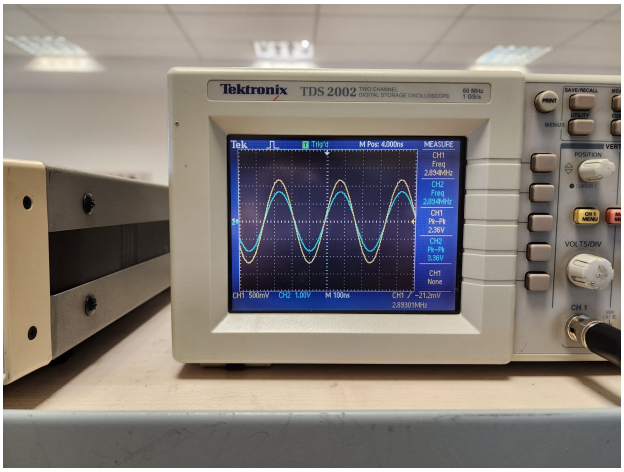


Fig. 9: Circuit with 2.89 freq.

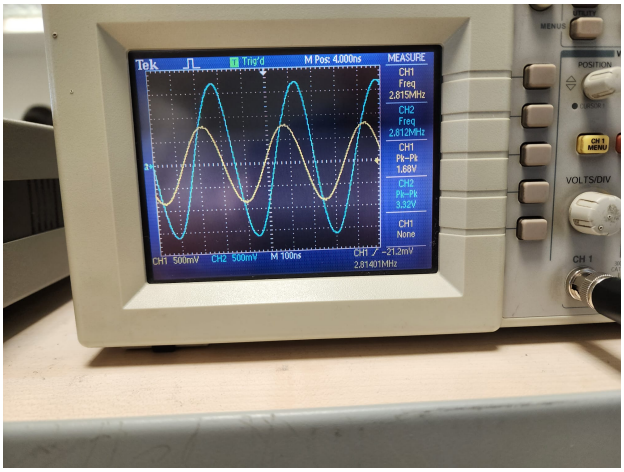


Fig. 10: Circuit with 2.81 freq.

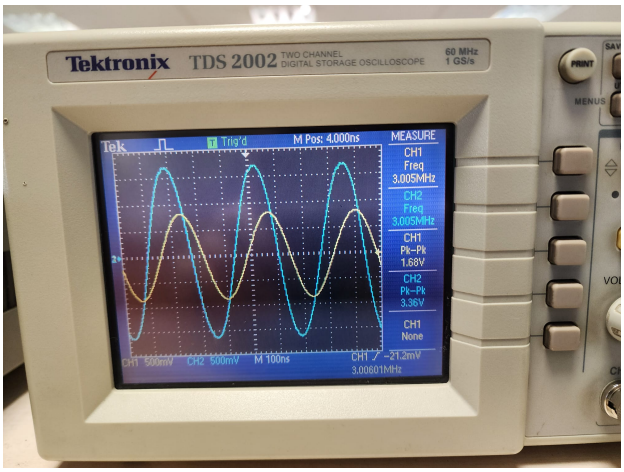
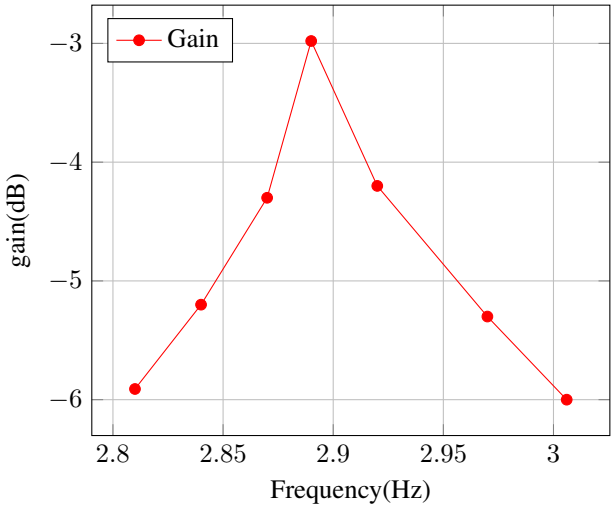


Fig. 11: Circuit with 3.006 freq.

TABLE OF GAIN



Frequency(Hz)	Gain(dB)
1.4MHz	-72dB
2.81MHz	-5.91dB
2.84MHz	-5.2dB
2.87MHz	-4.3dB
2.89MHz	-2.98dB
2.92MHz	-4.2dB
2.97MHz	-5.3dB
3.006MHz	-6dB
6MHz	-76dB

TABLE III: Frequency and gain table

component	software	hardware	error rate
center freq.	3Mhz	2.89Mhz	3.66%
cut-off freq. 1	3.06Mhz	2.81Mhz	8.16%
cut-off freq. 2	2.93Mhz	3.006Mhz	2.4%

TABLE IV: Error rate of freq.

Conclusion

As a result, in order to build a circuit with the desired values, we first chose to build a 2nd order butterworth filter. Then the values of the components in it were calculated. After that this circuit was simulated and the hardware was implemented. There is a error rate due to the hard to implement of hardware inductors(no suitable values in lab). While there was no error rate for the center frequency values in the software, an error not exceeding 10% was obtained in the hardware. All the remaining specifications have been fulfilled. So this experiment was successful.