EEE- 202 Circuit Theory
Lab-4

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Section - 2
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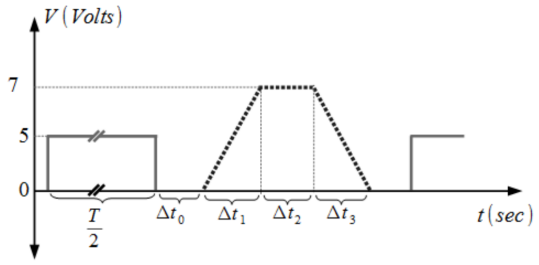
I. Software Implementation

1) Introduction

In this lab, we are asked to design a circuit according to the graph and values in figure 1.



$\Delta t_0 = 3ms, \quad \Delta t_1 = 3ms, \quad \Delta t_2 = 2ms, \quad \Delta t_3 = 2ms$

Input peak voltage: $5V$

Output peak voltage: $7V$

Input frequency: $f < 50Hz, \quad T = \frac{1}{f}$

Fig. 1: Graph of the circuit that to be made

The selected period value is 100ms.

2) Analysis

To complete this circuit, 3 types of opamps must be used:

- Comparator opamp (To create delay)
- Integrator opamp
- Subtractor opamp

a) Comparator opamp

In this type of opamp, if the (+) terminal is greater than the (-) terminal, the output voltage is equalized to the upper value (7 V), if less, it is equalized to the lower value (0 V). Delays are added to this circuit bu using this system, capacitors and resistors. Vccs will be chosen at simulation (with a value found by trying is 8.5V) in order to create delayed signals equals to 7 V.

The comparator opamp is as follows:

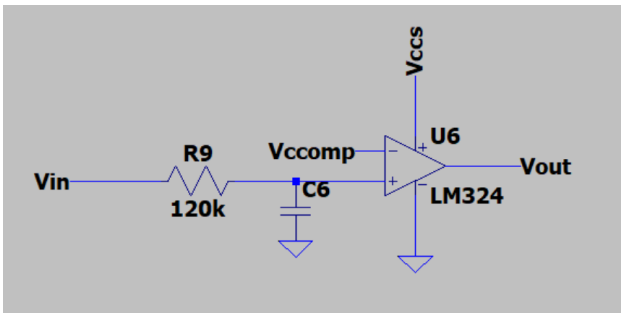


Fig. 2: Circuit of comparator opamp

$$\frac{dV_c}{dt} * C + \frac{V_c - V_{in}}{R} = 0$$

$$\frac{C * dV_c}{dt} + \frac{V_c}{R} = \frac{V_{in}}{R}$$

By solving equation with $V_c(i) = 0, V_c(f) = 5$:

$$V_c(t) = 5 - 5 * e^{\frac{-t}{R*C}}$$

In order to create 3ms and 8ms delay:

$$R_1 * C_1 = 0.0115, \text{ for } t = 8ms$$
$$R_2 * C_2 = 0.0043, \text{ for } t = 3ms$$

To simplify the hardware part, when we calculate the R's, taking C's as $100nF$:

Component	Value
R_1	$120k\Omega$
C_1	$100nF$
R_2	$100k\Omega$
C_2	$100nF$

TABLE I: Table of values of delayed opamp circuits components

b) Integrator opamp

In this section, İn order to add the desired slope to the delayed voltages, we calculated, we will integrate with the integrator opamp.

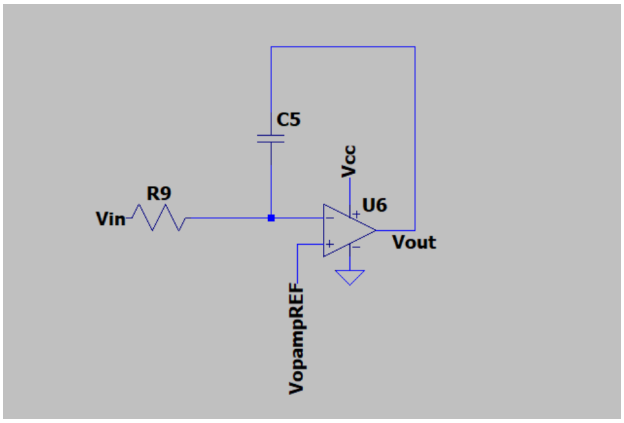


Fig. 3: Circuit of Integrator opamp

$$\frac{V_{in} - V_{ref}}{R} = C * \frac{dV_c}{dt}$$

$$\int \frac{V_{in} - V_{ref}}{R * C} = \int \frac{dV_c}{dt}$$

$$V_c = \frac{1.5}{R * C} * t$$

Signal that come from delay opamp is 7V then V_{ref} will be $5.5V$ and $V_c = 2V$.

$$R * C = \frac{3}{4} * t$$

For t= 3ms and 2ms:

$$R_3 * C_3 = 0.00225 \text{ and } R_4 * C_4 = 0.0015$$

Again to simplify the hardware part, when we calculate the C's, taking R's as $100k\Omega$ and $120k\Omega$:

Component	Value
R_3	$100k\Omega$
C_3	$22nF$
R_4	$120k\Omega$
C_4	$12nF$

TABLE II: Table of values of Integrator opamp circuits components

c) Subtractor opamp

In this section, a subtractor opamp will be designed that subtracts the 2 incoming signals from each other. so that the combination of the two signals will give the desired signal.

The subtractor opamp is as follows:

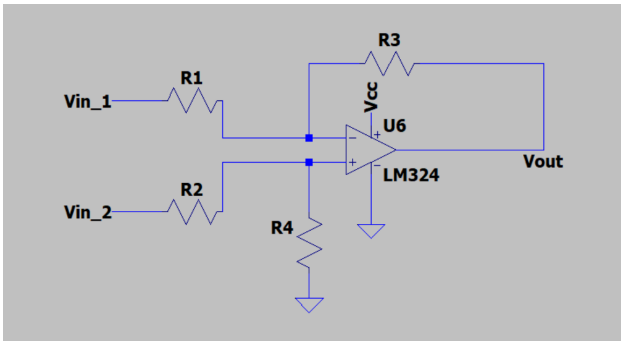


Fig. 4: Circuit of subtractor opamp

$$\frac{V_{in1}-\frac{V_{in2}*R_4}{R_2+R_4}}{R_1} = \frac{\frac{V_{in2}*R_4}{R2+R4}-V_o}{R_3}$$

$$R_3 * V_{in1} - \frac{V_{in2}*R_4*R_3}{R_2+R_4} = \frac{V_{in2}*R_4*R_1}{R_2+R_4} - V_o * R_1$$

$$V_O = \frac{\frac{V_{in2}*R_4*(R_1+R_4)}{R_2+R_4} - R_3*V_{in1}}{R_1}$$

By give same value to R's:

$$V_o = V_{in2} - V_{in1}$$

3) Simulations

In this section, green input, blue output signal unless otherwise specified.

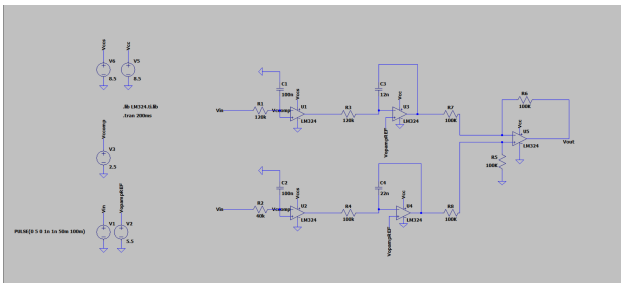


Fig. 5: Circuit at simulation

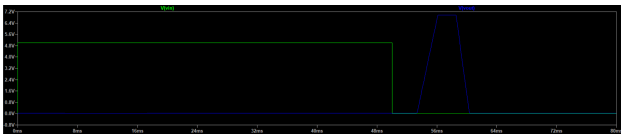


Fig. 6: Input and output signals

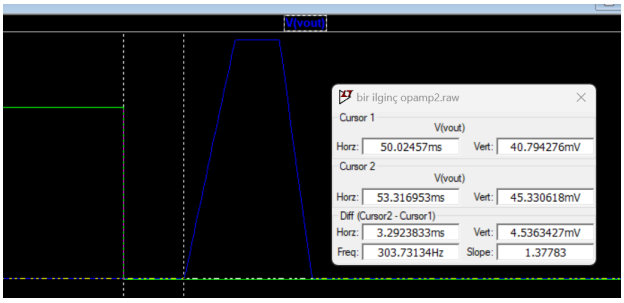


Fig. 7: 3.2ms delay

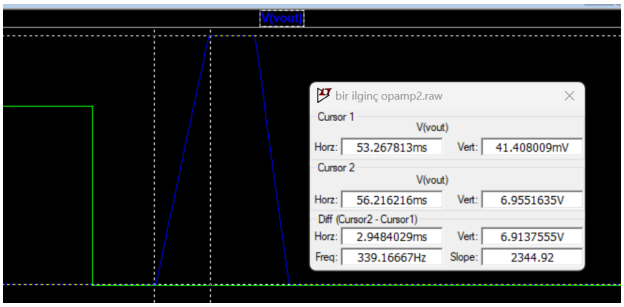


Fig. 8: 2.94ms slope

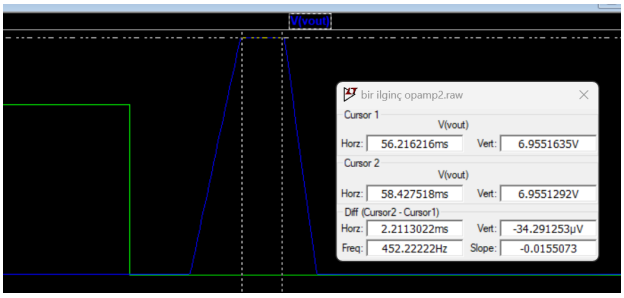


Fig. 9: 2.2ms delay

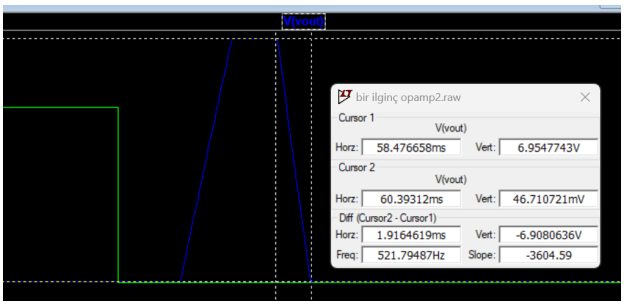


Fig. 10: 1.91ms slope

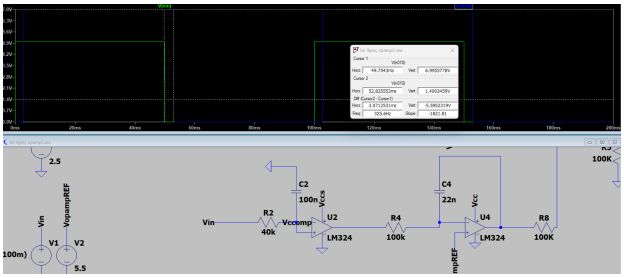


Fig. 11: Input and output of 3ms delay opamp

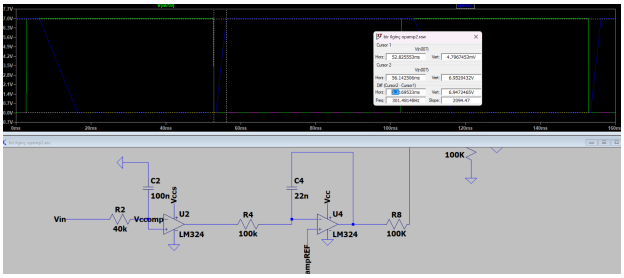


Fig. 12: Input and output of integrating opamp with 3ms

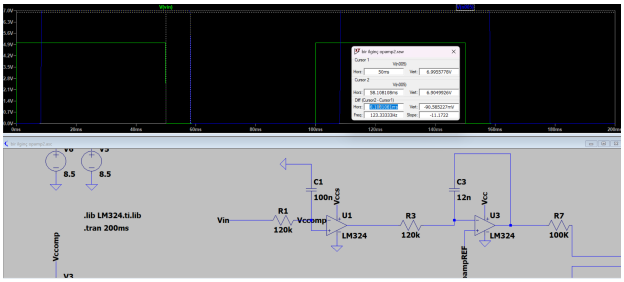


Fig. 13: Input and output of 8ms delay opamp

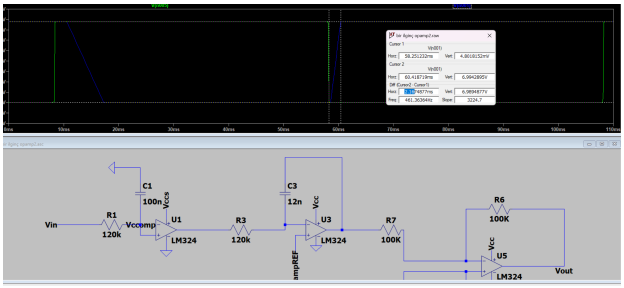


Fig. 14: Input and output of integrating opamp with 2ms

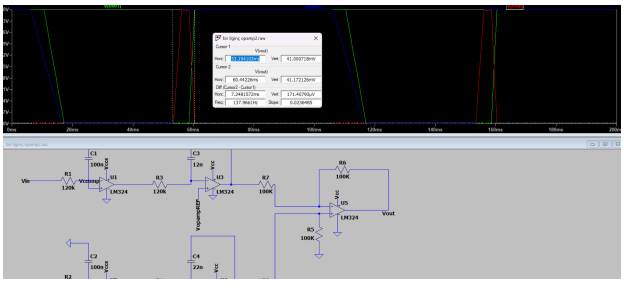


Fig. 15: Inputs and output of subtractor opamp(green and blue is input and red one is output)

times	calculation	simulation	error rate
First delay	3ms	3.2ms	6.66%
First slope	3ms	2.94ms	3.33%
second delay	2ms	2.2ms	10%
Second slope	2ms	1.91ms	4.5%

TABLE III: Error rate of times

II. Hardware implementation

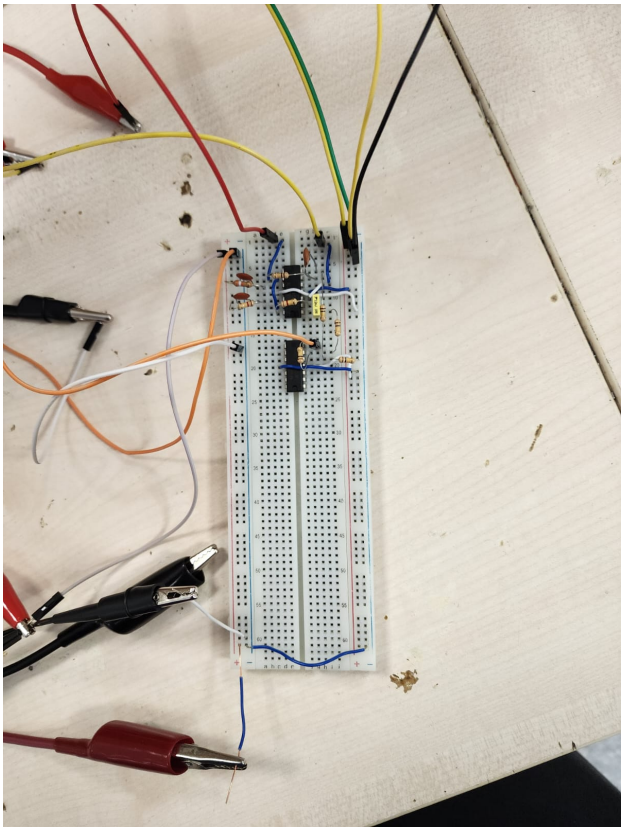


Fig. 16: Circuit at Hardware

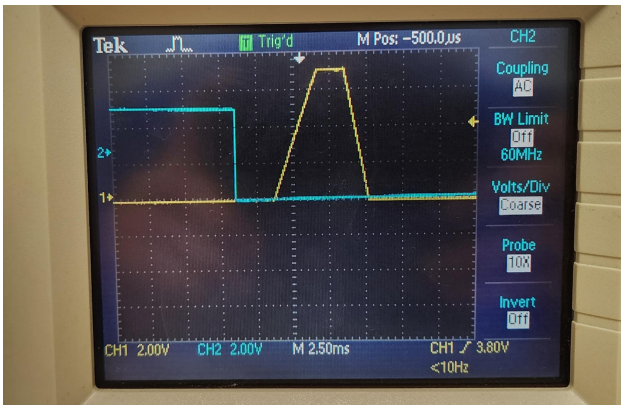


Fig. 17: Input and output signals at oscilloscope

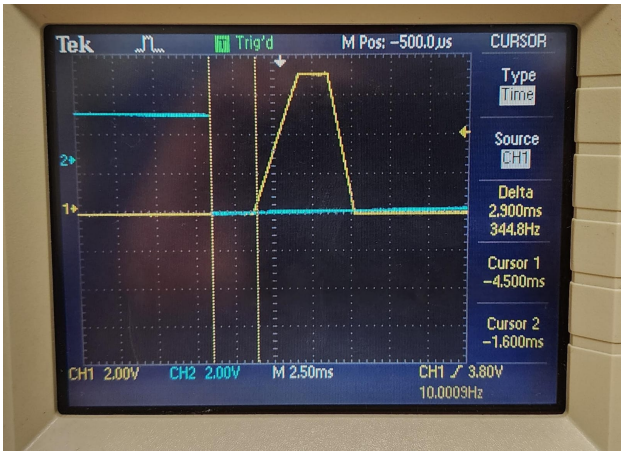


Fig. 18: First delay with 2.9ms

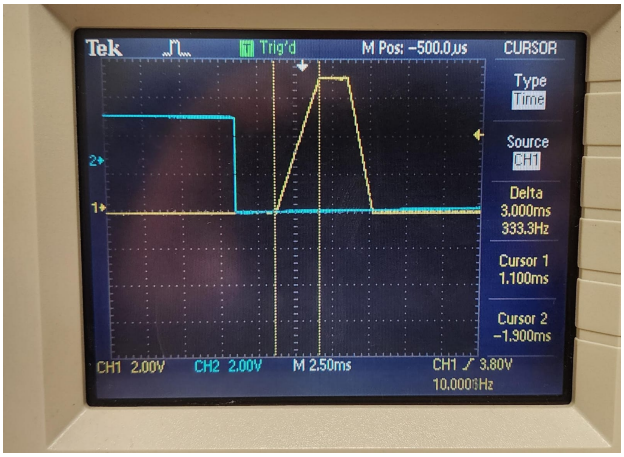


Fig. 19: slope with 3ms

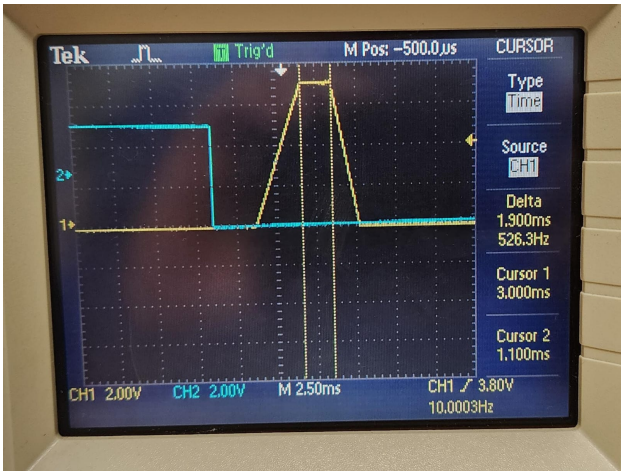


Fig. 20: Second delay with 1.9ms

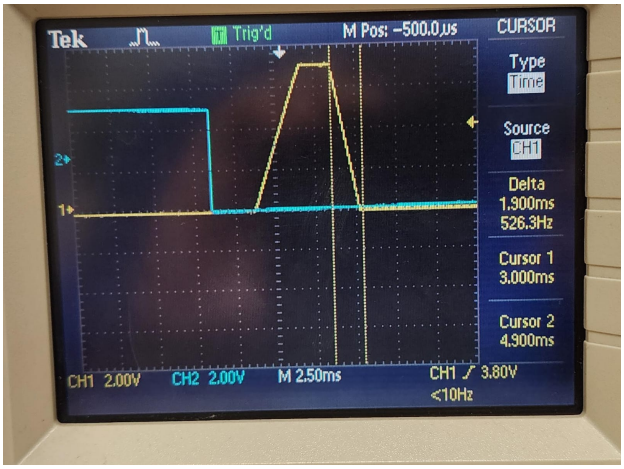


Fig. 21: Slope with 1.9ms

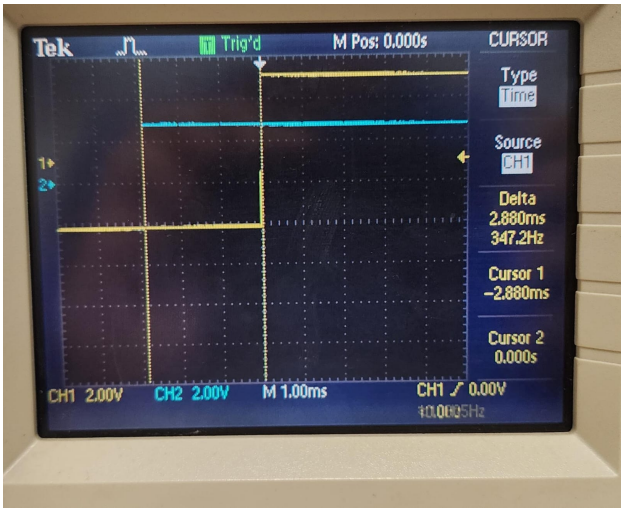


Fig. 22: First delay on 3ms delay opamp with 2.88ms

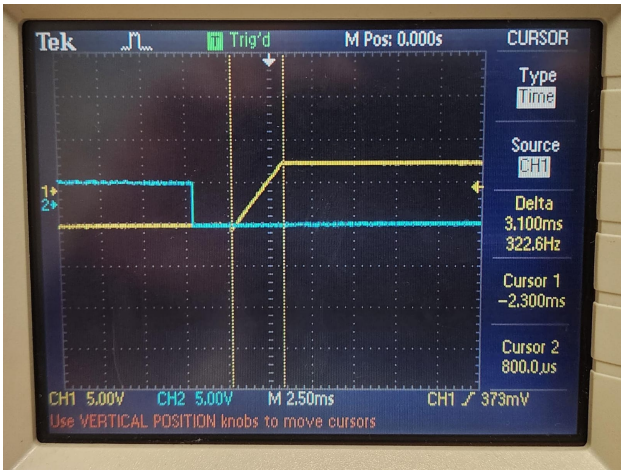


Fig. 23: First slope on Integrator opamp with 3.1ms

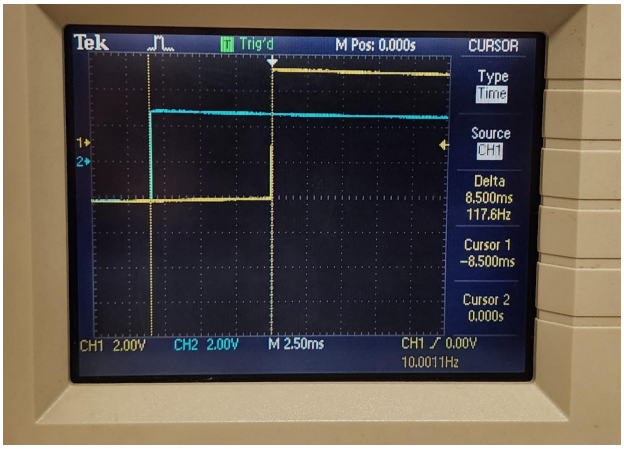


Fig. 24: Second delay on 8ms opamp with 8.5 ms delay

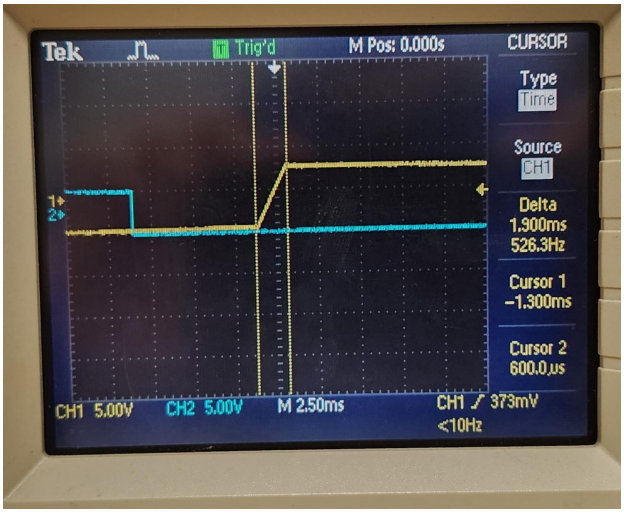


Fig. 25: Second slope with 1.9ms

times	calculation	simulation	error rate
First delay(on opamp)	3ms	2.88ms	4%
First slope(on opamp)	3ms	3.1ms	3.33%
second delay(on opamp)	8ms	8.5ms	6.25%
Second slope(on opamp)	2ms	1.9ms	5%
First delay	3ms	2.9ms	3.33%
First slope	3ms	3ms	0%
second delay	2ms	1.9ms	5%
Second slope	2ms	1.9ms	5%

TABLE IV: Error rate of times at hardware

Conclusion

As a result, a specific desired signal was obtained with the pulse voltage given in the experiment, by using a comparator opamp for delay and an integrator opamp for slope. As seen in Table III, error rates were calculated to be within acceptable values(less than or equal to 10%). Therefore the experiment is successful.