Lab 4: Arithmetic Logic Unit

The purpose of the lab is to build an Arithmetic Logic Unit (ALU). An ALU is a combinational circuit that can perform mathematical operations and is an essential building block for most digital devices .

1) Design a 6-bit ALU. The ALU needs to perform the following **eight** functions: **addition**, **subtraction**, **logical shift left, arithmetic shift right, logical shift right, comparator (with equal, less than, and greater than outputs), rotate right, and bitwise xor**. Implement it in VHDL in a modular fashion. Simulate your modules and put the **simulation results** in your report. Generate an **RTL schematic** and explain it briefly in your report. Deploy your ALU on your **FPGA** and display the outputs through LEDs. Show your schematics and working FPGA to your TA to get their approval. Include representative photos of your FPGA in your report.

Do not use operators from libraries. Implement your operations yourself. (Hint: You can first design a one-bit adder and then use this component for implementing other operations)

References:

[1] Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with VHDL Design," Fourth Edition, McGraw-Hill, 2023, Chapters 3 and 7.

[2] John F. Wakerly, "Digital Design Principles and Practices," Fourth Edition, 2001, Pearson Prentice Hall, Chapter 7.