EE313 Laboratory #4 (v3)

Wide-Band Amplifier with Feedback

Design a two-stage amplifier with feedback to achieve a low output impedance and a flat gain. You may use BJT, MOS, or both in your design. Use standard resistor values.

Specifications:

Source impedance: 500Ω

Load impedance: 47Ω

Mid band voltage Gain: 20 dB±0.5dB

Bandwidth (−3dB): at least 5KHz to 5MHz (by CNTL-Click in AC analysis)

Supply voltage: 12V (single supply)

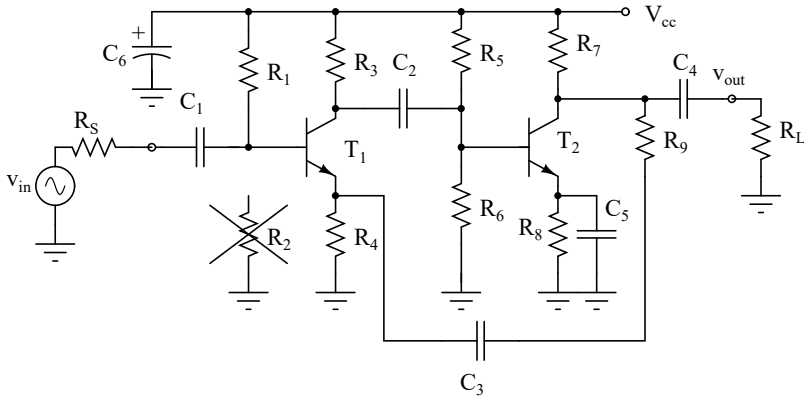
Maximum current consumption: 70mA from the supply voltage

Undistorted peak-to-peak output voltage: $2V_{pp}$ at 500KHz.

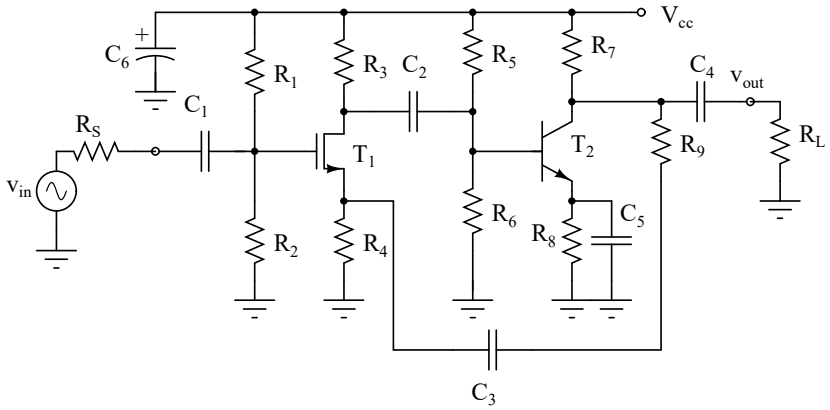
Distortion at the output: Harmonics less than −30dBc at 500KHz $2V_{pp}$ output voltage (the difference between the fundamental and the highest harmonic in FFT window)

Preliminary work (due April 23) (upload LTSpice asc file and pdf report)

Since we need a low output impedance, the feedback type should be voltage feedback. One possible solution using two BJTs and voltage-series feedback is given below. A voltage-shunt feedback is not used since that configuration will also reduce the amplifier's input impedance.



Another solution using an NMOS transistor and a BJT using voltage-series feedback is shown below.



Available transistors (BJT: BC238, NMOS: 2N7000)

First, make the amplifier's mid-band voltage gain (with R_S and R_L in place) without the feedback resistor R_9 much larger than the required 20 dB gain (about 40 dB). For this purpose, the currents in T_1 and T_2 should be chosen so that their sum is slightly less than the allowed supply current of 70 mA. It is better to reserve more current for T_2 since it has a smaller load resistance.

Choose R_4 and R_8 so that the voltage across them is about 1V.

T_1 and T_2 can be independently biased with their respective biasing resistors (R_1 for T_1 BJT, R_1 and R_2 for T_1 NMOS; and R_5, R_6 for T_2). For the BJT solution, choose the resistor R_1 so that T_1 has the desired current. (For the BJT solution, R_2 is avoided so as not to lower the input impedance.) For the NMOS solution, choose voltage divider resistors (R_1 and R_2) so that the voltage at the gate is more than V_S+V_T=3.1V. $R_1 \| R_2$ can be smaller if the NMOS gate pole limits the gain at high frequencies.

Choose R_5 so its current is about 1/20 of the T_2 collector current. R_6 can be adjusted to set the required T_2 collector current.

Choose R_3 and R_7 as large as possible to maximize the gain while keeping the transistors always in the active(BJT)/sat(NMOS) region (observe the collector/drain currents; they should be undistorted sinusoidal).

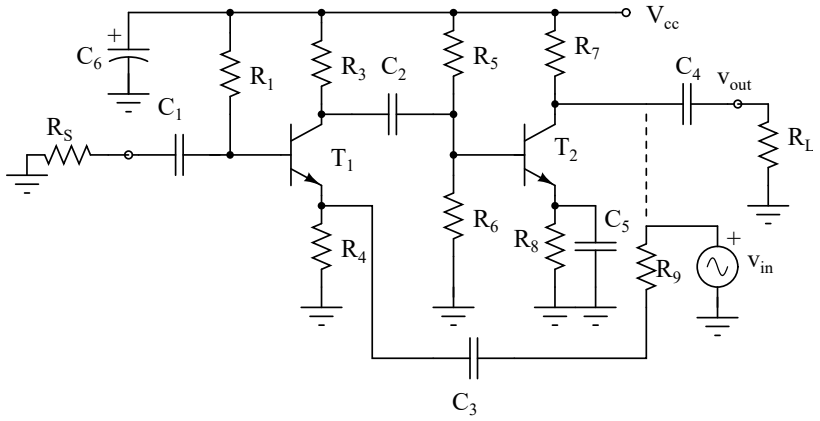
With the feedback resistor R_9 inserted, the voltage gain is given approximately by R_9/R_4. Change R_9 so that the voltage gain is nearly 20 dB.

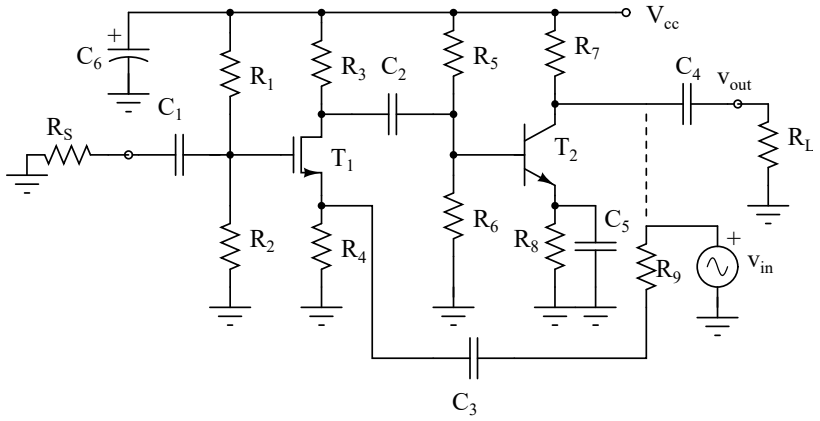
C_1, C_2, C_3, and C_4 are DC block capacitors. They should pass the lowest frequency of interest without attenuation.

C_5 is an emitter resistor bypass capacitor. Its reactance should be about $R_8 \| (1/g_{m2})$ at the lowest frequency.

C_6 is a supply bypass capacitor found in every electronic circuit to have the power supply behave like a short circuit at all frequencies. Its reactance at the lowest frequency should be about $0.1 \times V_{cc}/I_{cc}$.

To ensure the feedback circuit does not oscillate, measure the open-loop frequency response by breaking the closed-loop as shown below. Perform an AC analysis (small-signal gain), and plot v_{out} while v_{in}=1. Find the frequency where the magnitude of the voltage gain is unity (0dB). Determine the phase shift at this frequency. This phase shift should be greater than −360° by a margin for stability. The *phase margin* is the difference between this phase shift and −360°. It is preferable to have a phase margin greater than 45°.





Provide a schematic of your design, showing a component list. Show how you calculated the value of each of the components. Use Diptrace to generate the schematic.

Show that

1. The current consumption is less than 70mA
2. The small-signal bandwidth is at least 5KHz-5MHz while the mid-band gain is 20dB±0.5dB (by AC analysis)
3. The harmonic content of the output voltage is better than −30dBc with 0.1V peak input signal at 500KHz.

Determine

4. The small-signal input impedance of the amplifier at 500KHz (the adjusted value of R_S in AC analysis until the voltage gain drops by 6dB compared to R_S=0)
5. The small-signal output impedance of the amplifier at 500KHz (the adjusted value of R_L in AC analysis until the voltage gain drops by 6dB compared to R_L=∞)
6. The phase margin of the open-loop system.

Experimental work (Due May 8) (Upload pdf report)

Build your design on a breadboard. Use as short leads as possible. For this purpose, place the components while thinking about short connections.

Test your circuit one stage at a time without feedback. Make sure that the DC voltages of the transistors are correct, and you can measure each stage's voltage gain at 500KHz. Measure the voltage gain of the two-stage circuit and bandwidth without feedback. Then, insert the feedback resistor.

Show that

1. The current consumption is less than 70mA
2. The bandwidth is at least 5KHz-5MHz while the mid-band gain is 20dB±0.5dB (measure at 5KHz, 500KHz and 5MHz). Adjust the signal generator to 50mV peak (meaning it generates 200mV peak-to-peak) and insert a 470Ω resistor in series with the signal generator to simulate R_S=500Ω. The output voltage across R_L=47Ω should be 2V peak-to-peak.
3. The harmonic content of the output voltage is better than −30dBc at 500KHz.

Determine

4. The small-signal input impedance of the amplifier at 500KHz (with R_L=47Ω, adjusted value of R_S until the voltage gain drops to half its value compared to R_S=0)
5. The small-signal output impedance of the amplifier at 500KHz (with R_S=500 Ω, adjusted value of R_L until the voltage gain drops to half its value compared to R_L=∞ while applying the smallest signal of the signal generator. Use EXT SYNC for problem-free oscilloscope measurement.)