# *1. Description*

## 1.1. Project

| | |
|---|---|
| Project Name | AutoPilot |
| Board Name | AutoPilot |
| Generated with: | STM32CubeMX 4.16.1 |
| Date | 09/24/2016 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F4 |
| MCU Line | STM32F405/415 |
| MCU name | STM32F405RGTx |
| MCU Package | LQFP64 |
| MCU Pin number | 64 |

# 2. Pinout Configuration
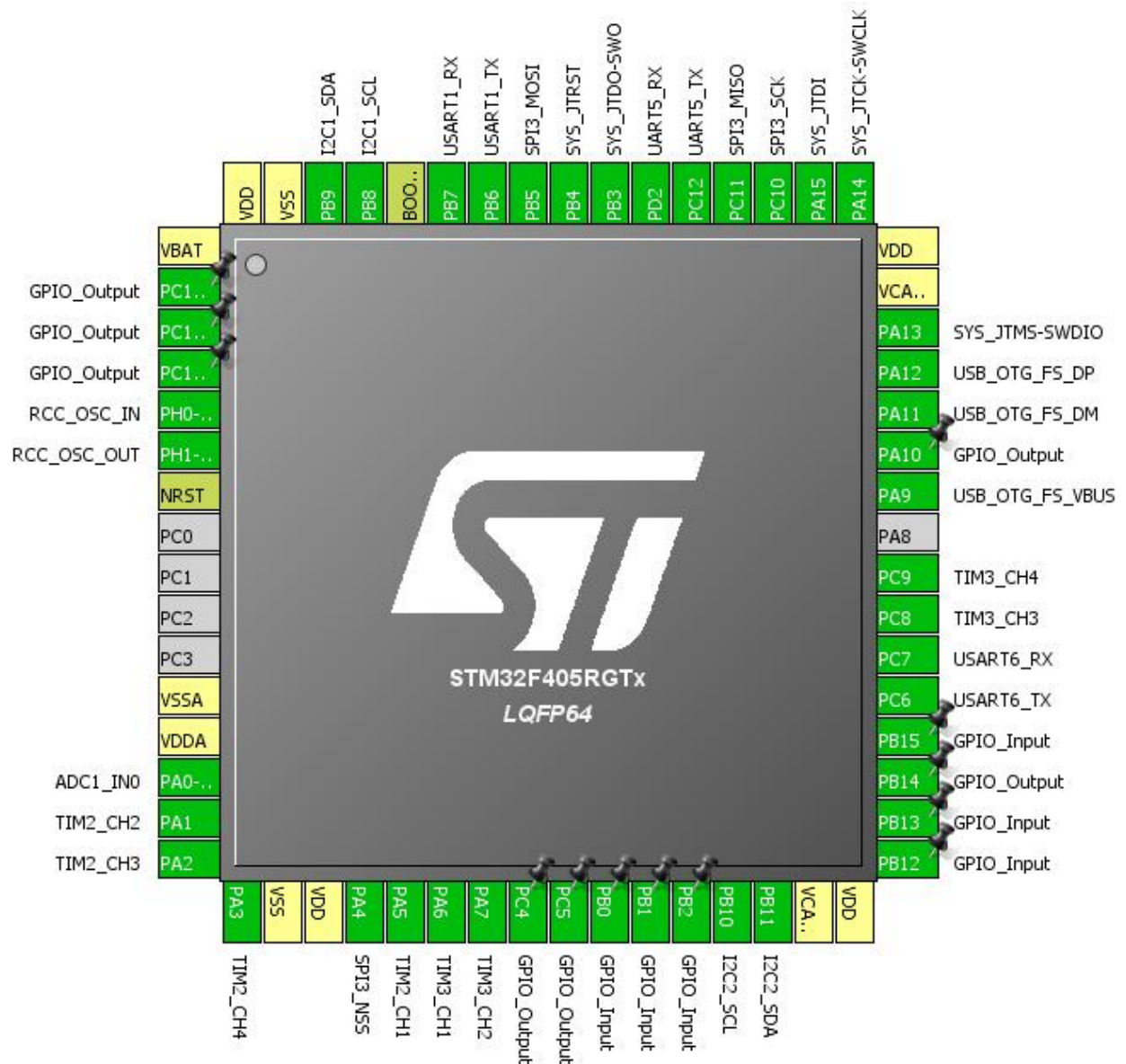
# 3. Pins Configuration

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | VBAT | Power | | |
| 2 | PC13-ANTI_TAMP * | I/O | GPIO_Output | |
| 3 | PC14-OSC32_IN * | I/O | GPIO_Output | |
| 4 | PC15-OSC32_OUT * | I/O | GPIO_Output | |
| 5 | PH0-OSC_IN | I/O | RCC_OSC_IN | |
| 6 | PH1-OSC_OUT | I/O | RCC_OSC_OUT | |
| 7 | NRST | Reset | | |
| 12 | VSSA | Power | | |
| 13 | VDDA | Power | | |
| 14 | PA0-WKUP | I/O | ADC1_IN0 | |
| 15 | PA1 | I/O | TIM2_CH2 | |
| 16 | PA2 | I/O | TIM2_CH3 | |
| 17 | PA3 | I/O | TIM2_CH4 | |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 20 | PA4 | I/O | SPI3_NSS | |
| 21 | PA5 | I/O | TIM2_CH1 | |
| 22 | PA6 | I/O | TIM3_CH1 | |
| 23 | PA7 | I/O | TIM3_CH2 | |
| 24 | PC4 * | I/O | GPIO_Output | |
| 25 | PC5 * | I/O | GPIO_Output | |
| 26 | PB0 * | I/O | GPIO_Input | |
| 27 | PB1 * | I/O | GPIO_Input | |
| 28 | PB2 * | I/O | GPIO_Input | |
| 29 | PB10 | I/O | I2C2_SCL | |
| 30 | PB11 | I/O | I2C2_SDA | |
| 31 | VCAP_1 | Power | | |
| 32 | VDD | Power | | |
| 33 | PB12 * | I/O | GPIO_Input | |
| 34 | PB13 * | I/O | GPIO_Input | |
| 35 | PB14 * | I/O | GPIO_Output | |
| 36 | PB15 * | I/O | GPIO_Input | |
| 37 | PC6 | I/O | USART6_TX | |
| 38 | PC7 | I/O | USART6_RX | |
| 39 | PC8 | I/O | TIM3_CH3 | |
| 40 | PC9 | I/O | TIM3_CH4 | |

| Pin Number LQFP64 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 42 | PA9 | I/O | USB_OTG_FS_VBUS | |
| 43 | PA10 * | I/O | GPIO_Output | |
| 44 | PA11 | I/O | USB_OTG_FS_DM | |
| 45 | PA12 | I/O | USB_OTG_FS_DP | |
| 46 | PA13 | I/O | SYS_JTMS-SWDIO | |
| 47 | VCAP_2 | Power | | |
| 48 | VDD | Power | | |
| 49 | PA14 | I/O | SYS_JTCK-SWCLK | |
| 50 | PA15 | I/O | SYS_JTDI | |
| 51 | PC10 | I/O | SPI3_SCK | |
| 52 | PC11 | I/O | SPI3_MISO | |
| 53 | PC12 | I/O | UART5_TX | |
| 54 | PD2 | I/O | UART5_RX | |
| 55 | PB3 | I/O | SYS_JTDO-SWO | |
| 56 | PB4 | I/O | SYS_JTRST | |
| 57 | PB5 | I/O | SPI3_MOSI | |
| 58 | PB6 | I/O | USART1_TX | |
| 59 | PB7 | I/O | USART1_RX | |
| 60 | BOOT0 | Boot | | |
| 61 | PB8 | I/O | I2C1_SCL | |
| 62 | PB9 | I/O | I2C1_SDA | |
| 63 | VSS | Power | | |
| 64 | VDD | Power | | |

* The pin is affected with an I/O function

# *4. Clock Tree Configuration*
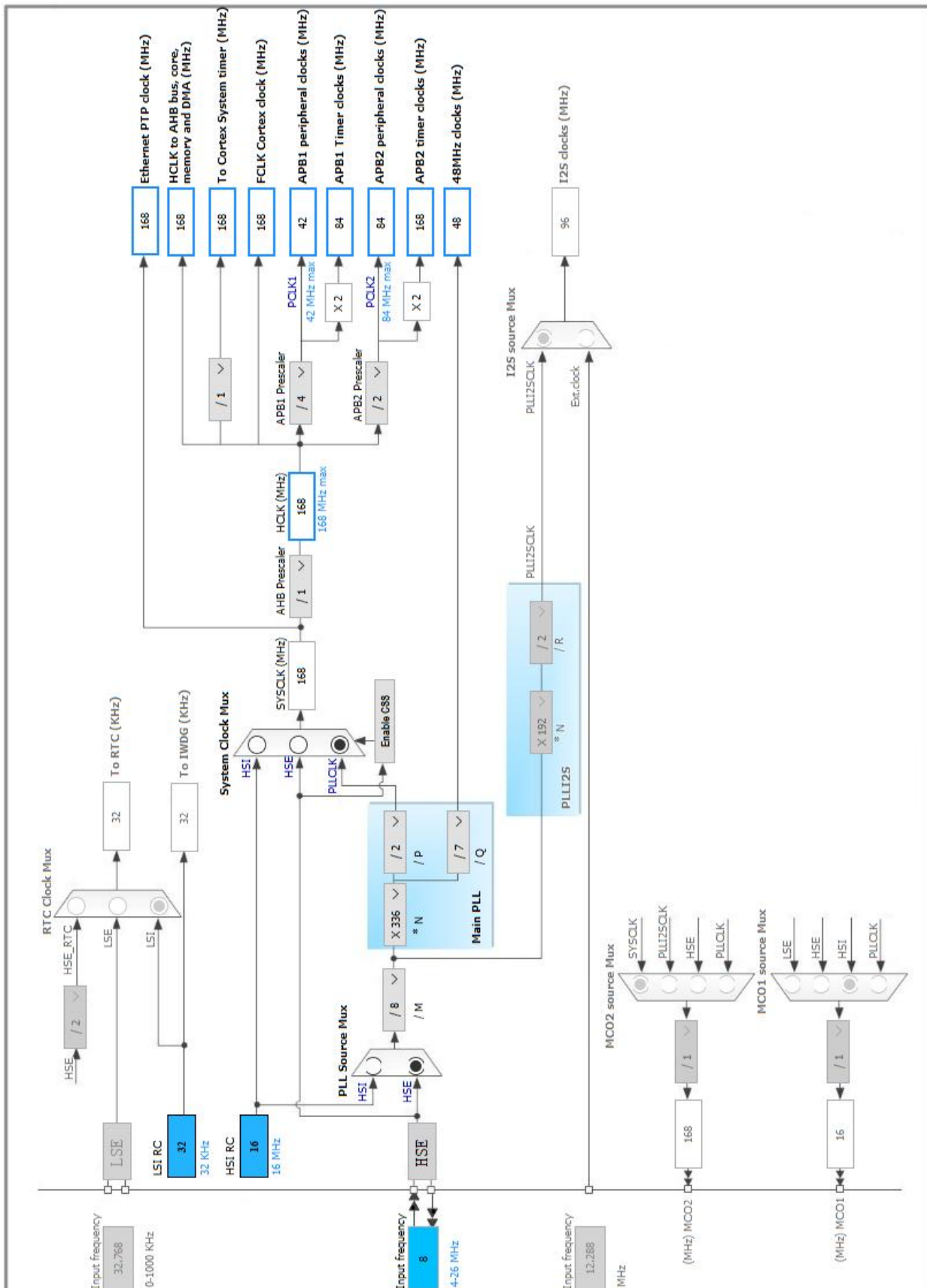
# 5. IPs and Middleware Configuration

## 5.1. ADC1
**mode: IN0**

### 5.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 0 |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 5.2. CRC
**mode: Activated**

## 5.3. I2C1
**I2C: I2C**

### 5.3.1. Parameter Settings:

**Master Features:**

| | |
|---|---|
| I2C Speed Mode | **Fast Mode *** |
| I2C Clock Speed (Hz) | 400000 |
| Fast Mode Duty Cycle | Duty cycle Tlow/Thigh = 2 |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |
| General Call address detection | Disabled |

## 5.4. I2C2

**I2C: I2C**

### 5.4.1. Parameter Settings:

**Master Features:**

| | |
|---|---|
| I2C Speed Mode | Standard Mode |
| I2C Clock Speed (Hz) | 100000 |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |
| General Call address detection | Disabled |

## 5.5. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

### 5.5.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |

| | |
|---|---|
| Prefetch Buffer | Enabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 5 WS (6 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Regulatror Voltage Scale | Power Regulator Voltage Scale 1 |

## 5.6. SPI3

**Mode: Full-Duplex Master**

**Hardware NSS Signal: Hardware NSS Output Signal**

### 5.6.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 8 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | **4 \*** |
| Baud Rate | **10.5 MBits/s \*** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSS Signal Type | Output Hardware |

## 5.7. SYS

**Debug: JTAG (5 pins)**

**Timebase Source: TIM1**

## 5.8. TIM2

**Channel1: PWM Generation CH1**
**Channel2: PWM Generation CH2**
**Channel3: PWM Generation CH3**
**Channel4: PWM Generation CH4**

### 5.8.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode | Disable (no sync between this TIM (Master) and its Slaves |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## *5.9. TIM3*

**Channel1: PWM Generation CH1**
**Channel2: PWM Generation CH2**
**Channel3: PWM Generation CH3**
**Channel4: PWM Generation CH4**

### 5.9.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode | Disable (no sync between this TIM (Master) and its Slaves |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## 5.10. UART5

**Mode: Asynchronous**

### 5.10.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | **100000 *** |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## *5.11. USART1*

**Mode: Asynchronous**

### 5.11.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | **57600 *** |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## *5.12. USART6*

**Mode: Asynchronous**

### 5.12.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |

| Stop Bits | 1 |
|---|---|

**Advanced Parameters:**

| Data Direction | Receive and Transmit |
|---|---|
| Over Sampling | 16 Samples |

## 5.13. USB_OTG_FS

**Mode: Device_Only**
**mode: Activate_VBUS**

### 5.13.1. Parameter Settings:

| Speed | Device Full Speed 12MBit/s |
|---|---|
| Endpoint 0 Max Packet size | 64 Bytes |
| Enable internal IP DMA | Disabled |
| Low power | Disabled |
| Link Power Management | Disabled |
| VBUS sensing | Enabled |
| Signal start of frame | Disabled |

## 5.14. FREERTOS

**mode: Enabled**

### 5.14.1. Config parameters:

**Versions:**

| CMSIS-RTOS version | 1.02 |
|---|---|
| FreeRTOS version | 8.2.3 |

**Kernel settings:**

| USE_PREEMPTION | Enabled |
|---|---|
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 7 |
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | 16 |
| USE_16_BIT_TICKS | Disabled |
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |

| | |
|---|---|
| USE_RECURSIVE_MUTEXES | Disabled |
| USE_COUNTING_SEMAPHORES | Disabled |
| QUEUE_REGISTRY_SIZE | 8 |
| USE_APPLICATION_TASK_TAG | Disabled |
| TOTAL_HEAP_SIZE | 15360 |
| Memory Management scheme | heap_4 |
| USE_ALTERNATIVE_API | Disabled |
| ENABLE_BACKWARD_COMPATIBILITY | Enabled |
| USE_PORT_OPTIMISED_TASK_SELECTION | Disabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |

**Hook function related definitions:**

| | |
|---|---|
| USE_IDLE_HOOK | Disabled |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Disabled |

**Run time and task stats gathering related definitions:**

| | |
|---|---|
| USE_TRACE_FACILITY | Enabled |
| GENERATE_RUN_TIME_STATS | Disabled |

**Co-routine related definitions:**

| | |
|---|---|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

**Software timer definitions:**

| | |
|---|---|
| USE_TIMERS | Disabled |
| TIMER_TASK_PRIORITY | 2 |
| TIMER_QUEUE_LENGTH | 10 |
| TIMER_TASK_STACK_DEPTH | 256 |

**Interrupt nesting behaviour configuration:**

| | |
|---|---|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 15 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 5 |

## 5.14.2. Include parameters:

**Include definitions:**

| | |
|---|---|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Enabled |
| vTaskCleanUpResources | Disabled |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | Disabled |
| vTaskDelay | Enabled |

| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Disabled |
| xSemaphoreGetMutexHolder | Disabled |
| pcTaskGetTaskName | Disabled |
| uxTaskGetStackHighWaterMark | Disabled |
| xTaskGetCurrentTaskHandle | Disabled |
| eTaskGetState | Disabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall | Disabled |

## 5.15. USB_DEVICE

### Class For FS IP: Communication Device Class (Virtual Port Com)

### 5.15.1. Parameter Settings:

**Basic Parameters:**

| USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces) | 1 |
| USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration) | 1 |
| USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors) | 512 |
| USBD_SUPPORT_USER_STRING (Enable user string descriptor) | Disabled |
| USBD_SELF_POWERED (Enabled self power) | Enabled |
| USBD_DEBUG_LEVEL (USBD Debug Level) | 0: No debug message |

**Class Parameters:**

| USBD_CDC_INTERVAL (Number of micro-frames interval) | 1000 |

### 5.15.2. Device Descriptor:

**Device Descriptor:**

| VID (Vendor IDentifier) | 1155 |
| LANGID_STRING (Language Identifier) | English(United States) |
| MANUFACTURER_STRING (Manufacturer Identifier) | STMicroelectronics |

**Device Descriptor FS:**

| PID (Product IDentifier) | 22336 |
| PRODUCT_STRING (Product Identifier) | STM32 Virtual ComPort |
| SERIALNUMBER_STRING (Serial number) | 00000000001A |
| CONFIGURATION_STRING (Configuration Identifier) | CDC Config |
| INTERFACE_STRING (Interface Identifier) | CDC Interface |

**\* User modified value**

# 6. System Configuration

## 6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PA0-WKUP | ADC1_IN0 | Analog mode | No pull-up and no pull-down | n/a | |
| I2C1 | PB8 | I2C1_SCL | Alternate Function Open Drain | Pull-up | **Very High \*** | |
| | PB9 | I2C1_SDA | Alternate Function Open Drain | Pull-up | **Very High \*** | |
| I2C2 | PB10 | I2C2_SCL | Alternate Function Open Drain | Pull-up | **Very High \*** | |
| | PB11 | I2C2_SDA | Alternate Function Open Drain | Pull-up | **Very High \*** | |
| RCC | PH0-OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1-OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SPI3 | PA4 | SPI3_NSS | Alternate Function Push Pull | No pull-up and no pull-down | **Very High \*** | |
| | PC10 | SPI3_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High \*** | |
| | PC11 | SPI3_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High \*** | |
| | PB5 | SPI3_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High \*** | |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| | PA15 | SYS_JTDI | n/a | n/a | n/a | |
| | PB3 | SYS_JTDO-SWO | n/a | n/a | n/a | |
| | PB4 | SYS_JTRST | n/a | n/a | n/a | |
| TIM2 | PA1 | TIM2_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA2 | TIM2_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA3 | TIM2_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA5 | TIM2_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| TIM3 | PA6 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA7 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC8 | TIM3_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC9 | TIM3_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| UART5 | PC12 | UART5_TX | Alternate Function Push Pull | Pull-up | **Very High \*** | |
| | PD2 | UART5_RX | Alternate Function Push Pull | Pull-up | **Very High \*** | |
| USART1 | PB6 | USART1_TX | Alternate Function Push Pull | Pull-up | **Very High \*** | |
| | PB7 | USART1_RX | Alternate Function Push Pull | Pull-up | **Very High \*** | |
| USART6 | PC6 | USART6_TX | Alternate Function Push Pull | Pull-up | **Very High \*** | |
| | PC7 | USART6_RX | Alternate Function Push Pull | Pull-up | **Very High \*** | |
| USB_OTG_FS | PA9 | USB_OTG_FS_VBUS | Input mode | No pull-up and no pull-down | n/a | |
| | PA11 | USB_OTG_FS_DM | Alternate Function Push Pull | No pull-up and no pull-down | **Very High \*** | |
| | PA12 | USB_OTG_FS_DP | Alternate Function Push Pull | No pull-up and no pull-down | **Very High \*** | |
| GPIO | PC13-ANTI_TAMP | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PC14-OSC32_IN | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PC15-OSC32_OUT | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PC4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PC5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PB0 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PB1 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PB2 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PB12 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PB13 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PB14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PB15 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PA10 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |

## 6.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| I2C1_RX | DMA1_Stream5 | Peripheral To Memory | Low |
| I2C1_TX | DMA1_Stream6 | Memory To Peripheral | Low |
| SPI3_RX | DMA1_Stream2 | Peripheral To Memory | **High \*** |
| SPI3_TX | DMA1_Stream7 | Memory To Peripheral | **High \*** |
| USART6_RX | DMA2_Stream1 | Peripheral To Memory | Low |
| USART6_TX | DMA2_Stream6 | Memory To Peripheral | Low |
| UART5_RX | DMA1_Stream0 | Peripheral To Memory | Low |
| USART1_RX | DMA2_Stream2 | Peripheral To Memory | Low |
| USART1_TX | DMA2_Stream7 | Memory To Peripheral | Low |

### I2C1_RX: DMA1_Stream5 DMA request Settings:

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable \*** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### I2C1_TX: DMA1_Stream6 DMA request Settings:

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable \*** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### SPI3_RX: DMA1_Stream2 DMA request Settings:

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable \*** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### SPI3_TX: DMA1_Stream7 DMA request Settings:

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### USART6_RX: DMA2_Stream1 DMA request Settings:

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### USART6_TX: DMA2_Stream6 DMA request Settings:

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### UART5_RX: DMA1_Stream0 DMA request Settings:

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### USART1_RX: DMA2_Stream2 DMA request Settings:

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| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

## *USART1_TX: DMA2_Stream7 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

## 6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 15 | 0 |
| System tick timer | true | 15 | 0 |
| DMA1 stream0 global interrupt | true | 5 | 0 |
| DMA1 stream2 global interrupt | true | 5 | 0 |
| DMA1 stream5 global interrupt | true | 0 | 0 |
| DMA1 stream6 global interrupt | true | 5 | 0 |
| TIM1 update interrupt and TIM10 global interrupt | true | 0 | 0 |
| DMA1 stream7 global interrupt | true | 5 | 0 |
| SPI3 global interrupt | true | 5 | 0 |
| DMA2 stream1 global interrupt | true | 5 | 0 |
| DMA2 stream2 global interrupt | true | 5 | 0 |
| USB On The Go FS global interrupt | true | 5 | 0 |
| DMA2 stream6 global interrupt | true | 5 | 0 |
| DMA2 stream7 global interrupt | true | 5 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1, ADC2 and ADC3 global interrupts | unused | | |
| TIM2 global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| I2C1 event interrupt | unused | | |
| I2C1 error interrupt | unused | | |
| I2C2 event interrupt | unused | | |
| I2C2 error interrupt | unused | | |
| USART1 global interrupt | unused | | |
| UART5 global interrupt | unused | | |
| USART6 global interrupt | unused | | |
| FPU global interrupt | unused | | |

**\* User modified value**

# *7. Power Consumption Calculator report*

## 7.1. Microcontroller Selection

| Series | STM32F4 |
|---|---|
| Line | STM32F405/415 |
| MCU | STM32F405RGTx |
| Datasheet | 022152_Rev7 |

## 7.2. Parameter Selection

| Temperature | 25 |
|---|---|
| Vdd | 3.3 |

# 8. Software Project

## 8.1. Project Settings

| Name | Value |
| --- | --- |
| Project Name | AutoPilot |
| Project Folder | E:\yExin\dasLaboratorium\STM32\STMGenerated\AutoPilot |
| Toolchain / IDE | MDK-ARM V5 |
| Firmware Package Name and Version | STM32Cube FW_F4 V1.13.0 |

## 8.2. Code Generation Settings

| Name | Value |
| --- | --- |
| STM32Cube Firmware Library Package | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |