California State University, Northridge

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Lab 10

Interrupts

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ECE 425L

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Introduction:

In lab 10 we are introduced to interrupts. Interrupts are a very important tool for handling large applications and multitasking. Here we use specifically the SoftWare Interrupt (SWI), Interrupt ReQuest (IRQ), and Fast Interrupt ReQuest (FIQ).

Procedure:

Equipment Used

- Keil uVision4
- Keil Debugger
- LPC2148 Education Board

Description of Procedure

1. We first set up the startup code for this lab. We initially start using the same startup code from lab 3. We are asked to modify the startup code so that the stack initialization is performed in the reset handler for all processor modes. This is done by first setting the number of bytes attached or used, to the stack at each mode as shown below.

2. Then defining the mode bits from the manual as shown below.

```
16
   Mode USR
                   EOU
                           0x10 : Mode bits for USR mode
17
                           0x13 ; Mode bits for Supervisor mode
   Mode SVC
                   EQU
18 Mode UND
                   EQU
                           0x1B ; Mode bits for Undefined mode
19 Mode IRQ
                 EQU
                          0x12 ; Mode bits for IRO mode
20 Mode FIQ
                   EQU
                          0x11 ; Mode bits for FIQ mode
                          0x17 ; Mode bits for ABT mode
21 Mode ABT
                   EQU
```

3. Then adding these last three lines for the stack in the definitions. This will be more clear in the next step.

```
;Defintions of User Mode Stack and Size

24 SRAM_BASE EQU 0x40000000; Starting address of the SRAM

25 I_Bit EQU 0x80; when I bit is set, IRQ is disabled

26 F_Bit EQU 0x40; when F bit is set, FIQ is disabled

27 USR_Stack_Size EQU 0x00000100

28 SRAM EQU 0X40000000

29 Stack_Top EQU SRAM+USR_Stack_Size
```

4. Then for the final part of task 1 we load the descending stack for each mode. This is done by loading r0 with the SRAM+BASE and adding the corresponding mode stack. Then we move the value from the selected special-purpose register, which is the mode+ I_Bit + F_Bit into CPSR_c. Finally move r0 to sp and load user code to PC.

This process is repeated for all modes as shown below.

```
Reset Handler
101
                     ;;Supervisor mode
102
                     LDR
                            r0, =SRAM BASE+ Len SVC Stack; Descending stack
103
         ; Enter each mode in turn and set up the stack pointer
104
                    MSR
                            CPSR c, #Mode SVC+I Bit+F Bit
105
                             sp, r0
106
                            PC, =user code
                     LDR
107
                     ;;FIQ mode?
108
109
                           r0, =SRAM BASE+ Len FIQ Stack
                    LDR
110
         ; Enter each mode in turn and set up the stack pointer
111
                    MSR
                           CPSR c, #Mode FIQ+I Bit+F Bit
112
                    MOV
                            sp, r0
113
                     LDR
                            PC, =user code
114
115
                     ;; IRQ mode
116
                            r0, =SRAM BASE+ Len IRQ Stack
                    LDR
117
         ; Enter each mode in turn and set up the stack pointer
118
                    MSR
                           CPSR c, #Mode IRQ+I Bit+F Bit
119
                    MOV
                            sp, r0
120
                     LDR
                            PC, =user code
121
122
                     ;;Undefined mode
                            r0, =SRAM BASE+ Len UND Stack
123
                     LDR
124
         ; Enter each mode in turn and set up the stack pointer
125
                    MSR
                          CPSR c, #Mode UND+I Bit+F Bit
126
                     MOV
                             sp, r0
127
                     LDR
                           PC, =user code
128
                     ;;Abort mode
129
130
                     LDR
                           r0, =SRAM BASE+ Len ABT Stack
131
         ; Enter each mode in turn and set up the stack pointer
132
                           CPSR_c, #Mode_ABT+I_Bit+F_Bit
                    MSR
133
                    MOV
                            sp, r0
                            PC, =user code
134
                     LDR
```

5. For Task 2 we are write a complete ARM assembly program which calls a single Software Interrupt to light up all 8 LEDs connected to P0.15 - P0.8, in the service routine.

This is done by first setting up GPIO as shown below.

```
26 PINSELO EQU 0xE002C000 ;pin function for port 0, equate symbolic name PINSELO as address 0xE002C000

27
28 ;;Selecting function as GPIO by writing all zeros to given address
29 MOV r0, #0 ;moves #0 into register r0
30 LDR r1,=PINSELO ;puts what is stored in register 0xE002C000 (PINSELO) in r1 register; CANNOT PUT MOV, outputs error in kei
31 STR r0,[r1] ;copies value stored in r0 to memory address specified by r1
```

6. Then set IO Direction and the initial clear and set of the LEDs we simply created a loop for these tasks as you will see in the next steps, some tasks require doing these steps again. So for a more clear and shorter code we implemented a loop.

```
;Initially Assigning B constant to zero

MOV B_var, $0

11

22  ;set IODIRECTION

43  BL setIODIR  ;;Selecting signal direction of each port pin, we put '1' in each to bit to make it an output pi

44

45  BL clrset  ;initial clr and set
```

7. Now after implementing a small delay for clarity when testing, we add the first exception which is SWI#1 that is meant to turn on all the lights.

8. The step above causes the PC to jump to the exception which is the SWI Handler. Shown below is the SWI Handler where we first decrement the link register by 4 so it will step back to the next line in the main program. R9 is loaded with the SWI value where we simply use a CMP function to BEQ to the desired action loop.

```
63
    SWIHandler
64
                           r9, [LR, #-4]
                  LDRB
65
                           r9, #0
                  CMP
66
                  BEQ
                           turnoff
67
                  CMP
                           r9, #1
68
                           lighton
                  BEQ
69
                  CMP
                           r9, #2
```

9. For this particular task it will branch to the loop shown below.

```
80 lighton ; turning on ALL LEDS

81 MOV r0, #0x0000FF00

82 LDR r1, =IO0BASE

83 STR r0, [r1, #IO0CLR]

84 MOVS PC, LR
```

10. Then for task 3 we are to make three different software interrupts which does 3 different functions with the lights. This is done in the same way as task 2 except we set a different number for each interrupt. Shown below are those respective interrupts and their functions in the main file.

```
49
    task3
50
                 T.DR
                         r5,=delayone
51
                 ;BL
                         RTN
                                          ;delay subroutine here
52
53
                 SWI #0
                                          ;to turn off all lights
                 SWI #2
54
                                           ;to turn on first four lights
55
56
                 LDR
                         r5,=delayone
57
                 ;BL
                         RTN
                                          ;delay subroutine here
58
59
                 SWI #3
                                          ;to turn on last four lights
60
61
                 LDR
                         r5,=delayone
                 ;BL
62
                         RTN
                                          :delay subroutine here
63
64
                 SWI #0
                                           ;turns it all off
65
                         endref
```

11. Shown below is the respective branch in the SWI Handler that achieves the tasks explained in the main.

```
73
    turnoff
                                       ;turning off ALL LEDs, (forcing a high) (binary 11111111100000000)
               MOV
                       r0, #0x0000FF00 ;LDR for this?
75
76
               LDR
                       rl,=IOOBASE
77
                       r0,[r1,#I00SET]
               STR
78
               MOVS
                      PC.LR
79
80 lighton
                                       turning on ALL LEDS
                      r0,#0x0000FF00
               MOV
81
                       r1,=IOOBASE
82
               T.DR
83
               STR
                       r0, [r1, #IOOCLR]
84
               MOVS
                      PC, LR
85
86 firstfour
87
               ;LDR R0,[LR,#-3]
                    r0,#0x0000F000 ;turns on first 4 (0000)111100000000
               MOV
88
                       rl,=IOOBASE
89
               LDR
                      r0,[r1,#IOOCLR]
90
               STR
                     PC, LR
               MOVS
91
93 lastfour
               ;LDR R0,[LR,#-3]
                    r0,#0x00000F00 ;turns on last 4 1111(0000)00000000
95
               MOV
               LDR
                       rl,=IOOBASE
96
97
               STR
                       r0,[r1,#IOOCLR]
               MOVS PC, LR
```

12. For the first task we are to set the lights to turn on one by one using loops and a 1 second delay. We calculated the delay for one second in ARM is about 4 million loops (as shown in step 1 screenshot, the 'delayone' hex number). We first load the delay to a register then we branch link to another file that we named RTN. This loop follows the same logic as the previous lab where we subtract 1 from the imported number in r5. Then once that is done, PC is loaded with the next line or link register of the previous file so it continues with the next step after the loop.

That step is a loop where we do a logical left shift of bit 8 in a loop 8 times for all 8 LEDs. This is shown in the code below.

```
47 taskl
48
              CMP
                      B var,#8
                                    ;B var = 8 BEQ next loop for task 2
49
              BEQ
                     task2
50
51 turnLow
              LDR r5,=delayone ;delaying onesec
BL RTN ;branching to external file delay_arm.s
;for logical shift
52
53
54
             LDR r0,=0x00000100 ;binary 100000000 (bit 8)
55
              LSL r0,B_var ;Logical shift left of B_var
56
57
58
             LDR rl,=IOOBASE ; forcing low
              STR r0, [r1, #IO0CLR]
59
60
61
              ADD B var, B var, #1 ;+1 B var
62
63
              В
                     taskl
1
           GLOBAL RTN
 2
            AREA mycode, CODE, READONLY
            ENTRY
 3
 4
            ;STMFD sp!, {LR}
 5
 6
 7
 8 RTN
               SUBS r5,#1
                       RTN
9
                BNE
                                   jump to given address if not zero;
                MOVEQ pc, lr
10
                ;LDMFD sp!, {PC} ;works without LDMFD and STMFD
11
12
13
            B RTN
14
            END
```

Results:

Task 1

```
LDR r0,=SRAM+FIQ_Stack
MSR CPSR_c,#Mode_FIQ+I_Bit+F_Bit
MOV sp,r0

LDR r0,=SRAM+IRQ_Stack
MSR CPSR_c,#Mode_IRQ+I_Bit+F_Bit
MOV sp,r0

LDR r0,=SRAM+Len_SWI_Stack
MSR CPSR_c,#Mode_SWI+I_Bit+F_Bit
MOV sp,r0
```

In task 1 all stack initializations were performed in the reset handler for the processor modes needed in this experiment

Task 2

General Purpose Input/Ou	tput 0 (GPI	O 0) - Slo	ow Interfa	ice					×
GPI00 IO0DIR: 0x0000FF00	31 Bi	ts 24	23	Bits 1	5 15 VVV	Bits	8 7	Bits	0
IO0SET: 0x00000000									
IO0CLR: 0x00000000									
IO0PIN: 0x82FF00FF									V V
Pins: 0xF2FF00FF		~							~~

In task 2 LEDs on P0.8-P0.15 were turned on by a single software interrupt call

Task 3

GPIO0-	urpose Input/Ou					(9874)		*****		15000	250		
	0x0000FF00	31	Bits	24	23	Bits	16	15	Bits	8	7	Bits	0
IOOSET:	0×0000F000						_	VVV		ГГ			П
IOOCLR:	0x00000000	ГГГ					Т	ГГГ					ГГ
IOOPIN:	0x82FFF0FF	PIT		V		IVIVIVI	VV	기기기	TIN	ГГ		VVV	VV
Pins:	0xF2FFF0FF	マママ	⊽	⊽			ママ		VI	ГГ			VV
GPIO0-	0.0005500	31	Bits	24	23	Bits	16	15	Bits	8	7	Bits	0
		31	Bits	24	23	Bits	16	15	Bits	8	7	Bits	0
	0x0000FF00									<u> </u>			
IO0SET:	0x00000F00									<u> </u>			П
IO0CLR:	0x00000000		ТГГ										ГГ
IO0PIN:	0x82FF0FFF	VII	ГГГ				717	ГГГ					
Pins:	0xF2FF0FFF	777	v	⊽			フレ	ГГГ		VV			VV
		, , , , , ,					-			, . ,	, . , . , .	, , , , ,	
eneral P	urpose Input/Ou	itput 0 (GPIO 0) - Slo	w Inter	face							
GPIO0-		24	Die	24	22	D::	10	45	D:	_	-	Dis	_
IOODIR:	0x0000FF00	31	Bits	24	23	Bits	_16		Bits	8		Bits	0
	0x0000FF00	ГГГ								VV	ГГГ		
	0x00000000	ГГГ					_	ГГГ		ГГ	ГГГ		
IO0CLR:		, , ,		, ,									
	0x82FFFFFF						77	V V V		VV	V V V	7000	VV

In task 3 we use 3 software interrupt calls. The first turns on LEDs P0.8-P0.11, the second turns on P0.12-P0.15, and the third turns off all LEDs that were turned on by the previous two software interrupts.

Conclusion:

In conclusion, we were able to successfully handle the different types of interrupts in assembly. In task 1 we initialized the stack for all different processor modes in the reset handler and this allowed us to later have the ability to handle both software and external interrupts. Task 2 and 3 were very similar and they both ran successfully in simulation and on the physical board as well. Task 4 was extra credit and we managed to successfully complete the set up for both the IRQ and FIQ interrupts but we were not able to exit the interrupts after we had serviced the interrupts. One way this lab could have gone better is for us to have exited the external interrupts in task 4 properly so that the board wouldn't get stuck in an infinite loop. This lab introduced us to both software and external interrupts and furthered our understanding of using pins as both inputs and outputs.