Comparative Analysis of SRAM and DRAM

Cristian Robles, Peter Guzman

***Abstract*—This paper conducts a comparative analysis of SRAM and DRAM from a designer's perspective, specifically focusing on their construction and performance at the CMOS transistor level. Despite use of similar components like sense amplifiers, row and column decoders, and equalization and pre-charge circuits, these two types of RAM show distinct behaviors and efficiencies. By analyzing how different RAM cells operate within similar environmental contexts, we seek to clarify the differences in their design and functionality. This investigation aims to provide insights into the selection and optimization of different RAM technologies for various applications.**

I. Introduction

THERE is a constant need for increasing speeds in future digital devices such as smartphones, personal computers and future technologies. One of the most crucial components in technology are complementary metal oxide semiconductors (CMOS), specifically the use of CMOS in random-access memory (RAM). With CMOS devices continuously down-sizing to attain increased speed, enhanced performance, and reduced power consumption, designing RAM with CMOS technology can result in memory configurations that are capable of delivering high-speed read and write operations [2]. A comparative analysis will be made on the two types of CMOS memory known as static random-access memory (SRAM) and dynamic random-access memory (DRAM). Other components in a memory chip such as the sense amplifier, row and column decoders will also be analyzed.

II. SRAM Theory

SRAM, or static random access memory, stores and provides access to digital information in electronic devices so long as power is not removed. This memory does not require constant refreshing compared to Dynamic random access memory, or DRAM. Therefore, SRAM is preferable as it can provide rapid operations to frequently accessed data [1]. A common design for an SRAM cell consists of six complementary metal oxide semiconductors, where two inverters are cross-coupled from each other to form a positive latch and are jointly connected with two access transistors as shown in Fig. 1. The access transistors Q5 and Q6 are on when the word-lines are high, allowing power through the mirrored inverters and a connection to the bit-lines to read or write a bit value in the bit-cell [2]

A. Read Operation

Consider the Q output is high at V_{DD} and $\overline{Q}$ output is low at 0 V in Fig. 1. The cell is currently storing a 1. In order to read the stored 1, the bit line and bit-bar line must be pre-charged to V_{DD}. The word line (WL) of the cell is selected and raised to

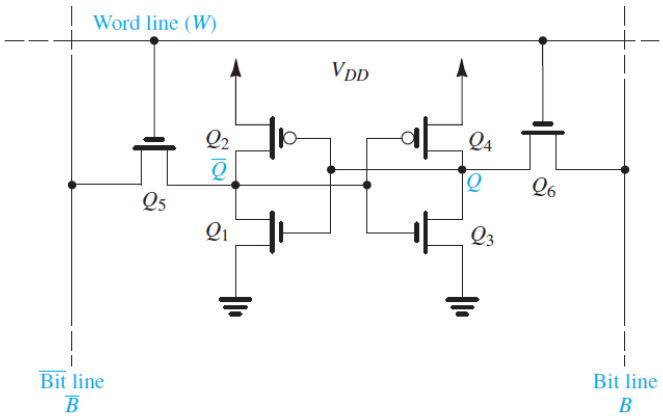

Fig. 1: Model of 6 transistor CMOS static RAM cell

V_{DD} as well, which is what turns on the n-type metal-oxide-semiconductor (NMOS) transistors Q_5 and Q_6 to access the cell. Since the output voltage at $\overline{Q}$ ($V_{\overline{Q}}$) is low, current I5 will discharge from the bit-bar line capacitance as shown in Fig. 2. It will continue discharging through Q_5 and charge the equivalent capacitance of $\overline{Q}$, rising $V_{\overline{Q}}$ until Q_1 conducts. Equilibrium is reached when $V_{\overline{Q}}$ no longer rises, making the current I_1 equal to I_5. In order to avoid a destructive read, $V_{\overline{Q}}$ must not exceed the voltage threshold of the other inverter, Q_3 and Q_4. With proper sizing of the access transistor, $V_{\overline{Q}}$ would be less than that voltage threshold, providing a nondestructive read operation [2].

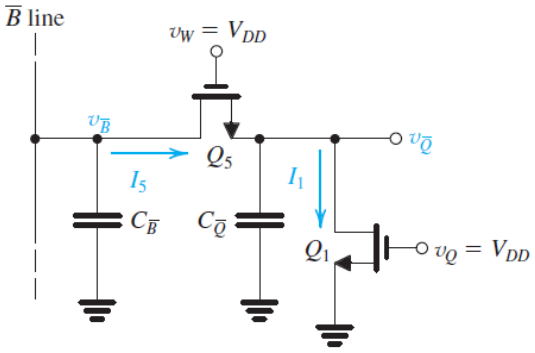

Fig. 2: Transistors in use during a read '1' operation for SRAM

For a read 0 operation, V_Q is storing a 0 and $V_{\overline{Q}}$ is high. The bit-lines are pre-charged to V_{DD} and the word line to the cell is activated to turn on the access transistors. The capacitance of the bit-line will begin discharging and current will be flowing

through Q_6 and into Q_3. Similarly to read 1, the equilibrium is reached when I_6 is equal to I_3 and $V_{\overline{Q}} \leq V_{tn}$.

B. Write Operation

In order to write a 1, it is assumed first that the cell is storing a 0. The word lines raise up to V_{DD} which turn on Q_5 and Q_6 and give access to the cell. Bit line capacitance is pre-charged to V_{DD}, and the bit-bar line is 0 V. Since the bit-bar line is 0 V, $V_{\overline{Q}}$ stays low and turns on the p-type metal-oxide-semiconductor (PMOS) of the inverter Q_3. The current I_3 flows to $V_{\overline{Q}}$ and charges the capacitance of the bit-bar line ensuring it is below the voltage threshold when equilibrium is reached (I_3 = I_6). With the bit-bar line is below V_t, bit line voltage still stays at V_{DD} so Q has a successful write-1 operation. Inversely, if trying to write a 0 when there is currently a stored 1, V_B is 0 V and $V_{\overline{Q}}$ is pre-charged to V_{DD}. As shown in Fig. 3 , the current from transistor Q_4 flows to the bit line capacitance and charges the line until it reaches equilibrium (I_4 = I_6) with the current at Q_6, such that V_B is less than the voltage threshold [2].

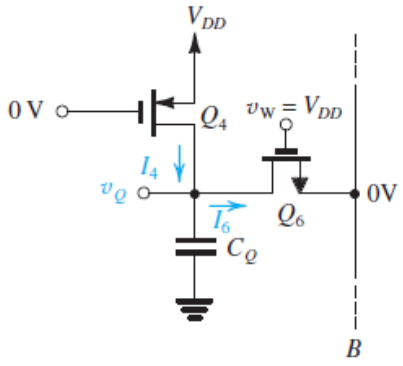

Fig. 3: SRAM write '0' operation for Q_4 and Q_6

Proper sizing of the transistors for reading and writing operations will be discussed in the design section of this report.

III. DRAM Theory

As illustrated in Fig. 4, a DRAM cell is composed of a single NMOS transistor and a capacitor (C_S), which are connected to the bit and word lines. When the word line is activated to a high state, the NMOS transistor becomes conductive and creates a connection between the capacitor C_S and the bit line. This connection is necessary for read and write operations in the DRAM cell. A charge equivalent to V_{DD} stored on the capacitor C_S indicates the cell holding a binary '1', while having no charge on the capacitor indicates that the cell is storing a binary '0'.

A. Read Operation

In a DRAM cell, the bit line has a parasitic capacitance C_B Fig. 5. This capacitance of the bit line is estimated to be about ten times the capacitance of the cell's storage. During the reading process, the bit line is pre-charged to $V_{DD}/2$ through the equalization and pre-charge circuitry. When the word line is driven high, it activates the NMOS transistor which links the bit line's parasitic capacitance with the cell's capacitor C_S. If C_S is storing a binary '1', meaning it holds a charge equivalent to V_{DD}, this results in an increase in the bit line's capacitance. When the sense amplifier is activated, it detects this change and amplifies the bit line voltage up to V_{DD}. On the other hand, if C_S is holding a binary '0' the bit line capacitance decreases. The sense amplifier responds to this change by pulling the voltage on the bit line down to zero. This allows the DRAM cell to be accurately read for both cases.

B. Write Operation

In the write operation of a DRAM cell, the word line is driven high, enabling a connection to the capacitor C_S. For writing a zero, the bit line is grounded, causing the capacitor to discharge. When the word line is lowered, this discharged state, representing a zero, is preserved in C_S. Conversely, to write a one, the bit line is connected to V_{DD}, allowing the capacitor to charge up to V_{DD}. Once the word line is driven low, this charge, representing a one, is retained within C_S.

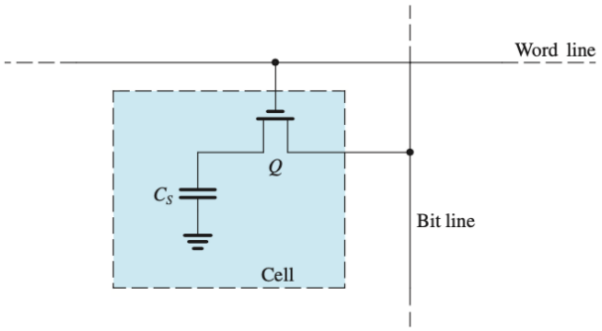

Fig. 4: Single transistor DRAM cell

Fig. 5: Cell capacitor and bit line parasitic capacitor

IV. Design / Analysis Methodology

For comparing SRAM to DRAM, there was a consideration to use the same parameters for the CMOS transistors. The NMOS model used is a 0.18 um TSMC CMOS technology named "nmos018." It is a T14B, BSIM3, and level 7 model with a V_{tn} = 0.366 V. PMOS model is named "pmos018" with

similarly 0.18 um CMOS technology , T14B, BSIM3, level 7 and a $|V_{tp}|$ = 0.37 V. Based on the design of the cell, the widths of the transistors needed to be sized accordingly when V_{DD} = 1.8 V, V_{tn} = $|V_{tp}|$ = 0.366 V, and transistors are matched. The selected NMOS and PMOS models were essential in constructing the RAM cells and other key components, including the sense amplifier, row and column decoders, and pre-charge and equalization circuits. This approach enabled the creation of a circuit with diverse memory cells, providing a basis for analyzing the differences between SRAM and DRAM.

A. Inverter Design

To create the first building block of an SRAM, the inverter shown in Fig. 6 is built with one PMOS and one NMOS connected in series between the power supply and ground. To find the widths of both transistors, the decision to make the ratio $(\frac{W}{L})_n$ = 1 was made as this is a common practice for sizing NMOS. This would make the width and length of the NMOS both 0.18 um. For PMOS, the transistor width must be bigger than NMOS to balance out any differences in carrier mobility and current carrying capabilities.

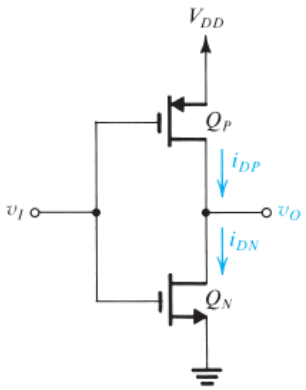

Fig. 6: A CMOS inverter

For the matched case, the transconductance of the NMOS is equal to the transconductance of the PMOS, or k_n = k_p. Solving the transconductance requires the use of eq (1) and eq (2) for calculating the parameters in terms of the NMOS and PMOS.

$$k_n = \mu_n * C_{ox} * (\frac{W}{L})_n \tag{1}$$

$$k_p = \mu_p * C_{ox} * (\frac{W}{L})_p \tag{2}$$

μ_n and μ_p is given in the SPICE parameters as 265.1889 $(\frac{cm^2}{Vsec})$ and 103.0478 $(\frac{cm^2}{Vsec})$ respectively. To find the oxide capacitance C_{ox}, eq (3) is applied where the oxide permittivity E_{ox} is divided by the oxide thickness t_{ox}.

$$C_{ox} = \frac{E_{ox}}{t_{ox}} \tag{3}$$

The thickness is given for both metal-oxide-semiconductor field effect transistors (MOSFETs) as 4 nm. The permittivity of the oxide is found by multiplying the permittivity of free space (approximately 8.854 $(\frac{pF}{m})$ with the dielectric constant of the oxide material being silicon dioxide (approximately equal to 3.9). With E_{ox} = 34.53 pF, the calculated oxide capacitance C_{ox} = 8.632 $(\frac{mF}{A})$. When k_n = k_p, the solved value for the width of the PMOS is 0.464 um. The voltage transfer characteristic (VTC) curve is simulated on PSPICE as shown in Fig. 7.

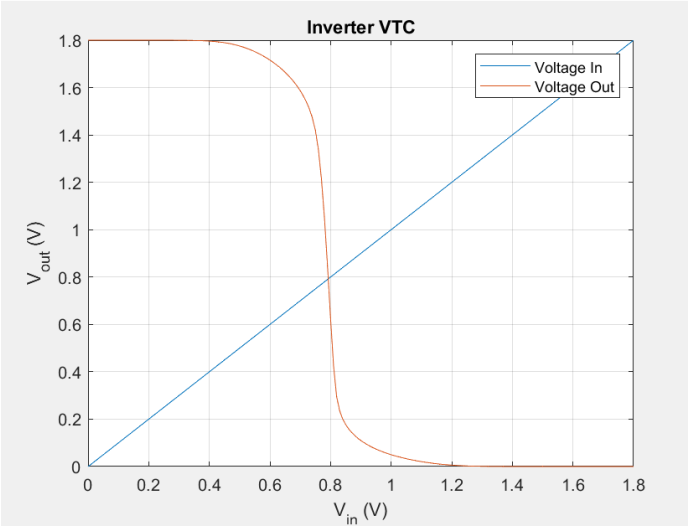

Fig. 7: VTC of PSPICE inverter

As the input voltage progresses from a low state to a high state, the output voltage undergoes a transition from high to low. The shift between high and low states happens at a threshold voltage (V_{th}) marking the point at which NMOS and PMOS transistors change their conduction states. From the PSPICE simulation, the VTC curve is symmetric, demonstrating a steep slope near the threshold for a swift and well-defined transition.

B. Sense Amplifier Design

As previously noted, the inverter is a critical element in SRAM design. Similarly, the sense amplifier depicted in Fig 8 also employs the inverter in a nearly identical manner. The main difference of the sense amplifier from the SRAM cell lies in the presence of a pulse at the top which dictates its activation and deactivation. The sense amplifier functions crucially in both cell types, acting to elevate the bit line to V_{DD} when there's an increase in the bit line voltage, and to ground the bit line when the bit line voltage decreases. The functionality of the sense amplifier is significantly dependent on the equalization and pre-charge circuitry. This is due to the necessity of having both the bit line and bit bar line pre-charged to $V_{DD}/2$. To ensure the same charge across both lines before the activation of the sense amplifier it is necessary to have a switch. This switch facilitates the connection between the bit line and bit bar line, ensuring they are at the same potential, thereby setting the stage for effective sensing.

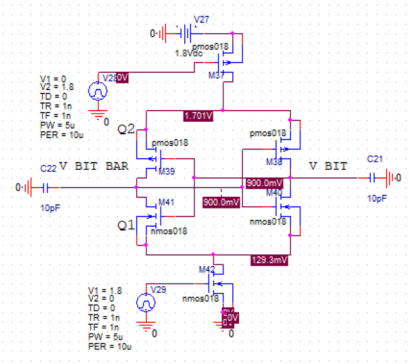

Fig. 8: PSPICE sense amplifier circuit

C. Row/Column Decoder Design

In a full-block RAM, a necessary mechanism is the cell selectors for read or write operations. This is achieved through decoders. Decoders function by receiving address bits and based on these inputs select a single line from their many outputs. The relationship between the number of address bits and the number of outputs follows a 2 to the power of n rule. For example, a 3-bit address can select from 8 lines, while a 2-bit address can choose from 4 lines. In our PSPICE design, we incorporated a 1-bit address for both row and column decoders, as shown in Fig. 9 and Fig. 10, enabling the selection of 2 lines. This setup was designed to accommodate a 4-bit SRAM and DRAM.

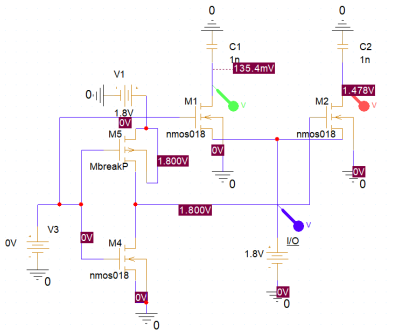

Fig. 9: Two line PSPICE tree column decoder

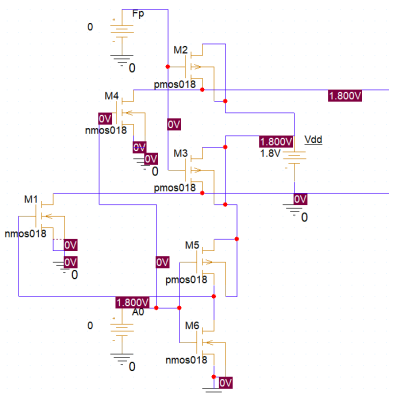

Fig. 10: Two line PSPICE NOR row decoder

D. SRAM Design

With transistors properly sized and a working CMOS inverter, the SRAM cell can be designed. As previously mentioned, two inverters are cross-coupled and form a positive latch. The access transistors Q_5 and Q_6 would need to be sized accordingly such that the SRAM cell would be able to have successful read and write operations while also not be susceptible to destructive reads. Eq. 4 is used to solve for the ratio $(\frac{W}{L})_a$ / $(\frac{W}{L})_n$, which would be the maximum value permitted on the access transistor to ensure V_q and $V_{\overline{Q}}$ does not rise above the voltage threshold.

$$\frac{(\frac{W}{L})_a}{(\frac{W}{L})_n} = \frac{1}{(1 - \frac{V_t}{V_{DD} - V_t})^2} - 1 \tag{4}$$

When $(\frac{W}{L})_n$ = 1, V_{DD} = 1.8 V, and V_{tn} = 0.37 V, the ratio for the access transistor $(\frac{W}{L})_a$ is calculated to be less than or equal to 0.8028. This makes the width of the access transistors Q_5 and Q_6 = 0.144 um. Specifically for write operations, eq. 5 solves the ratio $(\frac{W}{L})_p$ / $(\frac{W}{L})_a$ in order to find the maximum width required for the two PMOS in the SRAM cell and successfully do a write operation.

$$\frac{(\frac{W}{L})_p}{(\frac{W}{L})_a} = (\frac{\mu_n}{\mu_p})[1 - (1 - \frac{V_t}{V_{DD} - V_t})^2] \tag{5}$$

$(\frac{W}{L})_p$ is less than or equal to 0.9229, so the width of the PMOS transistors should be 0.166 um. Table I shows the width over length ratios of transistors used for the 6T SRAM cell.

TABLE I: $(\frac{W}{L})$ ratios for the SRAM cell

Transistor (Q)	Width(μm)	Length (μm)
Q_1	0.180	0.180
Q_2	0.180	0.180
Q_3	0.464	0.180
Q_4	0.464	0.180
Q_5	0.464	0.180
Q_6	0.464	0.180

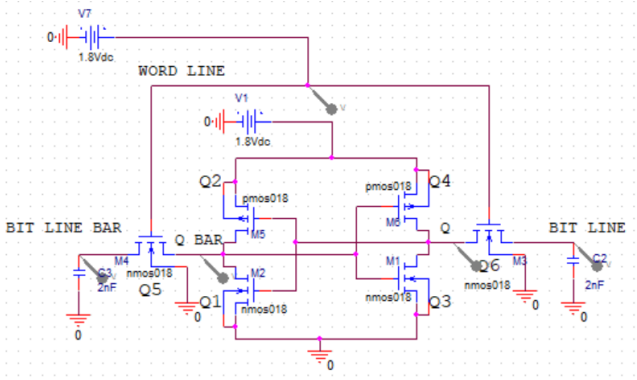

Fig. 11: PSPICE circuit of an SRAM cell

With this information gathered , The PSPICE circuit in Fig. 11 is created. Note the capacitance on the sides of the access transistors is like the capacitance on the bit line and bit line bar.

E. DRAM Design

In our PSPICE simulation, we first developed equalization and pre-charge circuitry before integrating a DRAM cell, seen in Fig 12. Given that the bit line capacitance is approximately ten times that of the cell's internal capacitor [2], we designed a cell with a 1nF capacitor and set the bit line capacitance to 9nF. As illustrated in Fig. 13, the circuit successfully charged the line capacitance when the DRAM gate was open without the use of the sense amplifier. After confirming that our cell was working we then moved onto determining the voltage difference (ΔV 6) required to trigger the sense amplifier. This was accomplished using Formula 7 for read 1 operations and Formula 8 for read 0 operations.

$$\Delta V \approx \frac{C_s}{C_b}\left(V_{CS} - \frac{V_{DD}}{2}\right) \tag{6}$$

$$\Delta V(1) \approx \frac{C_s}{C_b}\left(\frac{V_{DD}}{2}\right) \tag{7}$$

$$\Delta V(0) \approx -\frac{C_s}{C_b}\left(\frac{V_{DD}}{2}\right) \tag{8}$$

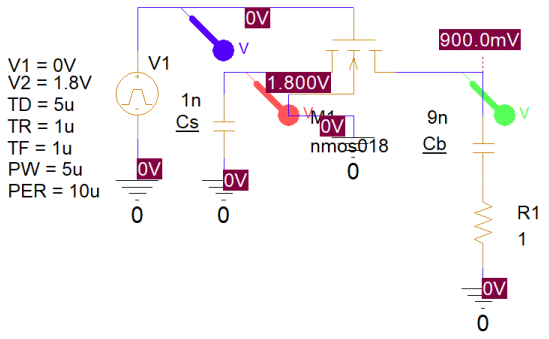

Fig. 12: PSPICE circuit of an DRAM cell

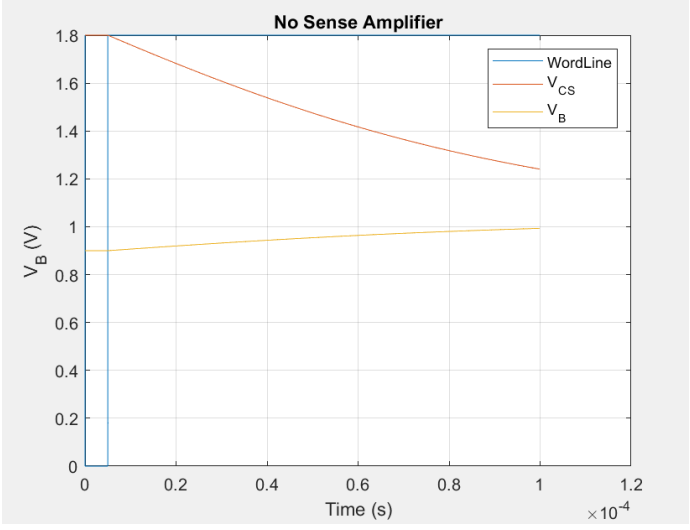

Fig. 13: DRAM capacitor charging bit line with no sense amplifier

V. Results

A. SRAM Simulation

The PSPICE simulations for read and write operations of the SRAM cell were successful. A transient analysis of the cell was made to confirm the operations followed through as the word line was raised to V_{DD}. The pulse voltage on the word line had a frequency of 100 kHz as it went from 0 to V_{DD}. To read a 1, a power source of V_{DD} is placed on the bit line (V_B) to replicate the stored 1. In Fig. 14, the circuit has a voltage source on the word line in order to determine voltages in the transistors when the word line is constantly on. The capacitances on the bit lines are 2 nF each.

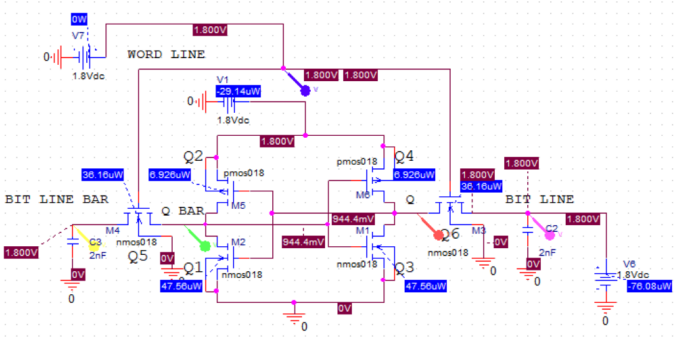

Fig. 14: PSPICE circuit of an SRAM cell for Read 1 operation

Viewing the resulting wave forms in Fig. 15, it is confirmed that as the word line is raised and both the bit lines are pre-charged at V_{DD}, $V_{\overline{B}}$ is decreasing each time the word line is increased to V_{DD}. Specifically, the voltage change (ΔV) is approximately 0.107 V. The ideal voltage difference that was desired was a ΔV between 0.1-0.2 V so that the sense amplifier can function and pull the voltage up to V_{DD}. Thus, read 1 operation was successful.

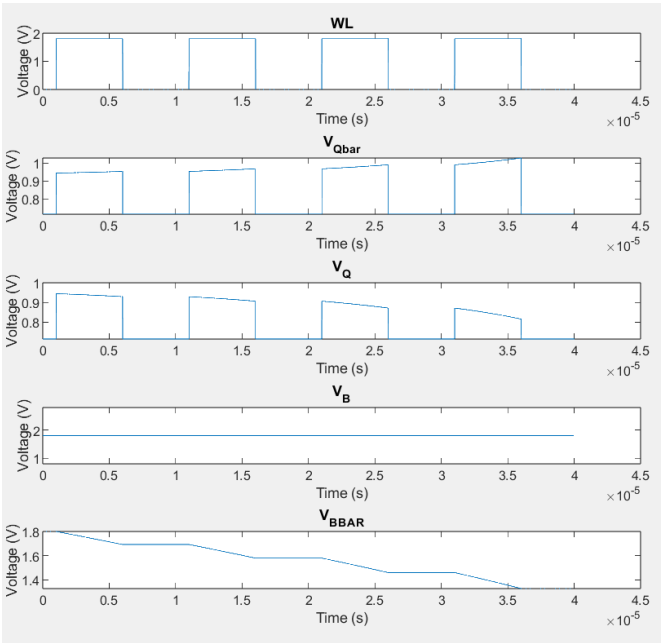

Fig. 15: PSPICE Wave forms of the SRAM read 1 operation

Reading a 0 requires V_{DD} source to be placed on the bit bar line while the bit line is only pre-charged to V_{DD}. In Fig. 16, V_B is now decreasing at a ΔV = 0.11 V, which means that when the sense amplifier is connected, it should detect this voltage difference and pull V_B down to 0 V.

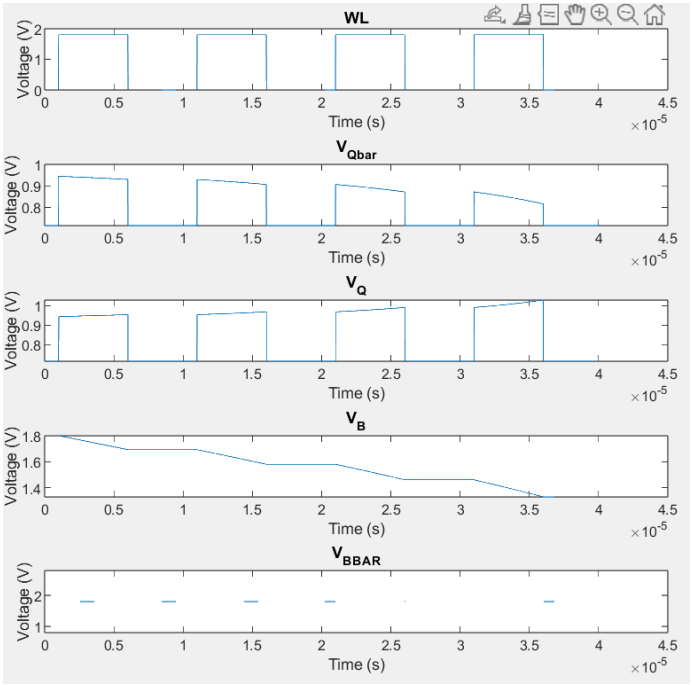

Fig. 16: PSPICE Wave forms of the SRAM read 0 operation

To write a 1, the external power source is removed from both bit lines and the cell currently stores 0 as shown in Fig. 17. The bit line capacitance (C_B) is pre-charged to V_{DD} and bit bar line is 0 V.

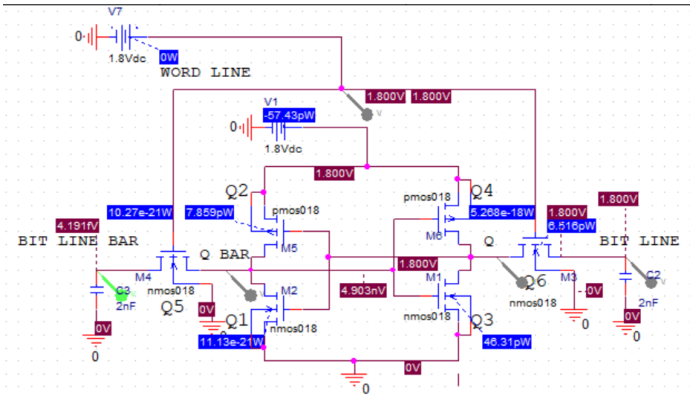

Fig. 17: PSPICE circuit of an SRAM cell for write 1 operation

Based on the waveform in Fig. 18, V_Q is high and stays high even when the word line is switching on and off, meaning that once the cell has stored a 1 the value remains unchanged while the cell is not accessed. V_B and $V_{\overline{B}}$ experience a small initial voltage change as the word line is first turned on because there is still a slight discharge of the capacitor as the word line increases above $\frac{V_{DD}}{2}$.The SRAM has now stored a 1.

Now that the SRAM cell once again has a 1 stored, an operation write 0 can be performed as visualized in Fig. 19.

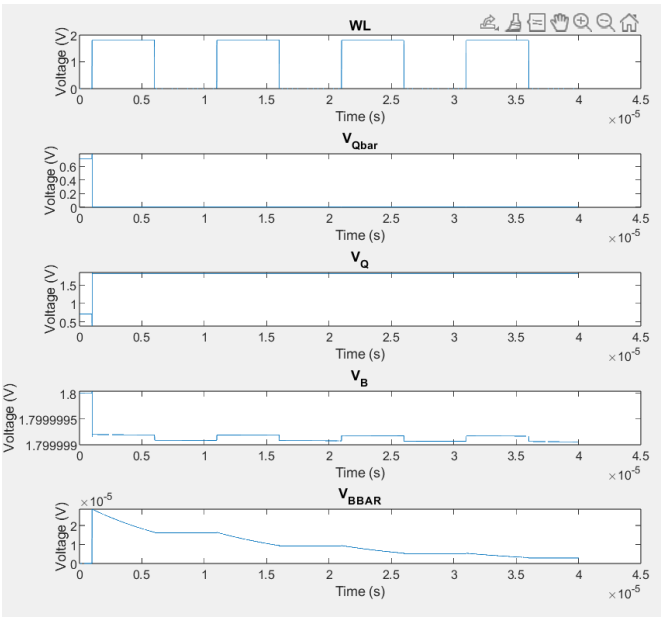

Fig. 18: PSPICE Waveforms of the SRAM write 1 operation

Only the bit-bar line capacitance will be pre-charged to V_{DD}, which results in $V_{\overline{Q}}$ at high, and V_Q at low. As the word line turns on, V_Q drops to 0 V.

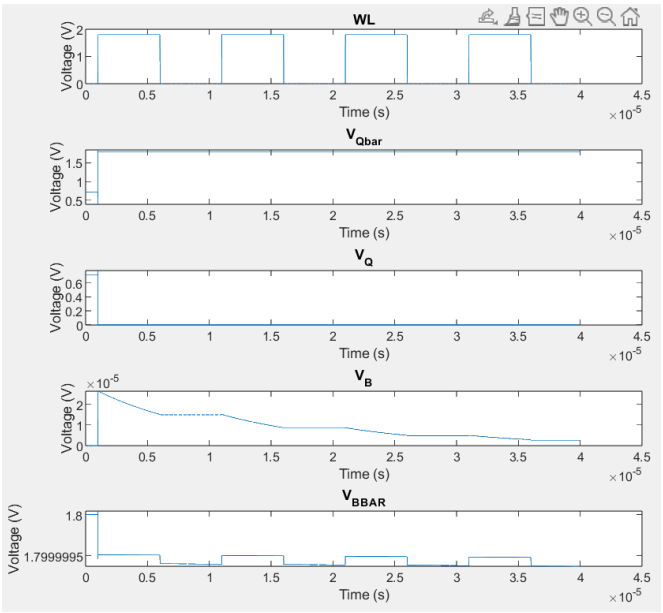

Fig. 19: PSPICE Wave forms of the SRAM write 0 operation

The SRAM cell simulated in PSPICE successfully handled its read and write operations. However, there were problems that eventually surfaced when a sense amplifier was connected to the bit lines of the single SRAM cell. As previously mentioned before, the sense amplifier functioned correctly such that during read operations (whether a read 0 or read 1), the sense amplifier would pull the initial pre-charge of V_Q (pre-charged to $\frac{V_{DD}}{2}$) down to ground or up to V_{DD}. This happens when the sense amplifier detects the voltage change (ΔV) of either V_B or $V_{\overline{B}}$ [2]. For the SRAM, it was found

that (ΔV) for read 0 and read 1 operations was 0.107 V and 0.11 V respectively.

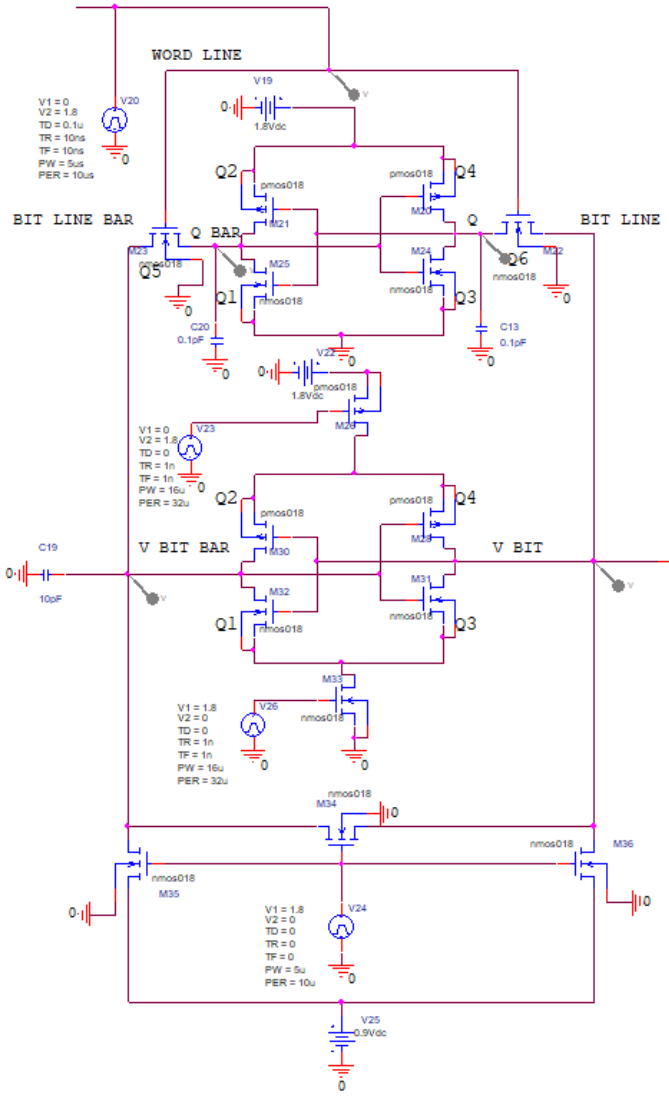

Fig. 20: PSPICE circuit of SRAM with sense amplifier

When connecting the SRAM cell to the sense amplifier as shown in Fig. 20, the first step was ensuring that the correct connections were made to the circuit. The pre-charge and equalization transistors are also installed to ensure that the voltages on the bit lines would equalize to $\frac{V_{DD}}{2}$. Once all connections were confirmed, the first operation decided was a read 1. The waveform simulation was exceuted and visualized in Fig. 21. V_Q could not be pulled up to V_{DD} at the intial rise of the word line and this may have been due to the high capacitance on the bit lines, as well as a possible issue with the pulse source frequencies ϕp and ϕs. The first change was the capacitance at the bit lines from 2 nF to 1 pF. This was a big change in capacitance, however the waveforms gave similar results as Fig. 21, so this was not the issue. After many frequency changes in the pulse voltage source, the sense amplifier was not able to sense the voltage change enough to pull up V_Q to V_{DD}

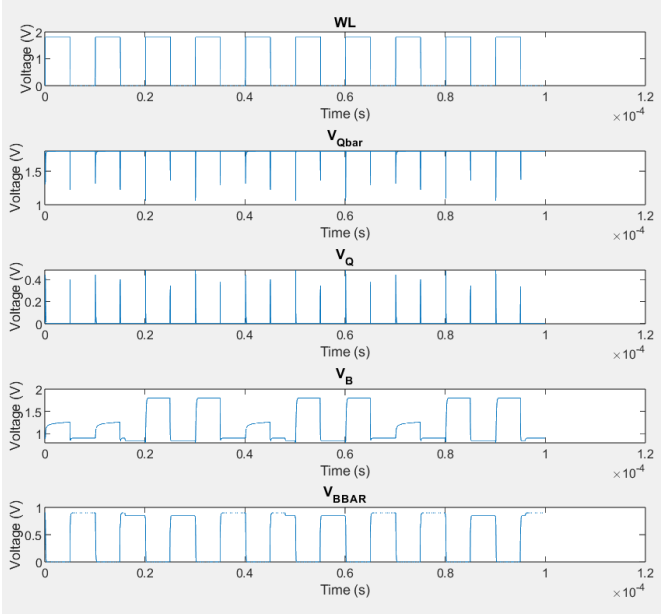

Fig. 21: PSPICE Waveform of SRAM with sense amplifier

B. DRAM Simulation

The integration of the sense amplifier and a dummy cell, as depicted in Fig. 22, required validation of the circuit's functionality before proceeding with further testing.

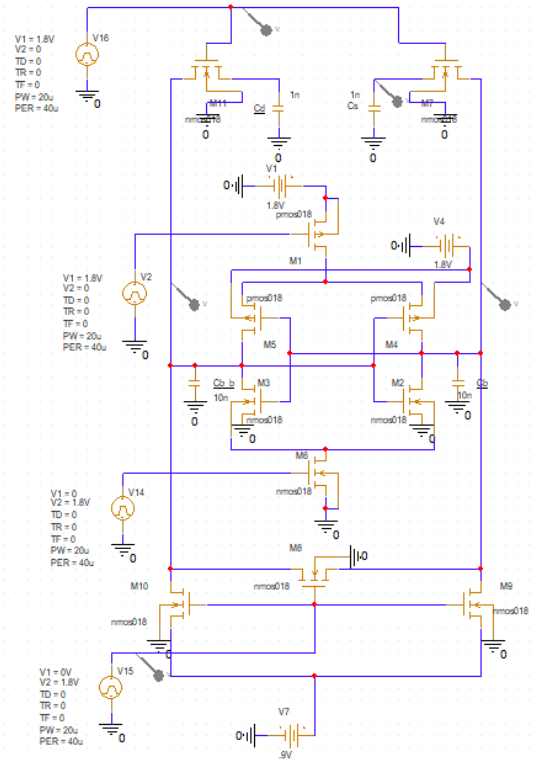

Fig. 22: DRAM cell with pre-charge, equalization sense amplifying circuitry

To determine if the circuit worked a test was performed. This involved initial activation of the pre-charge and equalization circuits. After a designated interval, these circuits

were turned off, and the sense amplifier was engaged. The anticipated outcome was an increase in the charge of the bit line capacitor from 0 to 0.9V, followed by the sense amplifier driving the lines to V_{DD} and ground, respectively. This test was successful, as evidenced by the results shown in Fig. 23, which set the stage for further evaluation of the read and write functionalities of the circuit.

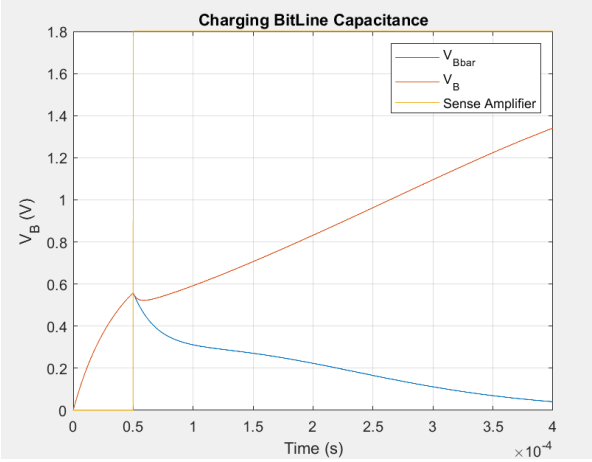

Fig. 23: Pre-charge and equalization test on bit line capacitance

Having established the functionality of the pre-charge and equalization circuits, we proceeded to assess the read and write operations of our DRAM cell. The initial test focused on the write zero operation. This procedure was consisted of grounding the bit line and enabling the word line resulting in the discharge of the internal capacitor, thereby storing a zero. The execution of this operation is captured in Fig. 24.

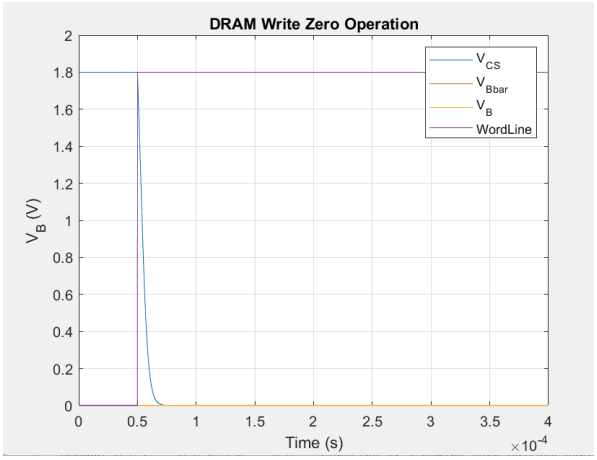

Fig. 24: DRAM cell write zero operation

The following test focused on the write one operation. This procedure consisted of placing V_{DD} on the bit line and enabling the word line resulting in the charging of the internal capacitor, thereby storing a one seen in Fig. 25.

Following the verification of the write operations, we conducted tests for the read operations. The first of these was a read one test, which started by activating the pre-charge and equalization circuit to charge the bit line to $V_{DD}/2$. After some

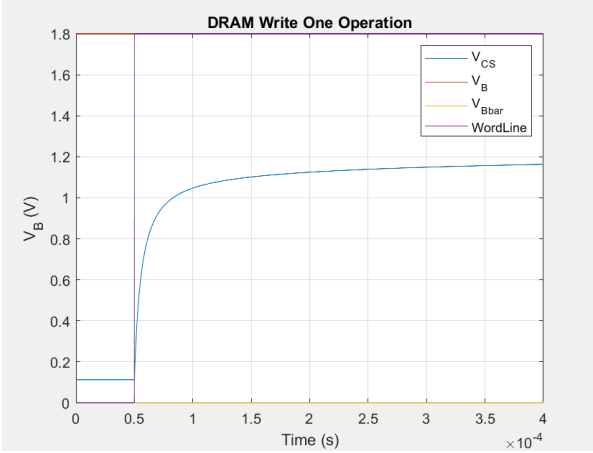

Fig. 25: DRAM cell write one operation

time, the pre-charge and equalization circuits were deactivated, and the sense amplifier was then enabled. The sense amplifier was expected to detect the slight increase in voltage due to the charge from the internal capacitor and consequently elevate the bit line voltage to V_{DD}. Although the sense amplifier appeared to be functioning, an issue was observed where the bit line voltage did not fully reach V_{DD}, indicating a potential discrepancy in the expected operation. This operation is depicted in Fig. 26.

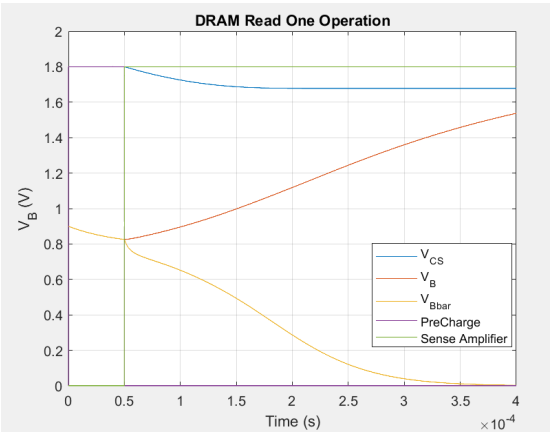

Fig. 26: DRAM cell read one operation

Similar to the read one test, the read zero began with engaging the pre-charge and equalization circuit, which brought the bit line voltage to $V_{DD}/2$. Once this state was achieved and maintained for a certain duration, the pre-charge and equalization circuits were disabled, followed by the sense amplifier activation. In this scenario, the sense amplifier was anticipated to sense a decrease in voltage due to the absence of charge from the internal capacitor, thereby driving the bit line voltage all the way down to ground (0V). Contrary to the read one operation where the bit line did not achieve the full V_{DD}, in the read zero test, the sense amplifier functioned correctly, pulling the bit line to a complete 0V, confirming the successful detection of a zero. This operation is illustrated in Fig. 27.

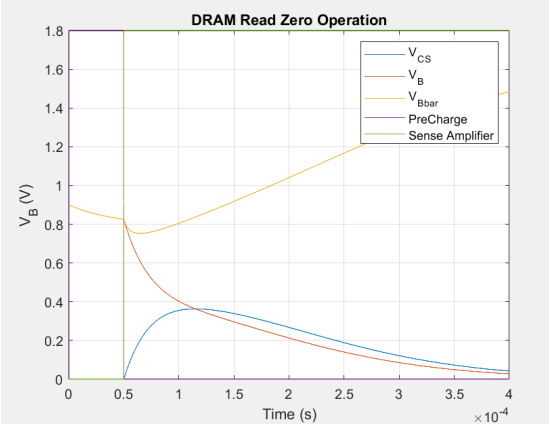

Fig. 27: DRAM cell read zero operation

VI. Future Works

The row and column decoders made in PSPICE were made for the opportunity to create a 4 by 4 bit comparison of the designed SRAM and DRAM in this paper. Although the decoders were not able to be utilized in this paper, future plans are to incorporate the decoders into the overall memory designs as they are essential for memory chips of high cell arrays.

VII. Conclusion

In this paper, both SRAM and DRAM were compared and analyzed through PSPICE simulation for their performance at the CMOS transistor level. Although the sense amplifier was not sensitive enough to properly execute read operations in the SRAM designed, it is proven to work in DRAM and this is understandable as with less transistors, there is less parasitic capacitance in the circuit, and therefore less issues with sizing transistors. The SRAM cell is simpler in structure than DRAM, so it offers rapid writing and reading operations. SRAM offers lower power consumption and it does not require the constant refreshing as opposed to DRAM. However, DRAM can reach higher memory density and allow a more cost-effective approach to large memory requirements in systems. The unique differences in both cells are what make both often used in many computer systems to optimize performance and costs.

References

[1] S. Lokesh et al. “Design of Read and Write Operations for 6t Sram Cell”. In: *IOSR Journal of VLSI and Signal Processing* 8.1 (2018), pp. 43–46. DOI: 10.9790/4200-0801014346. URL: https://www.iosrjournals.org/iosr-jvlsi/papers/vol8-issue1/Version-1/E0801014346.pdf.

[2] A. S. Sedra and Kenneth Carless Smith. *Microelectronic circuits*. New York ; Oxford Oxford University Press, 2015.