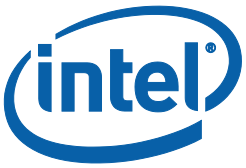

Intel Joule Module

Development Kit Hardware Guide

December 2016

Revision 1.0

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Revision History

Revision Number	Description	Revision Date
1.0	Initial Release	December 2016

1 Introduction

1.1 Scope

This document describes the devices and circuitry on the expansion board (also known as the Development Kit) for the Intel® Joule™ compute module.

The expansion board is a development platform for prototyping and exploring application solutions powered by the Intel Joule module. As such, certain devices and features might not function, depending on the firmware installed, the operating system installed, and devices attached to ports and connectors.

Scope of this document is limited to functions performed by the expansion board.

Consult datasheets from the original device manufacturer and available information provided by the operating system vendors for software environments to fully understand what is available from the original device manufacture.

1.2 Acronyms and terminology

Term or Acronym	Description or Definition
AC	Alternating Current
BIOS	Basic Input Output System
CC	Configuration Channel. Relates to USB Type-C connectors.
CSE	Converged Security Engine. Responsible for retrieving and validating all firmware.
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
eMMC	Embedded MultiMedia Card
FFC	Flexible Flat Cable
GPIO	General purpose input / output
HDMI*	High Definition Multimedia Interface
I2C	Inter-IC Bus; also known as the “I-squared-C bus”
I2S	Integrated Interchip Sound; also known as the “I-squared-S bus”

Term or Acronym	Description or Definition
IC	Integrated Circuit
LED	Light Emitting Diode
LCD	Liquid Crystal Display
NC	No Connect. Signal is not used or is to be left floating.
Net Names	Signals on the printed circuit board are often referred to by their signal, or net name. The name of a signal often changes when passing through a device.
OTG	On-The-Go; specifically related to the USB On-The-Go technology. OTG ports are required to provide a minimum power to devices.
OS	Operating System
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
SD Card	Secure Digital card
SoC	System on Chip
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

1.3 References

Document	Document Location
Intel® Joule™ Module Datasheet	https://software.intel.com/en-us/articles/intel-joule-module-datasheet
Intel® Joule™ Expansion Board Schematics and BOM	https://software.intel.com/en-us/articles/intel-joule-expansion-board-schematic
Intel® Joule™ Module User Guide	https://software.intel.com/en-us/intel-joule-getting-started
Mechanical Descriptor for Intel® Joule™ Platform	http://www.intel.com/content/www/us/en/support/boards-and-kits/000022366.html
Thermal Management Overview for the Intel® Joule™ Module Developer Kit	http://www.intel.com/content/www/us/en/support/boards-and-kits/000023095.html

Document	Document Location
Troubleshooting and FAQ – Using the Intel® Joule™ development platform	https://software.intel.com/en-us/troubleshooting-and-faq-for-joule

1.4 Part numbers

The part numbers listed throughout this document are the specific parts on the Intel Joule expansion board at the time of publication. Those parts may in the future be replaced with equivalent parts from other manufacturers.

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2 High Level Description

2.1 Intel Joule module to expansion board interface

The module interfaces to the expansion board through twin, high-density 100-pin connectors, J2 and J3, which respectively mate to J6 and J7 on the expansion board.

Caution: The board-to-board connectors are rated for a maximum of 30 socketing cycles. You risk signal degradation after seating and removing the compute module more than 30 times.

2.2 Expansion board feature highlights

The expansion board provides two 40-pin (0.1 x 0.1 pitch) breakout connectors that expose various features, power signals, and communication buses of the compute module. The expansion board also provides some standard, physical interface ports.

Some signals to and from the module are routed directly to the breakout connectors (J12 and J13) and physical ports; others receive level-conditioning when in transit on the board.

Table 1. Expansion board features

Component	Description
Power input	Physical input connector, fused for current protection
Physical interfaces	Physical connectors for a number of module interfaces are provided by the expansion board: • Micro USB Type A • USB Type-C • Micro USB Type-B for serial debug (UART bridge) • Micro HDMI*
Level translation	The expansion board provides open collector type level translation and requires pullups on the attached mezzanine cards to the end-user's desired voltage levels, not to exceed 3.3 VDC.
Voltage regulation	Expansion board provides additional voltage regulators to enable the level transition and conditioning devices.
Configuration jumpers	Header pins provide the ability to disable booting from the SD Card or from the eMMC image on the module.

2.3 Block diagram

Figure 1 and Figure 2 show the high-level block diagram for the expansion board in two parts for better readability.

Figure 1. Expansion board block diagram – module connector J2 to J12 breakout connector

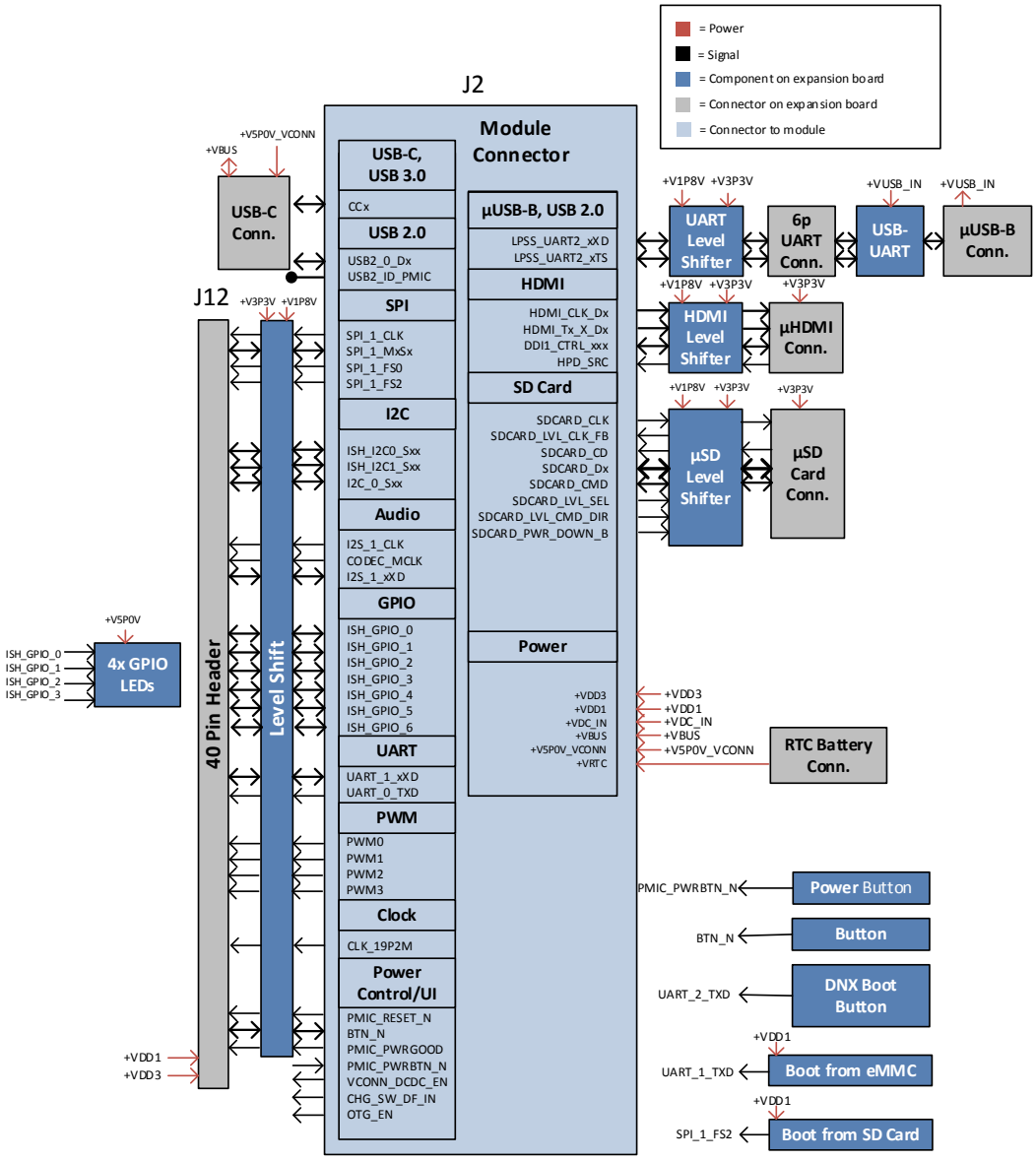
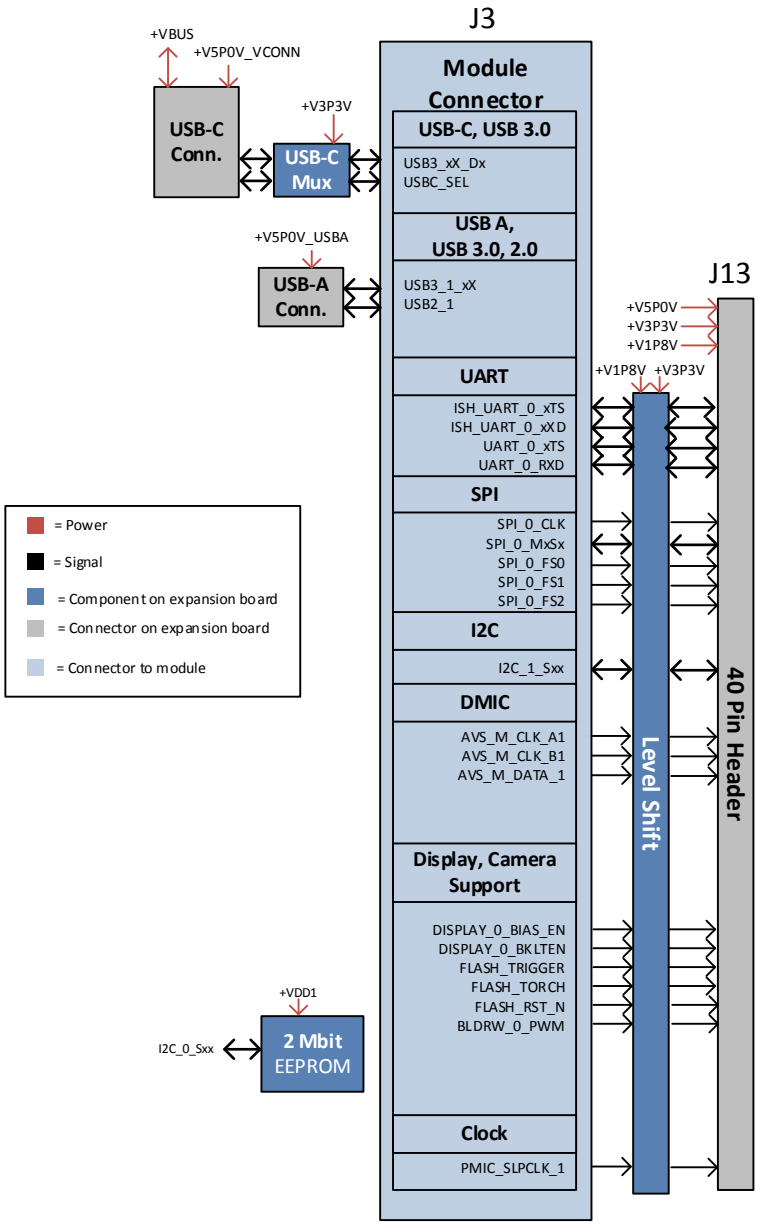


Figure 2. Expansion board block diagram – module connector J3 to J13 connector



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3 Expansion Board Interfaces

This section provides a visual overview of the ports, connectors, and mechanical interfaces of the Intel Joule expansion board; shown without an Intel Joule module installed.

Figure 3. Intel Joule expansion board - top view

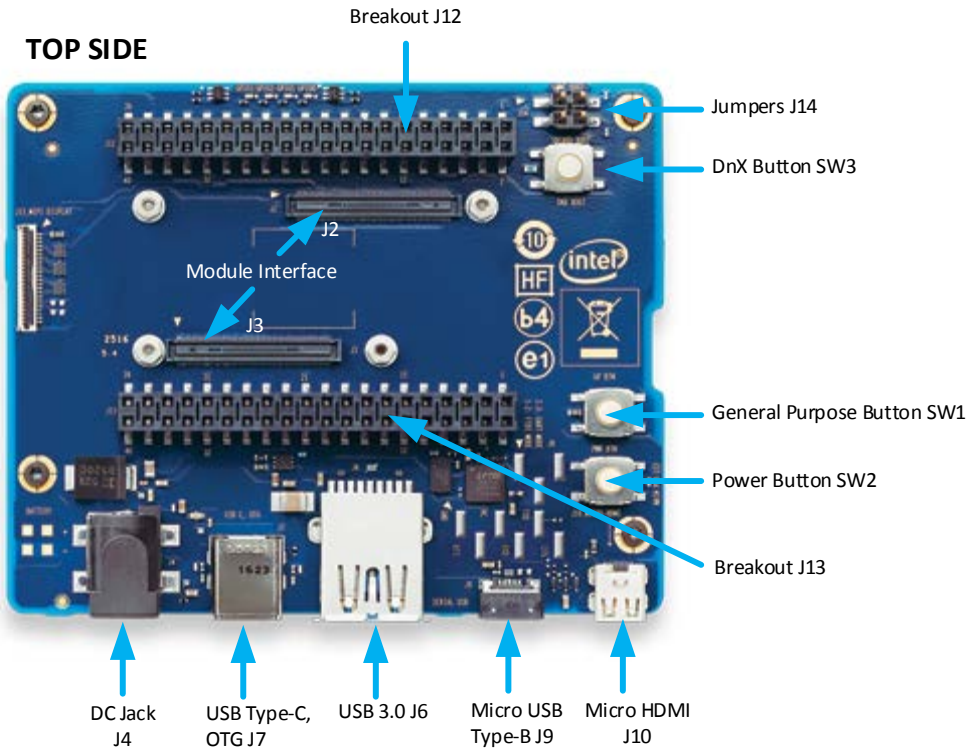
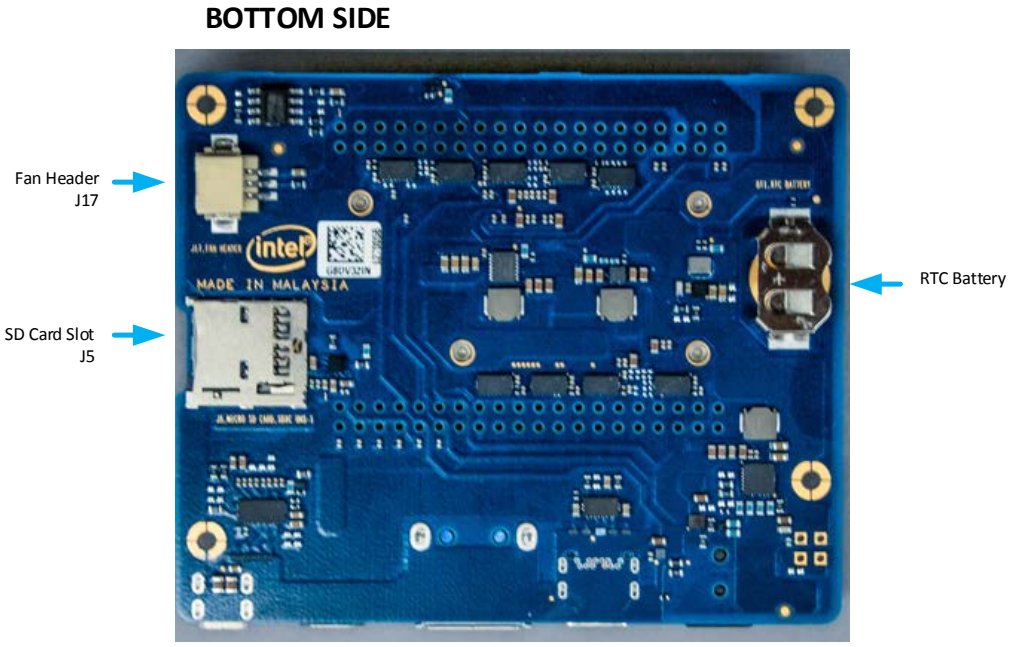


Figure 4. Intel Joule expansion board - bottom view



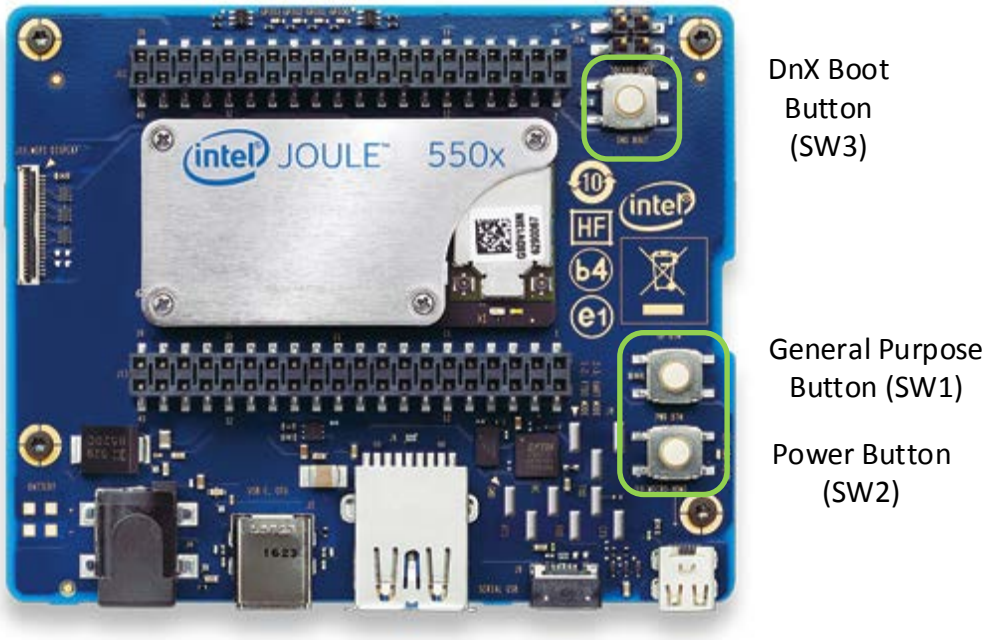
3.1 Buttons, jumpers, and LEDs

The Intel Joule expansion board contains three buttons. Two of the three buttons have predefined operation, while the third button is user defined. The three buttons are titled:

- Power Button (PWR BTN)
- DNX Boot Button (DNX BOOT)
- General Purpose Button (GP BTN)

Refer to Figure 5 for the locations of the buttons.

Figure 5. Intel Joule expansion board buttons



3.1.1 Power button (SW2)

The power button is connected to the PMIC_PWRBTN_N signal of the module. When the button is pressed, the PMIC_PWRBTN_N signal is pulled to ground, driving the PMIC_PWRBTN_N signal to a low state. When the button is released, the PMIC_PWRBTN_N signal is pulled high, to +VSYS in the module.

Note: The low time durations of the PMIC_PWRBTN_N signal result in various actions on the module. Refer to the Intel® Joule™ Module Datasheet for specific information and usage for the PMIC_PWRBTN_N signal and the resulting actions.

3.1.2 DNX boot button (SW3)

The DNX boot button is connected to the UART_2_TXD signal of the module. When the button is pressed, the UART_2_TXD signal is pulled high through a 100Ω resistor to +VDD1 (1.8 volts). When the button is released, the UART_2_TXD signal is left floating, but relies on a 20kΩ internal pull-down within the module SoC to insure a low-level signal.

The DNX boot button is used to initiate a BIOS programming cycle when pressed and held during a power-up cycle. At the rising edge of the module's PMIC_PWRGOOD signal (for example during a power-up cycle), the UART_2_TXD is sampled by the module SoC. If the UART_2_TXD is sampled as a high signal, then the SoC initiates a BIOS update from the USB Type-C port. Similarly, if the UART_2_TXD signal is sampled as a low signal (for example DNX boot button released) on the rising edge of PMIC_PWRGOOD, then a BIOS update is not initiated and the boot process continues normally.

3.1.3 General purpose button (SW1)

The general purpose button is available to be defined by the software developer. It is connected to the BTN_N signal of the module. When the button is pressed, the BTN_N signal is shorted to ground, driving the BTN_N signal to a low state. When the button is released, the BTN_N signal is pulled high, to +VDD1 (1.8 volts).

Refer to the Intel Joule Module Datasheet for the function mapping of the BTN_N signal.

3.2 Boot-option strapping jumpers (J14)

Jumper block J14 provides the ability to selectively enable boot sources for the expansion board, specifically, the ability to enable booting from the SD card or from eMMC.

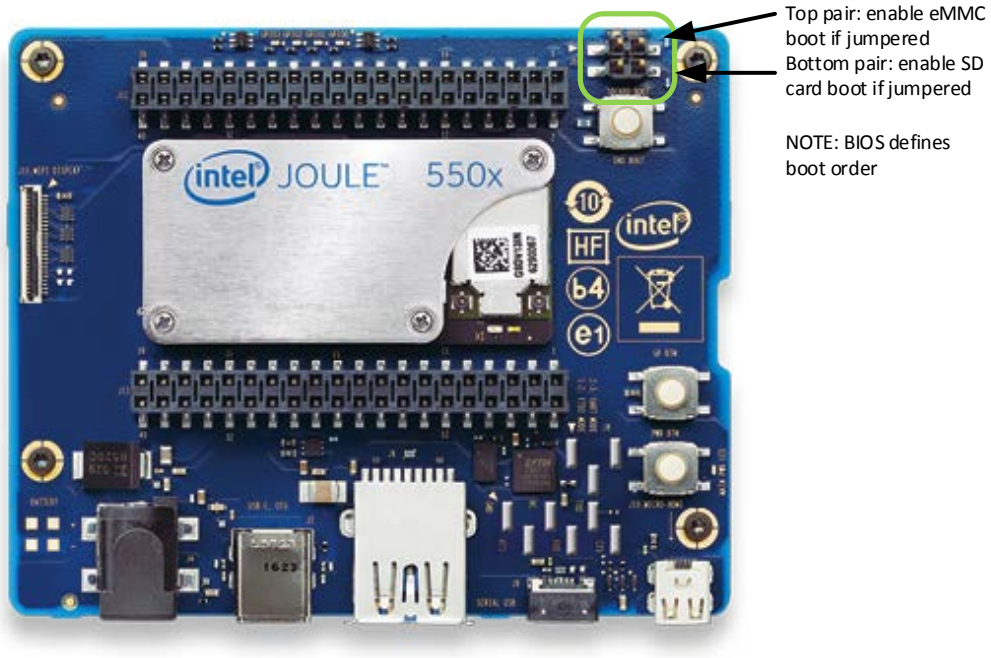
Refer to Figure 6 for the locations of the jumper block.

The jumper must be installed prior to a power-up of the expansion board, as the state of the jumpers is sampled by the module at the rising edge of the PMIC_PWRGOOD signal, during the power-up process.

- Placing a jumper across pins 1 and 2 of J14 enables booting from eMMC.
- Placing a jumper across pins 3 and 4 of J14 enables booting from the SD card.

Note: The default configuration is no jumpers installed.

Figure 6. Expansion board boot-strapping jumpers (J14)



3.3 Power LED (CR9)

A main power LED is located near the power switch (SW2) (refer to Figure 7 for the location) and is enabled when all expansion board power rails are stabilized and a general power good state is achieved.

3.4 General purpose LEDs

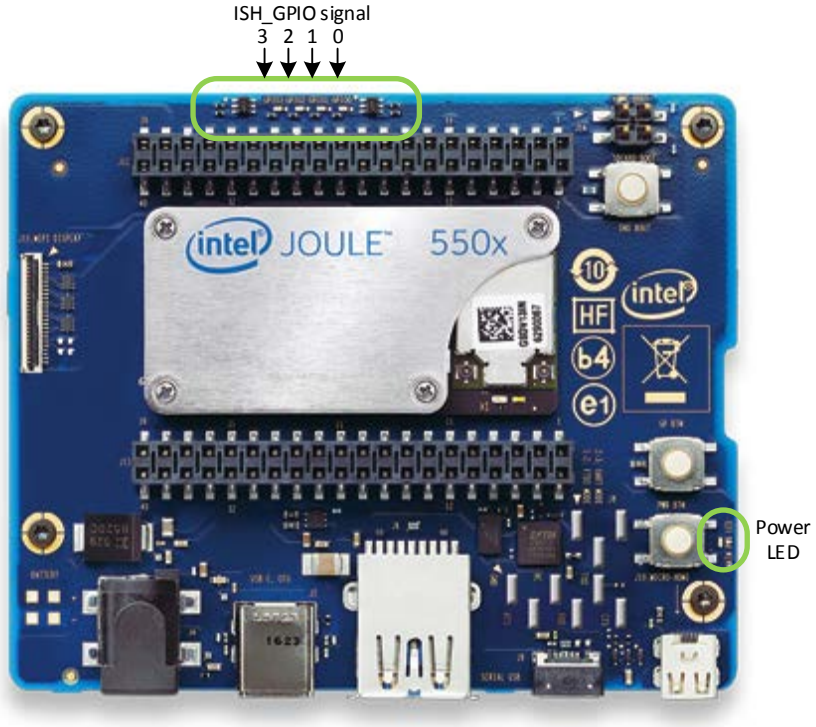
There are four general purpose LEDs located in the upper center area of the expansion board. Refer to Figure 7 for the location of the LEDs. The LED is turned on when the related GPIO signal is high, regardless of whether the GPIO is configured as an input or an output.

In addition to being user programmable, these LEDs are used by the BIOS to indicate progression of the boot process or other information. All four LEDs are illuminated when BIOS passes code execution to the operating system (OS). Depending on the BIOS build, these GPIO lines can be left high or low, and set as either input or output. See the BIOS release notes for additional information.

Table 2. General purpose LED mapping

LED Reference Designator	Net Name	Breakout Pin #	Linux* GPIO
GPIO0	ISH_GPIO_0	J12-35	337
GPIO2	ISH_GPIO_1	J12-33	339
GPIO1	ISH_GPIO_2	J12-31	338
GPIO3	ISH_GPIO_3	J12-29	340

Figure 7. Intel Joule expansion board LEDs



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4 Breakout Connectors

The Intel Joule expansion board contains two forty-pin connectors, each having a 2x20 configuration at 0.1-inch spacing, to enable external circuit connections.

These connectors are referred to as the breakout connectors. They expose several interfaces and module signals required to develop complete systems.

These breakout connectors provide access to the following interfaces:

- Two SPI ports
- Three UARTs
- Five I2C ports
- One I2S port
- Four PWM interfaces
- Eight dedicated GPIO signals, and seven user programmable GPIO signals
- Two digital microphone inputs
- Various voltage rails and power signals

The expansion board provides open collector type level translation (shifting) of the module 1.8 VDC I/O lines and requires pullups on the attached mezzanine cards to the end-user's desired voltage levels typically used in the development phase, not to exceed 3.3 VDC. Details of any level translation, conditioning or buffering applied by the expansion board are found in the respective sections for those specific interfaces where such is applied.

4.1.1 Breakout connector J12

The table below provides the pin assignment, signal name, and description for the signals on the breakout connector J12. The default breakout usage refers to the vantage point of the expansion board. For example, the SPI_1_MISO_LS signal originates in the breakout board and is delivered to the expansion board, therefore it is an input.

These signals are mapped by various operating systems in different ways. These mappings can change over time and with BIOS updates. This table does not address those mappings. Refer to the Intel Joule module website for current mappings for supported operating systems.

Table 3. Breakout connector J12 pinout

J12 Pin	Net Name at Breakout	Signal Description	Default Breakout Usage	Module Pin
1	GPIO_22_LS	General purpose input/output	Input	J2 - 94
2	SPI_1_MISO_LS	SPI port 1 receive data.	Input	J2 - 63
3	PMIC_RESET_N	Active low output from the expansion board to the module that controls the power state of the module and, by extension, the expansion board, see the Intel® Joule™ Module Datasheet for how the PMIC_PWRBTN_N signal controls the module power state based on duration of the low signal.	Input	J2 - 9
4	SPI_1_MOSI_LS	SPI port 1 transmit data	Output	J2 - 51
5	CLK_19P2M_LS	19.2 MHz clock	Output	J2 - 71
6	SPI_1_FS0_LS	SPI port 1 slave select 0	Output	J2 - 55
7	UART_0_TXD_LS[1]	UART port 0 transmit data, hardware strap with reserved functionality	Output	J3 – 15
8	SPI_1_FS2_LS	SPI port 1 slave select 2, hardware strap with disable boot from SD card functionality	Output	J2 - 14
9	PMIC_PWRGOOD_LS	Active high output signal from the module to the expansion board that latches the state of the module strapping options. This signal also indicates if +VDD1 and +VDD3 power supplies from the module are within specification.	Output	J2 - 33
10	SPI_1_CLK_LS	SPI port 1 clock	Output	J2 - 53
11	I2C_0_SDA_LS	I2C port 0 data, used for configuration EEPROM	Input/Output	J2 - 18
12	I2S_1_RXD_LS	I2S receive data	Input	J2 - 47
13	I2C_0_SCL_LS	I2C port 0 clock, used for configuration EEPROM	Output	J2 - 57
14	I2S_1_TXD_LS	I2S transmit data	Output	J2 – 49
15	ISH_I2C_0_SDA_LS	I2C port 0 data, mapped to I2C5	Input/Output	J2 - 18
16	I2S_1_FS_LS	I2S frame sync	Output	J2 - 45
17	ISH_I2C_0_SCL_LS	I2C port 0 clock, mapped to I2C5	Output	J2 - 16
18	I2S_1_CLK_LS	I2S-bit clock supplied by the module in master mode and serves as an input in slave mode.	Input/Output	J2 - 39
19	ISH_I2C_1_SDA_LS	I2C port 1 data, mapped to I2C6	Input/Output	J2 - 23
20	CODEC_MCLK_LS	MCLK for Master Mode operation of I2S audio	Output	J2 - 43
21	ISH_I2C_1_SCL_LS	I2C port 1 clock, mapped to I2C6	Output	J2 - 21
22	UART_1_TXD_LS	UART port 1 transmit data, hardware strap with disable boot from eMMC functionality	Output	J2 - 28
23	ISH_GPIO_6_LS	General purpose input/output 6	Output	J2 – 31

J12 Pin	Net Name at Breakout	Signal Description	Default Breakout Usage	Module Pin
24	UART_1_RXD_LS	UART port 1 receive data.	Input	J2 - 26
25	ISH_GPIO_5_LS	General purpose input/output 5	Output	J2 - 38
26	PWM_0_ LS	Programmable pulse width modulator port 0	Output	J2 - 1
27	ISH_GPIO_4_LS	General purpose input/output 4	Output	J2 - 29
28	PWM_1_LS	Programmable pulse width modulator port 1	Output	J2 - 3
29	ISH_GPIO_3_LS	General purpose input/output 3, set as output by BIOS until reconfigured[2]	Output	J2 - 34
30	PWM_2_LS	Programmable pulse width modulator port 2	Output	J2 - 22
31	ISH_GPIO_2_LS	General purpose input/output 2, set as output by BIOS until reconfigured[2]	Output	J2 - 32
32	PWM_3_LS	Programmable pulse width modulator port 3	Output	J2 – 24
33	ISH_GPIO_1_LS	General purpose input/output 1, set as output by BIOS until reconfigured[2]	Output	J2 - 27
34	+VDD1	System 1.8 VDC	Output	J2 - 36
35	ISH_GPIO_0_LS	General purpose input/output 0; set as output by BIOS until reconfigured[2]	Output	J2 - 25
36	GND	System Ground	Common Ground	Multiple
37	GND	System Ground	Common Ground	Multiple
38	GND	System Ground	Common Ground	Multiple
39	GND	System Ground	Common Ground	Multiple
40	+VDD3	System 3.3 VDC	Output	J2 - 30

1. UART_0_TXD is routed to a hardware-strapping pin on the Intel Joule module. Adding a pullup to this net or loading it with external circuitry such that it is not at a valid low input voltage at the rising edge of PMIC_PWRGOOD, on start-up will result in disabling aspects of the Converged Security Engine (CSE) which is responsible for retrieving and validating all firmware.
2. During BIOS execution, the ISH_GPIO_0 through _3 signals are configured as outputs and change state to indicated BIOS progression. End users should take this into account in their design.

4.1.2 Breakout connector J13

The table below provides the pin assignment, signal name, and description for the signals on the breakout connector J13. The default breakout usage refers to the vantage point of the expansion board. For example, the SPI_0_MISO signal originates in the breakout board and is delivered to the expansion board, therefore it is an input.

These signals are mapped by various operating systems in different ways. These mappings can change over time and with BIOS updates. This table does not address those mappings. Refer to the Intel Joule module website for current mappings for supported operating systems.

Table 4. Breakout connector J13 pinout

J13 Pin	Net Name at Breakout	Signal Description	Default Breakout Usage	Module Pin
1	GND	GND	Common Ground	Multiple
2	V5P0V	5V	Output	N / A
3	GND	GND	Common Ground	Multiple
4	V5P0V	5V	Output	N / A
5	GND	GND	Common Ground	Multiple
6	V3P3V	3.3V	Output	N / A
7	GND	GND	Common Ground	Multiple
8	V3P3V	3.3V	Output	N / A
9	GND	GND	Common Ground	Multiple
10	V1P8V	1.8V	Output	N / A
11	Reserved	Reserved	Not used / Reserved	J3 - 68
12	V1P8V	1.8V	Output	N / A
13	Reserved	Reserved	Not used / Reserved	J3 - 64
14	GND	GND	Common Ground	Multiple
15	Reserved	Reserved	Not used / Reserved	J3 - 58
16	FLASH_TORCH	GPIO Pin 7	Output	J3 - 75
17	Reserved	Reserved	Not used / Reserved	J3 - 58
18	FLASH_RST_N	GPIO Pin 8	Output	J3 - 73
19	SPI_0_FS0	SPI port 0 slave select 0	Input	J3 - 73
20	FLASH_TRIGGER	GPIO Pin 9	Output	J3 - 71
21	SPI_0_FS1[2]	SPI port 0 chip select 1	Output	J3 - 79
22	AVS_M_DATA_1	Microphone data for channels A and B	Input	J3 - 66
23	SPI_0_FS2	SPI port 0 chip select 2	Output	J3 - 53
24	AVS_M_CLK_B1	Microphone clock for channel B (secondary microphone)	Output	J3 - 62
25	SPI_0_CLK	SPI port 0 clock	Input	J3 - 59
26	AVS_M_CLK_A1	Microphone clock for channel A (voice trigger microphone)	Output	J3 - 52
27	SPI_0_MOSI	SPI port 0 transmit data	Output	J3 - 57
28	UART_0_RXD	UART port 0 receive data (Note: UART_0_TXD is on the J12 connector)	Input	J3 - 51

J13 Pin	Net Name at Breakout	Signal Description	Default Breakout Usage	Module Pin
29	SPI_0_MISO	SPI port 0 receive data	Input	J3 - 49
30	UART_0_RTS	UART port 0 ready-to-send	Output	J3 - 55
31	I2C_1_SDA	I2C port 1 data	Input/Output	J3 - 45
32	UART_0_CTS	UART port 0 clear-to-send	Input	J3 - 47
33	I2C_1_SCL	I2C port 1 clock	Output	J3 - 43
34	ISH_UART_0_TXD[1]	Although titled UART, function is configured as GPIO Pin 10	Output	J3 - 15
35	I2C_2_SDA	I2C port 1 data	Input/Output	J3 - 26
36	ISH_UART_0_RXD	Although titled UART, function is configured as GPIO Pin 11	Input	J13 - 13
37	I2C 2 SCL	I2C port 2 clock	Output	J3 - 28
38	ISH_UART_0_RTS[1]	Although titled UART, function is configured as GPIO Pin 12	Output	J3 - 11
39	PMIC_SLPCLK_1	32.768 kHz RTC	Output	J3 - 7
40	ISH_UART_0_CTS	Although titled UART, function is configured as GPIO Pin 13	Input	J3 - 9

1. ISH_UART_0_TXD pin 34 and ISH_UART_0_RTS pin 38 are routed to a hardware-strapping pin on the Intel Joule module. Adding a pullup to this net or loading it with external circuitry such that it is not at a valid low input voltage at the rising edge of PMIC_PWRGOOD, on start-up will result in boot failure due to improper clock selection.
2. SPI_0_FS1, pin 21, is routed to a hardware-strapping pin on the Intel Joule module. Adding a pullup to this net or loading it with external circuitry such that it is not at a valid low input voltage at the rising edge of PMIC_PWRGOOD, on start-up will result in boot failure due to boot halt being enabled.

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5 Powering the Expansion Board

The Intel Joule expansion board is designed to accept power from either the DC barrel jack (J4) or the USB Type-C connector (J7). When both the DC barrel jack and USB power are applied, the board takes its power through the barrel jack by default.

When it is booted, the input source cannot be switched without rebooting the platform.

It is recommended to use the DC power input jack while developing on the platform because it is easier to ensure input power quality over a direct DC connection.

Any source connected to the J4 input must meet these specifications:

- Voltage: 12.0 volts, ±3%
- Current: 2.7 amps, minimum – the expansion board contains a 3.5 amp fuse
- Safety Ratings: Listed LPS or Class 2

When using the USB Type-C as a power source, the developer must confirm the host system provides the required quality and capacity of input power. Excessive loads on a Type-C power bus can cause development platform and/or host instability.

As an Intel Joule-based project matures, the workload and platform power data can be used to guide an optimal power source that meets the intended form-factor goals.

5.1 DC power jack input (J4)

The J4 power jack on the expansion board is a surface mounted, RoHS compliant device. The connector is manufactured by CUI INC* as model number: PJ-002AH-SMT-TR.

- The inner pin is positive voltage becoming the +VDC_IN signal on the expansion board. The +VDC_IN signal passes through a discrete circuit that provides polarity protection and filtering before reaching the input power multiplexer, U18.
- Outer ring is ground; this is common with module ground and connector shields.
- The jack accepts a 5.5 mm plug to a depth of 8.9 mm.

Refer to the manufacturer's datasheet for additional details and the latest information.

Table 5. DC power jack electrical specifications

Source	Item	Min	Typ	Max	Units	Conditions
DC Power Jack	V_{DCIN}	7.0	12.0	12.4	V	At V_{DCIN} pin of DC power jack
	I_{DCIN}			2.7	A	At V_{DCIN} of 12.0 volts

Note: Minimum voltage 7.0 is only for lightly loaded configurations. Attaching accessories will require the more typical voltage of 12.0.

5.2 USB Type-C power input (J7)

The J7 Type-C connector accepts a 5 VDC level and is capable of delivering a maximum of 3 A into the expansion board. J7 pins A4, B4, A9 and B9, are +VBUS; J7 pins A1, B1, A12, B12 are ground.

The 4 positive voltage input lines are common on the expansion board and become +VBUS_USB3, which is conditioned to become +VBUS going into the power mux.

+VBUS is also connected to the module at J3 pin 1 as the USB adapter connection sense line.

When powering the expansion board from a USB PD charger/adaptor only capable of 5 volt output, workloads executing must not exceed a total current consumption of 3.0 amps, including any mezzanine boards and peripheral devices attached to it.

When powering the expansion board from a USB PD charger/adaptor capable of 9 volt output, the BIOS automatically negotiates PD output voltage from 5 volt to 9 volt operation.

Table 6. USB type-C power input electrical specifications

Source	Item	Min	Typ	Max	Units	Conditions
Type-C Connector	V_{BUS1}	4.75	5	5.25	V	At V_{BUS} pin of Type-C connector
	I_{BUS1}	3.0		3.5	A	
	V_{BUS2}		9	12.4	V	At V_{BUS} pin of Type-C connector
	I_{BUS2}	1.5		3.5	A	

The USB power system, OTG, and interface details are covered in Section 15.1.

5.3 Battery path

There are four (4) through-hole connection points near the J4 VDC input connector; a +VBATTERY trace begins here and is routed to the power management device, EU2.

Note: No battery enabling, charging, or support services are currently provided by the expansion board.

All battery solutions must be completely external to the expansion board except for standard communication and I/O interfaces. The EU2 device serves as the +VSYS voltage regulator.

5.4 Power-on and shut-down signaling

A power source must be available at either the DC input jack or the USB Type-C connector, which both connect to the power mux, before power on can be initiated.

Closing SW2 pulls PMIC_PWRBTN_N low, enabling the module to begin the power-on logic sequence. PMIC_PWRBTN_N is also connected to the module on J2 pin 9.

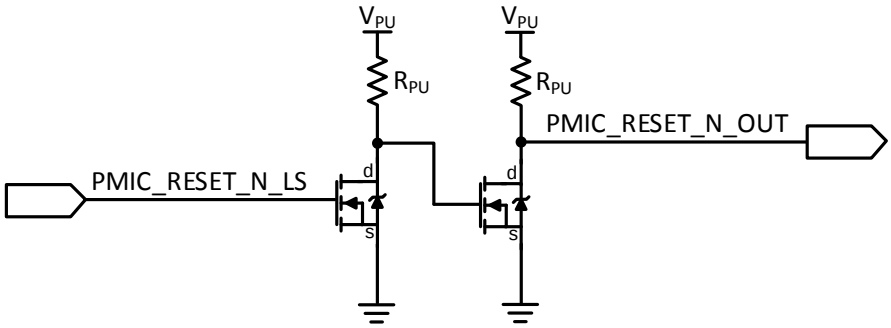
Refer to the Intel® Joule™ Module Datasheet for power button behaviors.

5.5 Control signal termination and conditioning

Additional buffering is needed for the PMIC_RESET_N_LS signal because the typical level translation does not use a strong enough pullup to 3.3 volts. The nFET transistor pairs have low Vts (part number DMN2400) operating at 1.5 V or 1.8 V levels, and offer the high-impedance level shifting requirement for this signal.

Table 7. Control signal level translation termination recommendations

Signal Name	Pullup Voltage	R_{min} Ω	CLOAD (pF)	T_{rise} (ns)	T_{fall} (ns)
PMIC_PWRGOOD_LS	3.3	2200	47	36800	19
PMIC_RESET_N_LS	Add a non-inverting buffer to the PMIC_RESET_N_LS signal				



Refer to Section 6.6 for a discussion of signal termination, how the values in the table were measured, and definitions of the values in the table. Refer to Figure 12 for an example pullup resistor for 3.3 V pullup voltage.

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6 Power Delivery Subsystem

6.1 Power delivery overview

All power sources for the Intel Joule expansion board are routed into a multiplexer device, U18.

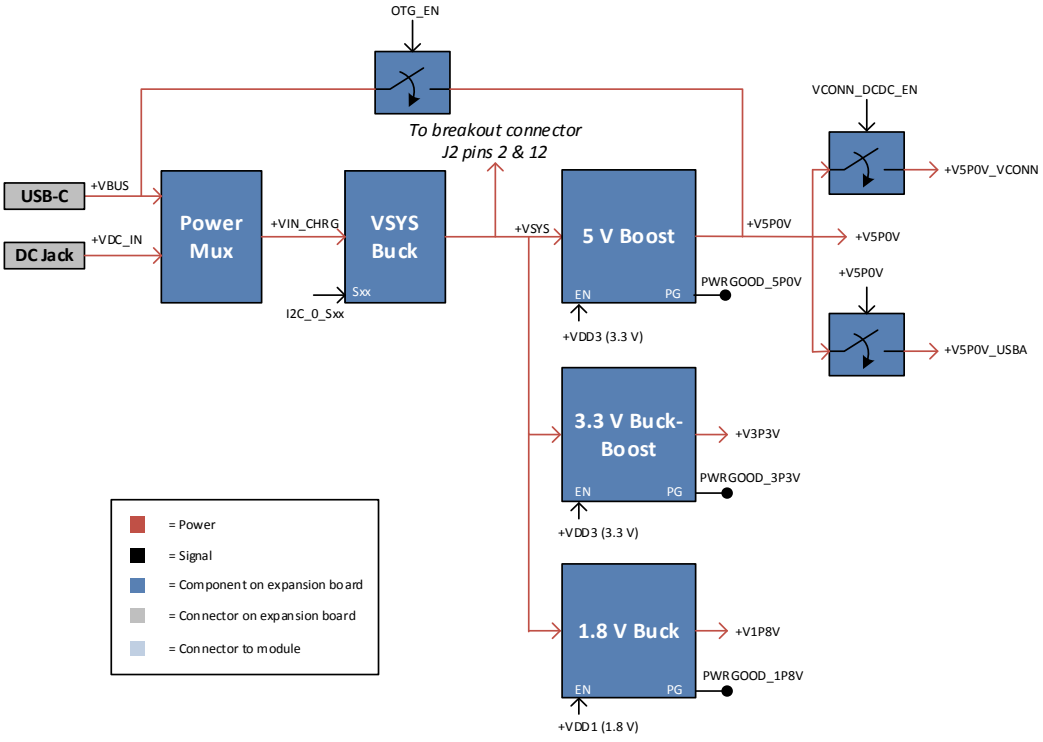
The power mux defaults to +VDC_IN when both +VDC_IN and +VBUS are present. Refer to the manufactures datasheet for input impedance, current limit details, and low voltage lock-out specifications.

When it is booted, it is not possible to switch between power input sources without rebooting the platform, because the power mux is a break-before-make connection.

The power mux passes the selected output onto the +VIN_CHRG bus, which is routed to the PMIC device, EU2. The battery management features of EU2 are not supported.

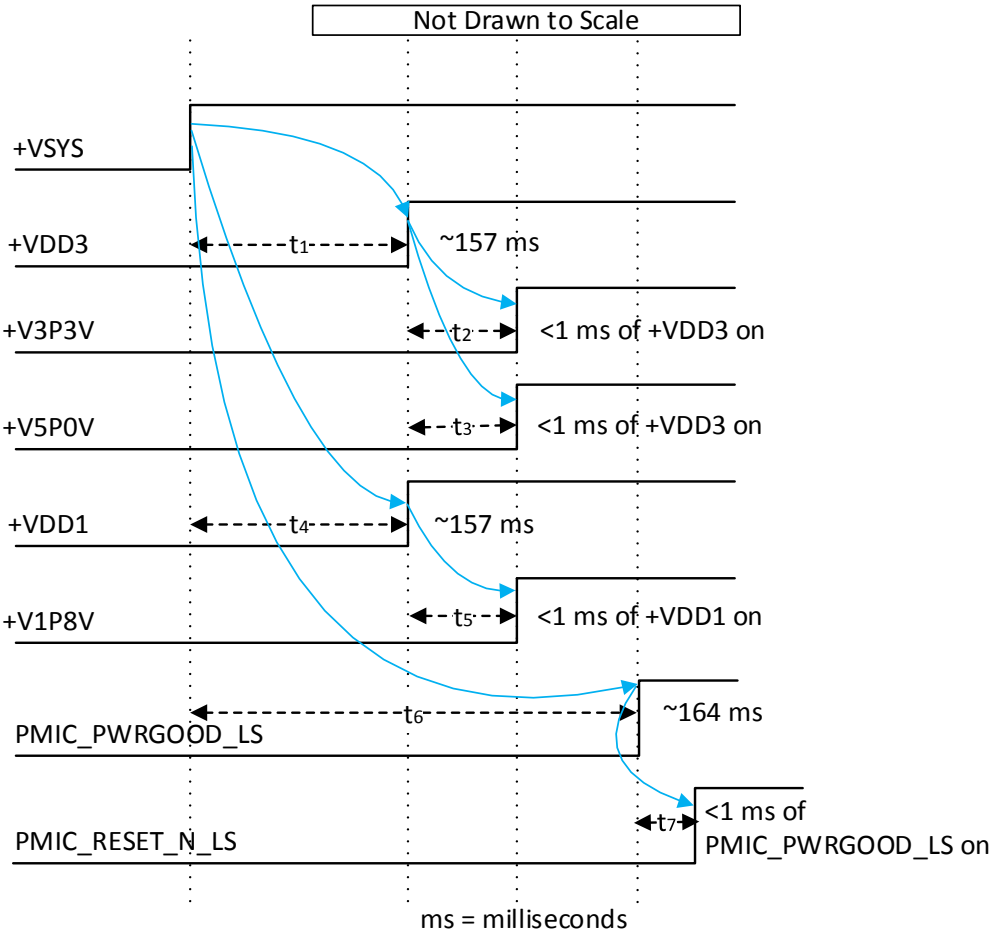
Voltage regulators and load switches on the expansion board provide the necessary supplies for various devices and interfaces of the board to function.

Figure 8. Expansion board power delivery block diagram



6.2 Power supply sequencing

Figure 9: Power on timing sequence (cold boot)



Once PMIC_PWRGOOD_LS goes high, PMIC_RESET_N_LS transitions high within 400 microseconds.

All rails are off within 2 milliseconds of a power off event.

Power up order of rails +VDD1 and +VDD3 is not guaranteed, but does not adversely affect operability.

6.3 Voltage regulators and load switches

6.3.1 +5 Boost regulator (U21)

The +5 volt boost regulator (a Fairchild* FAN48623 switching regulator) converts the +VSYS input supply to a +5 volt power rail, labelled +V5P0V. Refer to Table 9 for the maximum allowable current draw.

The +V5P0V power rail supplies power to:

- Micro-HDMI* connector
- USB load switches and the micro-USB Type-B debug port
- Breakout connector J13 and the fan header

Note: The +5-volt boost regulator does not start ramping up until the +VDD3 supply from the module connector (J2 pin 30) reaches a minimum of 1.575 V and +VSYS reaches at least 2.2 V.

6.3.2 +3.3 Boost regulator (U27)

The +3.3 volt buck/boost regulator (a Texas Instruments* TPS63021 switching regulator) converts the +VSYS input to a +3.3 volt power rail labelled +V3P3V. Refer to Table 9 for the maximum allowable current draw.

The +V3P3V power rail supplies power to:

- USB Type-C Mux
- Micro-SD card interface level shifter and connector
- HDMI and UART debug interface level shifters
- Intel Joule module connector level shifters
- Breakout connector J13 and the fan header

Note: The +3.3 volt buck/boost regulator does not start ramping up until the +VSYS supply reaches at least 1.8 V and the +VDD3 supply from the module connector reaches a minimum of 1.2 V.

6.3.3 +1.8 Buck regulator (EU5)

The +1.8 volt buck regulator (a Texas Instruments* TLV62084 switching regulator) converts the +VSYS input supply to a +1.8 volt power rail labelled +V1P8V. Refer to Table 9 for the maximum allowable current draw.

The +V1P8V power rail supplies power to:

- Micro-SD card interface level shifter and connector
- HDMI and UART debug interface level shifters
- Intel Joule module connector level shifters
- Breakout connector J13

Note: The +1.8 volt buck regulator does not start ramping until the +VDD1 supply from the module connector reaches a minimum of 1.0 V and +VSYS reaches at least 2.7 V.

6.3.4 USB load switches (U17 and EU3)

There are two USB load switches (a Fairchild* FPF2495UCX and a Texas Instruments* TPS2553DRVT) that control the delivery of the +V5P0V supply to the USB Type-C Configuration Channel (CC) lines for the module, and the USB Type-C and USB Type-A connectors.

6.3.5 Module sourced power supplies (+VDD1 and +VDD3)

The module provides two power rails, each limited to 300 mA, to expansion board J12.

The +VDD1 supply:

- Provides signal to enable the +1.8-volt buck regulator
- Enables pullup signals for the DnX and general purpose buttons and the EEPROM I2C interface

The +VDD3 supply:

- Enables +5 volt boost regulator and the +3.3 volt buck/boost regulator

The +VDD1 and +VDD3 are routed to the expansion board breakout connectors where they can be used to power other circuitry.

Caution: Ensure that breakout connector loads do not cause power supplies to be overloaded.

6.3.6 Module sourced power supplies

Table 8. Power supplies electrical specifications

Source	Item	Min	Typ	Max	Units	Max mA
VDD1	+VDD1	1.71	1.8	1.89	V	300
VDD3	+VDD3	3.15	3.3	3.45	V	300

Note: Do not exceed specified current limits; ensure that all device loads are accounted for.

6.4 RTC Backup battery

The expansion board supports a CR1225 coin cell backup battery. This backup battery is connected directly to the module and powers the module's time management unit's data, configuration, status registers, and timekeeping logic in the case of power loss.

Note: If the Intel Joule expansion board is removed from power (for instance, if no power is provided from the DC power jack or the USB Type-C connector) for an extended period of time, the back-up battery may drain to below the minimum operating voltage, with the result that the data stored in the Intel Joule module PMIC time management unit may become invalid.

6.5 Maximum current draw

Electrical specifications for each power source are as follows:

Table 9. Maximum current draw +V1P8V, +V3P3V, and +V5P0V

Source	Parameter	Min	Typical	Maximum	Units
+V1P8V	Voltage	1.71	1.8	1.89	V
	Current			1.8	A
+V3P3V	Voltage	3.135	3.3	3.465	V
	Current			1.4	A
+V5P0V	Voltage	4.75	5.0	5.25	V
	Current			1.0	A

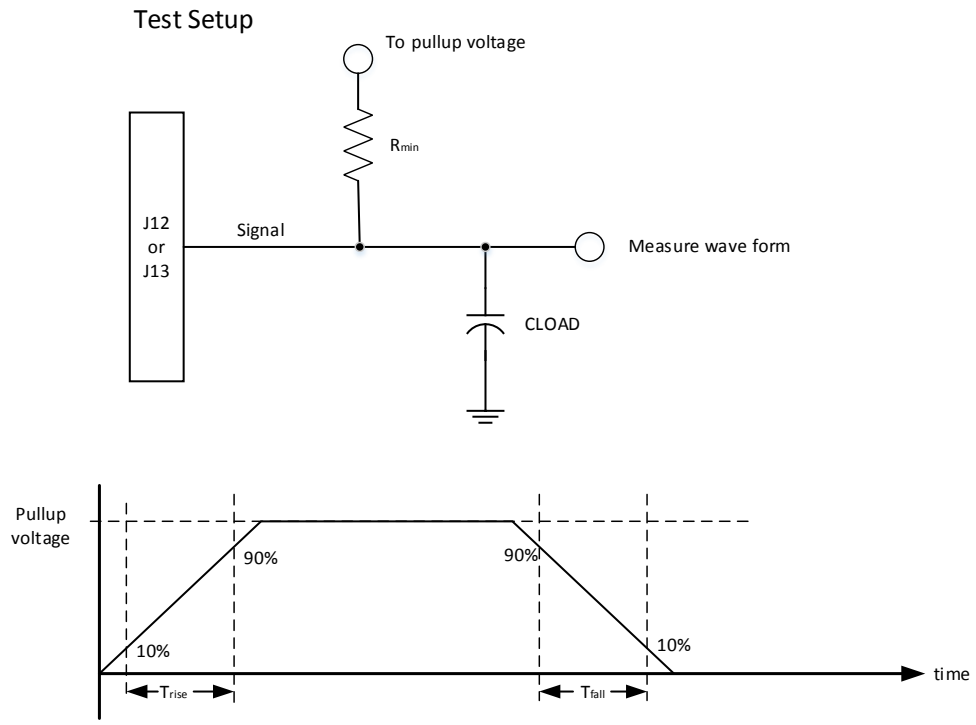
The total combined power for +V1P8V, +V3P3V and +V5P0V should not exceed .4.5 W given 12 V to VDCIN. This is assuming that the USB ports are not sourcing 900 mA to devices for OTG mode. If your use case requires full OTG current, then the OTG power should be subtracted from 4.5 W to find your new max power allowed to the IO breakout connectors. It is not recommended to operate both USB-C and USB-A ports at full OTG current loading simultaneously.

6.6 Termination and conditioning

You must terminate a signal so that the line doesn't float. For example, when data lines transitions from logic low to logic high, the level shifter opens similar to an open switch. The pullup resistor pulls the voltage up to logic high so that the signal can continue. Tables throughout this document provide the size of the pullup resistor you need for each signal.

The following diagram shows how the values in the tables were measured and what each value means, and an example table.

Figure 10: Test setup to determine the termination and conditioning values



T_{rise} is the rise time from 10% to 90% of pullup voltage, unless otherwise noted in the table.
T_{fall} is the fall time from 90% to 10% of pullup voltage, unless otherwise noted in the table.

Example table

Signal Name	Pullup Voltage	R_{min} Ω	CLOAD (pF)	T_{rise} (ns)	T_{fall} (ns)
PMIC_PWRGOOD_LS	3.3	2200	47	36800	19

The values in the table present the rise and fall times for a particular capacitive loading. You need to calculate the maximum frequency and values for Vol, Voh, Vil, Vih, Iol, Ioh based on the capacitive loading of your particular design.

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7 Clocks

The Intel Joule expansion board provides two clock signals on the breakout connectors, a 19.2 MHz clock and a 32.768 kHz real time clock (RTC). The following two sections provide the AC and DC specifications for both of these clock signals.

7.1 19.2 MHz system clock

The 19.2 MHz system clock is sourced from the Intel Joule module and is routed through a LSF0108 level shifter before routing to the break out connector. Due to the high frequency of this clock, it is recommended to not level shift this signal to 3.3 V, but instead place a weak pullup to the +V1P8V supply. The system clock is on J12 on pin 5.

Table 10. 19.2 MHz clock DC specifications

Parameter	Min	Typ	Max	Units	Conditions	Notes
V_{OH}	1.44			V	At R_{PULLUP}(min)	
V_{OL}			0.45	V	At R_{PULLUP}(min)	
I_{SOURCE}			1.5	mA		
I_{SINK}			1.5	mA		
R_{PULLUP}	1.2			kΩ	To +VDD1 supply	1

1. The resistance value of R_{PULLUP} must be equal to or greater than the minimum resistance value provided.

Table 11. 19.2 MHz clock AC specifications

Parameter	Min	Typ	Max	Units	Conditions	Notes
T_{RISE}	13		17	ns	20% to 80%	
T_{FALL}	13		17	ns	20% to 80%	
Frequency		19.2		MHz		
Duty Cycle	45	50	55	%		

Note: All AC measurements were made with R_{pullup} at 1.2 k and with 10 pF capacitive loading.

7.2 32.768 kHz real time clock

The 32.768 kHz real time clock (RTC) is sourced from the Intel Joule module and is routed through a LSF0108 level shifter before routing to the break out connector. The real time clock is at J13 on pin 39. A pullup resistor is required from pin 39 to the 3.3 V source. The following tables provide the DC and AC specifications for the 32.768 kHz RTC signal.

Table 12. RTC clock DC specifications (1.8 volt pullup)

Parameter	Min	Typ	Max	Units	Conditions	Notes
V_{OH}	V1P8V0-0.45			V		
V_{OL}			0.45	V		
R_{PULLUP}		1.1		kΩ	To +VDD1 supply	

Table 13. RTC clock AC specifications (1.8 volt pullup)

Parameter	Min	Typ	Max	Units	Conditions	Notes
T_{RISE}	1	5	25	ns	10% to 90%	
T_{FALL}	1	5	25	ns	10% to 90%	
Duty Cycle	40		60	%		
Jitter			±34	ppm	Cycle to Cycle	
Frequency		32.768		kHz		

Note: Capacitive loading during measurements was 47 pF

Table 14. RTC clock DC specifications (3.3 volt pullup)

Parameter	Min	Typ	Max	Units	Conditions	Notes
V_{OH}	+V3P3V-0.45			V	At R_{PULLUP}(max)	
V_{OL}			0.45	V	At R_{PULLUP}(min)	
R_{PULLUP}	1.5	2.2	4.9	kΩ	To +V3P3V supply	
I_{SOURCE}			3	mA		
I_{SINK}			3	mA		

Table 15. RTC clock AC specifications (3.3 volt pullup)

Parameter	Min	Typ	Max	Units	Conditions	Notes
T_{RISE}	47		60	ns	20% to 80%	
T_{FALL}	17		23	ns	20% to 80%	
Duty Cycle	40		60	%		
Jitter			±34	ppm	Cycle to Cycle	
Frequency		32.768		kHz		

Note: Capacitive loading during measurements was 47 pF.

7.3 Clock signal termination and conditioning

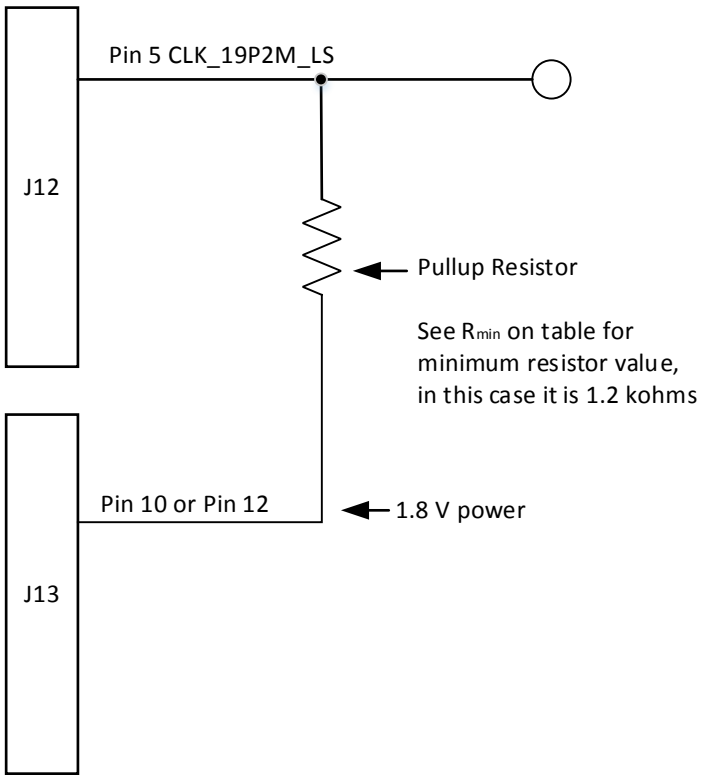
Table 16.Clock signal level translation termination recommendations

Signal Name	Pullup Voltage	R_{min} Ω	CLOAD (pF)	T_{rise} (ns)	T_{fall} (ns)
CLK_19P2M_LS	1.8	1200	10	16	15
CODEC_MCLK_LS	1.8	1200	10	16	15
PMIC_SLPCLK_1_LS	3.3	1100	47	54	20

7.3.1 Example using CLK_19P2M_LS signal

The following diagram shows how to use the information in the table to position a pullup resistor for the signal CLK_19P2M_LS. For information about how the values in the table were measured refer to Section 6.6.

Figure 11: Example pullup resistor for 1.8 V pullup voltage



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8 HDMI Subsystem

The HDMI subsystem provides a micro-HDMI* Type-D connector at J10 for connecting compliant displays and HDMI audio devices to the development platform. Refer to Figure 3 for the location of the HDMI connector.

The Intel Joule expansion board provides the required filtering and voltage level translation (shifting) between the module HDMI bus and the physical interface outputs.

Refer to the Parade* PS8203 datasheet for the HDMI interface signal specifications.

The required +5 volt power to the micro-HDMI connector is provided directly from the +5 volt boost regulator on the expansion board.

8.1 Micro-HDMI* (Type-D) connector pinout

Table 17. Micro-HDMI (type-D) connector pinout

Pin #	Net Name	Direction	Signal Description
1	HDMI_OP_HPD_INV	Input	Monitor or cable hot plug detect
2	N/C	No connect	No connect
3	HDMI_DAT2_CONN_DP	Output	Data lane 2, positive signal
4	GND	Ground	Ground
5	HDMI_DAT2_CONN_DN	Output	Data lane 2, negative signal
6	HDMI_DAT1_CONN_DP	Output	Data lane 1, positive signal
7	GND	Ground	Ground
8	HDMI_DAT1_CONN_DN	Output	Data lane 1, negative signal
9	HDMI_DAT0_CONN_DP	Output	Data lane 0, positive signal
10	GND	Ground	Ground
11	HDMI_DAT0_CONN_DN	Output	Data lane 0, negative signal
12	HDMI_CLK_CONN_DP	Output	Clock lane, positive signal
13	GND	Ground	Ground
14	HDMI_CLK_CONN_DN	Output	Clock lane, negative signal
15	N/C	No connect	No connect
16	GND	Ground	Ground
17	HDMI_OB_SCL	Output	I2C Clock
18	HDMI_OB_SDA	Bidirectional	I2C Data
19	+V5P0V_D	Output	+5-volt power to HDMI cable/sink device

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9 SD Card Subsystem

The expansion board contains a micro SD card slot at J5 attached to the bottom side. Refer to Figure 4 for the location of the SD card slot.

The SD card interface is sourced from the Intel Joule module and routed to an NXP IP4856CX25 level shifter. The level shifter allows for the support of both 1.8 volt and 2.9 volt cards. The output of the level shifter is routed directly to the micro SD card connector.

The micro SD card connector power is sourced from the +3.3 volt buck/boost regulator.

Refer to the micro SD card specifications for electrical and power requirements. Refer to the NXP IP4856CX25 datasheet for the SD card interface signal specifications. The power from the level shifter can support a maximum current of 100 mA and has a supply voltage of 2.9 V.

Table 18. Micro SD card connector pinout

Pin #	Net Name	Direction	Signal Description
1	SDCARD_D2_CONN	Bidirectional	Data lane 2
2	SDCARD_D3_CONN	Bidirectional	Data lane 3
3	SDCARD_CMD_CONN	Bidirectional	
4	+V3P3V_MICROSD	Output	+2.9 volt supply to SD card
5	SDCARD_CLK_CONN	Output	
6	GND	Ground	Ground
7	SDCARD_D0_CONN	Bidirectional	Data lane 0
8	SDCARD_D1_CONN	Bidirectional	Data lane 1

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10 GPIOs

The Intel Joule expansion board provides 8 dedicated GPIO lines and 7 additional GPIO lines at the breakout connectors; the first four GPIO lines (ISH_GPIO_0 through ISH_GPIO_3) are also connected to onboard LEDS that are activated when the line is HIGH from either the breakout source or the module. Refer to Figure 7 for the mapping of GPIO to LEDs.

All 15 GPIOs are level shifted by a by a Texas Instruments* LSF0108RKSR device and require pullups on the attached mezzanine cards to the end-user's desired voltage levels not to exceed 3.3 VDC. Level transition circuits for GPIO lines must be powered and stable before the module completes the cold boot routine.

The default pin usage refers to the vantage point of the breakout board. For example, the ISH_GPIO_0 signal originates in the breakout board and is delivered to the expansion board through the J12 connector; therefore ISH_GPIO_0 is an output (as configured by the BIOS).

Table 19. GPIO mapping table

Pin #	Signal Name	Default Breakout Usage	Signal Description
J12-1	GPIO_22	Input	GPIO Pin 14
J12-35	ISH_GPIO_0_LS	Output	GPIO Pin 0
J12-33	ISH_GPIO_1_LS	Output	GPIO Pin 1
J12-31	ISH_GPIO_2_LS	Output	GPIO Pin 2
J12-29	ISH_GPIO_3_LS	Output	GPIO Pin 3
J12-27	ISH_GPIO_4_LS	Output	GPIO Pin 4
J12-25	ISH_GPIO_5_LS	Output	GPIO Pin 5
J12-23	ISH_GPIO_6_LS	Output	GPIO Pin 6
J13-16	FLASH_TORCH	Output	GPIO Pin 7
J13-18	FLASH_RST_N	Output	GPIO Pin 8
J13-20	FLASH_TRIGGER	Output	GPIO Pin 9
J13-34	ISH_UART_0_TXD	Output	GPIO Pin 10
J13-36	ISH_UART_0_RXD	Output	GPIO Pin 11
J13-38	ISH_UART_0_RTS	Output	GPIO Pin 12
J13-40	ISH_UART_0_CTS	Input	GPIO Pin 13

Note: During BIOS execution, the ISH_GPIO_0 through ISH_GPIO_3 signals are configured as outputs and change state to indicate BIOS progression.

10.1 GPIO signal termination and conditioning

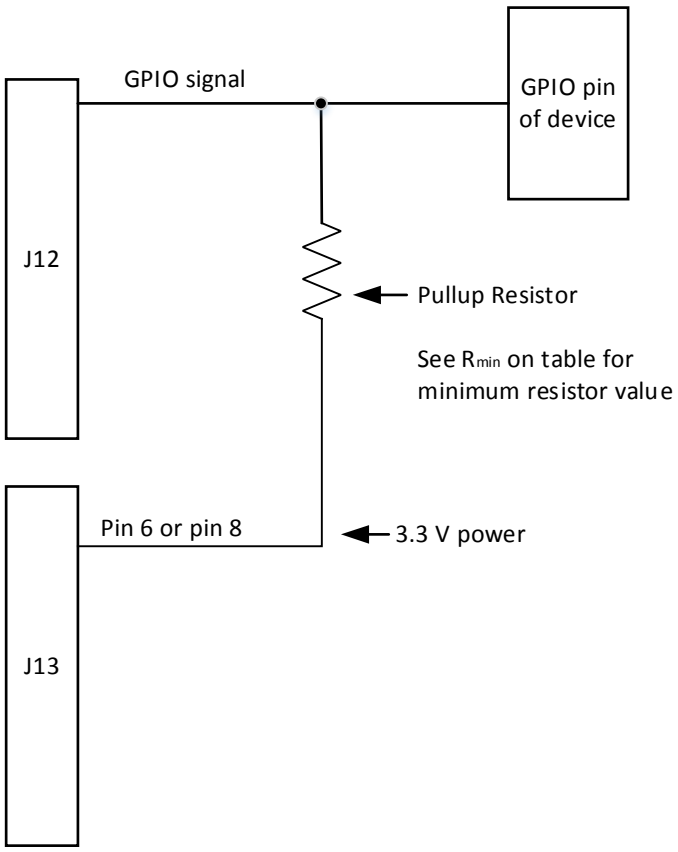
Table 20. GPIO signal level translation termination recommendations

Signal Name	Pullup Voltage	R_{min} Ω	CLOAD (pF)	T_{rise} (ns)	T_{fall} (ns)
FLASH_RST_N_LS	3.3	2200	47	138	35
FLASH_TORCH_LS					
FLASH_TRIGGER_LS					
GPIO_22_LS	3.3	2400	47	100	7.4
ISH_GPIO_0_LS	3.3	2200	47	162	35
ISH_GPIO_1_LS					
ISH_GPIO_2_LS					
ISH_GPIO_3_LS					
ISH_GPIO_4_LS					
ISH_GPIO_5_LS					
ISH_GPIO_6_LS					
ISH_UART_0_CTS_LS	3.3	2200	47	140	35
ISH_UART_0_RTS_LS					
ISH_UART_0_RXD_LS					
ISH_UART_0_TXD_LS					

10.1.1 Example using GPIO signal

The following diagram shows how to use the information in the table to position a pullup resistor for a GPIO signal For information about how the values in the table were measured refer to Section 6.6.

Figure 12. Example pullup resistor on a 3.3 voltage



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11 I2S Interface

The Intel Joule expansion board provides one I2S port at the breakout connector to enable the connection of audio-based devices.

Table 21. I2S Mapping to breakout connectors

Pin #	Signal Name	Direction Looking into Breakout Connector	Signal Description
J12-12	I2S_1_RXD_LS	Input	Audio data input to the expansion board, from an I2S compliant audio input device on the breakout board.
J12-14	I2S_1_TXD_LS	Output	Audio data output to an I2S compliant audio output device on the breakout board.
J12-16	I2S_1_FS_LS	Output	Audio left/right frame select signal to an I2S compliant audio device on the breakout board.
J12-18	I2S_1_CLK_LS	Input/Output	Audio bit clock output/input to an I2S compliant audio device on the breakout board.

Note: Direction can change for slave or master mode.

11.1 I2S level transitions

The breakout board must include pullup resistors to the logic levels required by the audio device on the breakout board, but not to exceed 3.3 V. The pullups are from the I2S signals to a 3.3 V source. We recommend using J13 pin 6 or 8 as the 3.3 V source for the pullup resistors.

Level translation is performed by a Texas Instruments* LSF0108RKSR open drain translator.

The expansion board uses a 200 kΩ pullup resistor from the +V3P3V supply to enable EU17 when the expansion board is active.

See the Intel® Joule™ Module Datasheet for I2S technical specifications.

11.2 Audio signal termination and conditioning

For information about signal termination and conditioning, definitions of the values in the following table, and how the values were measured, refer to Section 6.6. For an example of how to wire a pullup resistor for a 3.3 V pullup voltage, refer to Figure 12.

Table 22. SPI signal level translation termination recommendations

Signal Name	Pullup Voltage	R_{min} Ω	CLOAD (pF)	T_{rise} (ns)	T_{fall} (ns)
I2S_1_CLK_LS	3.3	1100	47	56	17
I2S_1_FS_LS					
I2S_1_RXD_LS					
I2S_1_TXD_LS					

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12 DMIC Interface

The Intel Joule module support microphones that use the PDM digital microphone standard attached through the AVS_M interface. Two microphones can share one data line by using time domain multiplexing to the two slots.

PDM microphones are enabled and disabled by the clock signal. Absence of clock signal will switch microphone to sleep mode, which can be utilized in system power management.

Additionally, the microphones can be power-gated to cut power consumption to zero when the microphones are not in use.

Refer to the Intel® Joule™ Module Datasheet for additional information.

12.1 DMIC signal termination and conditioning

For information about signal termination and conditioning, definitions of the values in the following table, and how the values were measured, refer to Section 6.6. For an example of how to wire a pullup resistor for a 3.3 V pullup voltage, refer to Figure 12.

Table 23. DMIC signal level translation termination recommendations

Signal Name	Pullup Voltage	R_{min} Ω	CLOAD (pF)	T_{rise} (ns)	T_{fall} (ns)
AVS_M_CLK_A1_LS	3.3	1100	47	184	17
AVS_M_CLK_B1_LS					
AVS_M_DATA_1_LS					

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13 SPI interface

The Intel Joule expansion board routes two SPI interfaces from the module, through a level translator to convert the module 1.8 V logic levels to those required by the breakout board. The breakout board should include appropriate pullup values to the desired voltage, but not to exceed 3.3 V.

Table 24. SPI mapping to breakout connectors

Pin #	Signal Name	Direction at Breakout Connector	Signal Description
J13-25	SPI_0_CLK_LS	Input	SPI port 0 Clock
J13-19	SPI_0_FS0_LS	Input	SPI port 0 slave select 0
J13-21	SPI_0_FS1_LS	Output	SPI port 0 chip select 1
J13-23	SPI_0_FS2_LS	Output	SPI port 0 chip select 2
J13-29	SPI_0_MISO_LS	Output	SPI port 0 receive data
J13-27	SPI_0_MOSI_LS	Input	SPI port 0 transmit data
J12-10	SPI_1_CLK_LS	Output	SPI port 1 Clock
J12-6	SPI_1_FS0_LS	Output	SPI port 1 slave select 0
J12-8	SPI_1_FS2_LS	Output	SPI port 1 slave select 2, hardware strap with disable boot from SD card functionality
J12-2	SPI_1_MISO_LS	Input	SPI port 1 receive data
J12-4	SPI_1_MOSI_LS	Output	SPI port 1 transmit data

13.1 SPI level transitions

All of the SPI interface lines are level transitioned (shifted) between the breakout connector 3.3 VDC levels and the Intel Joule compute module, which operates at 1.8 VDC levels.

Level translation is performed by a Texas Instruments* LSF0108RKSR open drain translator.

The expansion board uses a 200 kΩ pullup resistor from the +V3P3V supply to enable EU17 when the expansion board is active.

13.2 SPI strapping for SD card boot

To force the expansion board to boot from SD card, the FS2 signal of SPI port 1 is pulled low by strapping J14 Pin 2 and 4.

Additional boot-mode configuration by hardware strapping is covered in Section 3.2.

13.3 SPI signal termination and conditioning

For information about signal termination and conditioning, definitions of the values in the following table, and how the values were measured, refer to Section 6.6. For an example of how to wire a pullup resistor for a 3.3 V pullup voltage, refer to Figure 12.

Table 25. SPI signal level translation termination recommendations

Signal Name	Pullup Voltage	R_{min} Ω	CLOAD (pF)	T_{rise} (ns)	T_{fall} (ns)
SPI_0_CLK_LS	3.3	1100	22	33	17
SPI_0_FS0_LS					
SPI_0_FS1_LS					
SPI_0_FS2_LS					
SPI_0_MISO_LS					
SPI_0_MOSI_LS					
SPI_1_CLK_LS					
SPI_1_FS0_LS					
SPI_1_FS2_LS					
SPI_1_MISO_LS					
SPI_1_MOSI_LS					

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14 UART Interfaces

The Intel Joule expansion board exposes two UART ports, UART_0 and UART_1, at the breakout connectors for peripheral device communications and system development activities.

Table 26. UART mapping to breakout connectors

Pin #	Signal Name	Direction	Signal Description
J13-32	UART_0_CTS_LS	Input	UART port 0 clear-to-send
J13-30	UART_0_RTS_LS	Output	UART port 0 ready-to-send
J13-28	UART_0_RXD_LS	Input	UART port 0 receive data
J12-7	UART_0_TXD_LS	Output	UART port 0 transmit data
J12-24	UART_1_RXD_LS	Input	UART port 1 receive data
J12-22	UART_1_TXD_LS	Output	UART port 1 transmit data, and hardware strap. Refer to Section 3.2 for strapping information.

The UART controllers are integrated into the module. Consult the Intel® Joule™ Module Datasheet for specific modes of operation.

UART2 of the module is dedicated to serial debug port J9 on the expansion board. See the debug and troubleshooting Section19 for more information on UART2 usage.

14.1 UART level translation on the expansion board

Level translation (shifting) of the UART signals from the module native 1.8 VDC level to the expansion board is accomplished using the Texas Instruments* (TI) LSF0108RKSR device; the same device is used for other level translation activities on the expansion board. The expansion board should include appropriate pullup values to the desired voltage, but not to exceed 3.3 V.

14.2 UART Signal Termination and Conditioning

For information about signal termination and conditioning, definitions of the values in the following table, and how the values were measured, refer to Section 6.6. For an example of how to wire a pullup resistor for a 3.3 V pullup voltage, refer to Figure 12.

Table 27. UART signal level translation termination recommendations

Signal Name	Pullup Voltage	Rmin Ω	CLOAD (pF)	Trise (ns)	Tfall (ns)
UART_0_CTS_LS	3.3	2400	47	36	33
UART_0_RTS_LS					
UART_0_RXD_LS					
UART_0_TXD_LS					
UART_1_RXD_LS					
UART_1_TXD_LS					

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15 USB Subsystem

The Intel Joule expansion board has three physical USB connectors:

- J7 – USB 3.0; Type-C connector
- J6 – USB 3.0, Type A connector for a hub or single input device
- J9 – Micro USB connector dedicated to serial debug. See Section 19.1.

Refer to Figure 3 for the locations of these connectors.

See Section 5.2 for options to use USB Type-C to power the expansion board.

Table 28. USB type-C connector pinout

Pin #	Net Name	Direction	Signal Description
A1	GND	Ground	Ground
A2	USBC_USB3_0_MUX1_TX_DP	Output	USB 3.0 data transmit positive, from USB 3.0 2:1 mux
A3	USBC_USB3_0_MUX1_TX_DN	Output	USB 3.0 data transmit negative, from USB 3.0 2:1 mux
A4	+VBUS_USBC	Bidirectional	USB Type-C VBUS power source or sink
A5	USB_TYPC_CONN_CC1		USB type-C configuration channel 1
A6	USBC_USB2_0_DP	Bidirectional	USB 2.0 data positive
A7	USBC_USB2_0_DN	Bidirectional	USB 2.0 data negative
A8	N/C	No Connect	No connect
A9	+VBUS_USBC	Bidirectional	USB Type-C VBUS power source or sink
A10	USBC_USB3_0_MUX2_RX_DN	Input	USB 3.0 data receive negative, from USB 3.0 2:1 mux
A11	USBC_USB3_0_MUX2_RX_DP	Input	USB 3.0 data receive positive, from USB 3.0 2:1 mux
A12	GND	Ground	Ground
B1	GND	Ground	Ground
B2	USBC_USB3_0_MUX2_TX_DP	Output	USB 3.0 data transmit positive, from USB 3.0 2:1 mux
B3	USBC_USB3_0_MUX2_TX_DN	Output	USB 3.0 data transmit negative, from USB 3.0 2:1 mux
B4	+VBUS_USBC	Bidirectional	USB Type-C VBUS power source or sink
B5	USB_TYPC_CONN_CC2		USB Type-C configuration channel 2

Pin #	Net Name	Direction	Signal Description
B6	USBC_USB2_0_DP	Bidirectional	Bidirectional
B7	USBC_USB2_0_DN	Bidirectional	Bidirectional
B8	N/C	No Connect	No connect
B9	+VBUS_USBC	Bidirectional	USB Type-C VBUS power source or sink
B10	USBC_USB3_0_MUX1_RX_DN	Input	USB 3.0 data receive negative, from USB 3.0 2:1 mux
B11	USBC_USB3_0_MUX1_RX_DP	Input	USB 3.0 data receive positive, from USB 3.0 2:1 mux
B12	GND	Ground	Ground

15.1 USB Type-C with OTG (J7)

The USB Type-C port provides the following functionality:

- USB 3.0 and USB 2.0 interfaces
- Supports inverted connector insertion by auto multiplexing of USB 3.0 lanes
- Input for power source for expansion board; see Section 5.2.
- Power output of up to 900 mA for OTG device
- Powered Configuration Channel (CC) lines (+5VDC levels up to 300 mA, each)

The USB Type-C connector VBUS pin can either act as a power input to the expansion board or power output from the expansion board. The default mode is using the USB Type-C connector as a power input. However, when software executing on the module detects that the port must switch to OTG mode, a load switch is enabled, which supplies power from the +5 volt boost regulator to the VBUS pin of the USB Type-C connector, through the +VBUS rail of the expansion board.

USB loads that exceed 900 mA limit can have unpredictable behavior. Device load on the Type-C connector is to be considered in total platform power needs when selecting power supply solutions.

15.1.1 USB Type-C inverted cable mux (EU4)

The expansion board provides a USB multiplexer device to that is configured to detect and correct inverted cable configurations. Actual determination of cable inversion is performed by the module, activating USBC_SEC to control the mux as needed.

15.3 USB 3.0 Type-A (J6)

The USB 3.0 Type-A port supports both USB 3.0 and USB 2.0 speeds on connector J6.

J6 also provides a 5 VDC level on the VBUS pin that can source up to 900 mA by passing through the current limiting load switch EU3. USB loads that exceed the 900 mA limit can have unpredictable behavior. Device load on the Type-A connector is to be considered in total platform power needs when selecting power supply solutions.

Table 29. USB 3.0 type-A connector pinout

Pin #	Net Name	Direction	Signal Description
1	+V5P0V_USBA	Output	VBUS power
2	USBA_USB2_1_DN	Bidirectional	USB 2.0 data negative
3	USBA_USB1_1_DP	Bidirectional	USB 2.0 data positive
4	GND	Ground	Power return ground
5	USBA_USB3_1_RX_DN	Input	USB 3.0 data receive negative
6	USBA_USB3_1_RX_DP	Input	USB 3.0 data receive positive
7	GND	Ground	Signal return ground
8	USBA_USB3_1_TX_DN	Output	USB 3.0 data transmit negative
9	USBA_USB3_1_TX_DP	Output	USB 3.0 data transmit positive

15.4 USB electrical characteristics

The USB sub-system supports one DRD (dual-role device)/OTG (on-the-go) port, which uses separate host controller (xHCI) and device controller (xDCI) IPs. As a host, it can connect to any standard USB 1.1, 2.0, or 3.0 device. As a device, it can connect to any host and can expose various SoC capabilities based on what drivers are available. The USB interface has the following features:

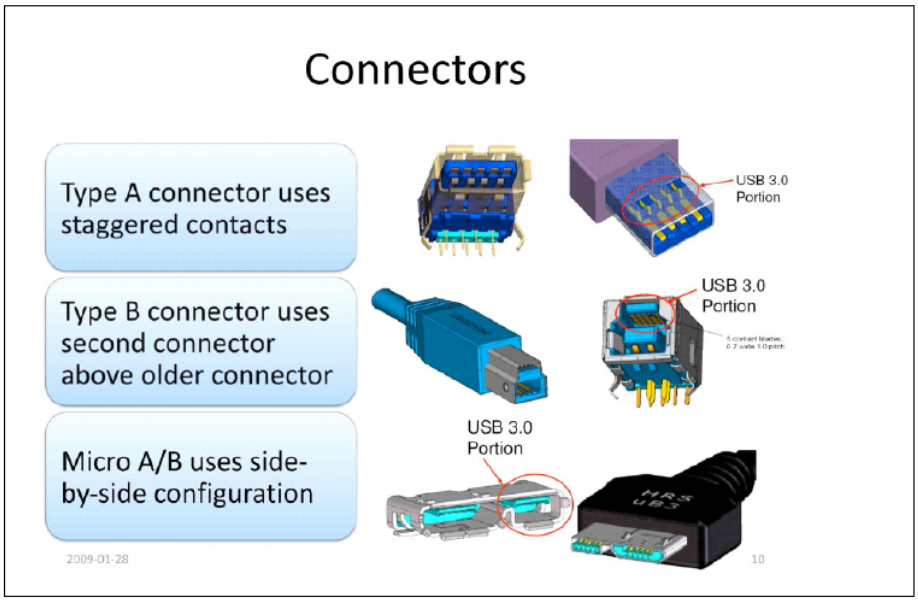
- USB 3.0 – one host only, and one OTG (host or device)
- Max USB 3.0 Speed – 5 Gb/s
- USB 2.0 – two host only, and one OTG
- Max USB 2.0 Speed – 480 Mb/s

Refer to the Intel® Joule™ Datasheet additional specifications of the USB controller.

15.4.1 USB Controllers

The USB subsystem incorporates the xHCI Host Controller, and USB 3.0 Controller configured as a USB Device only (xDCI).

Figure 13: USB connector types



A typical platform is expected to use a micro-AB connector on the OTG port.

Table 30. USB connect or disconnect scheme – connector dependent

Receptacle	Plug	Way of Detection	Action
Micro-AB on OTG only	Micro-A	ID pin pulled to GND (PMIC)	OTG start as Host (selected by software)
Micro-AB on OTG only	Micro-B	VBUS sensing (PMIC)	OTG start as device (selected by software)

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16 Pulse Width Modulators

The default BIOS configuration table defines four dedicated PWM outputs as PWM_0 through PWM_3 with programmable frequency and duty cycle.

All of the PWM signals are level transitioned (shifted) from 1.8 VDC to breakout board voltage levels by pullup resistors on the breakout board. Level translation is perform by a Texas Instruments* LSF0108RKSR open drain translator. The expansion board uses a 200 kΩ pullup resistor from the +V3P3V supply to enable EU17 when the expansion board is active.

Refer to the Intel® Joule™ Module Datasheet for additional details.

16.1 PWM signal termination and conditioning

For information about signal termination and conditioning, definitions of the values in the following table, and how the values were measured, refer to Section 6.6. For an example of how to wire a pullup resistor for a 3.3 V pullup voltage, refer to Figure 12.

Table 31. PWM signal level translation termination recommendations

Signal Name	Pullup Voltage	R_{min} Ω	CLOAD (pF)	T_{rise} (ns)	T_{fall} (ns)
PWM_0_LS	3.3	2200	47	134	35
PWM_1_LS					
PWM_2_LS					
PWM_3_LS					

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17 Configuration EEPROM

The Intel Joule expansion board contains a programmable EEPROM that can be used to identify the expansion board to the Intel Joule module, and to configure the module GPIO signals to the specific requirements of the expansion board.

The EEPROM includes board and manufacturer information, IDs for non-discoverable devices, modified GPIO, and interface bus configurations.

The EEPROM configuration tool is still under development and currently only the reference configurations are available.

Note: If the module determines that the expansion board EEPROM is not present or its contents are corrupted, then the BIOS executing on the module configures the module signals to the BIOS default configuration, as described in the Intel® Joule™ Module Datasheet.

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18 Mechanical and Environmental

18.1 Mechanical dimensions

The following figures provide pertinent dimensional information for the Intel Joule expansion board for reference only. This information can change at any time.

Refer to the Intel® Joule™ Development Kit Mechanical Descriptor for current information.

Figure 14. Expansion board key dimensions – top view

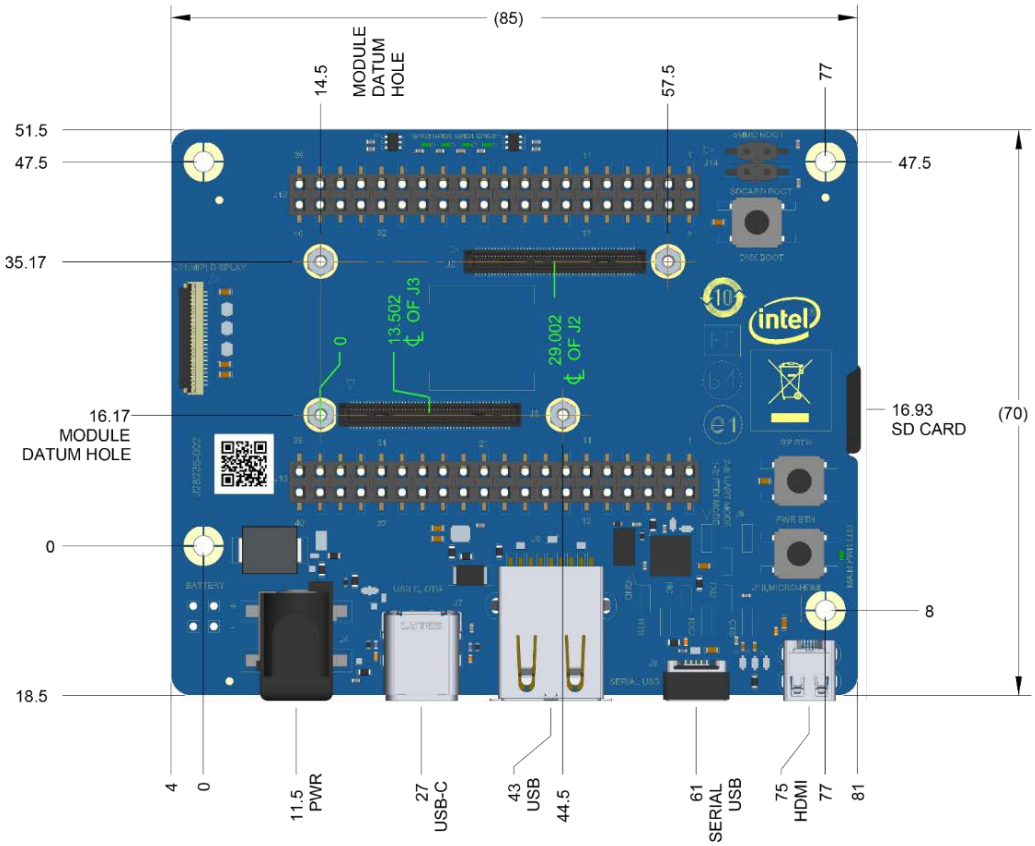
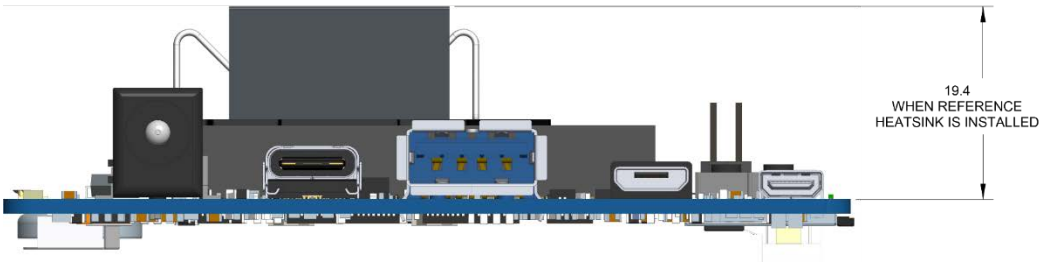


Figure 15. Expansion board key dimensions – side view



18.2 Operating electrostatic discharge (ESD)

Electrostatic discharge tolerance is specified at ±4 kV on all interface connectors.

18.3 Temperature range

The expansion board is rated from 32˚ to 158 ˚Fahrenheit (0˚ to 70˚ Celsius).

18.4 Cooling fan (J17)

The expansion board provides a three-pin fan connector (J17) which is located on the bottom side of the board. The connector provides a +5 volt (+V5P0V) supply.

Refer to the Intel® Joule™ Developer Kit Thermal Overview for related information.

Table 32. Fan connector pin assignments

Pin #	Net Name	Direction	Signal Description
1	+V5P0V	Output	+5 volt supply to fan assembly
2	Reserved – No connect	No connect	No connect - Reserved for future use
3	GND	Ground	Ground

18.5 Thermal profiling and enclosures

See the Thermal Overview for the Intel Joule Developer Kit for guidance on measuring application workload and selecting an appropriate cooling solution.

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19 Debug and Troubleshooting

The Intel Joule expansion board provides a single “serial over USB” debug port that is intended to capture boot time flow and provide a command console to the module.

Although an inspection of the schematic shows component locations to support a high-speed UART debug port, high-speed UART functionality is not enabled.

19.1 Serial debug port (J9)

The debug port is mapped from the module to the expansion board as a standard Type-B interface; data lines are routed through an active ESD filter (U24) in route to a USB to UART translation device (EU6).

Expansion board reference designator EU6 is a FTDI* FT232RQ USB UART device. This device translates the 5 VDC USB communications into a 3.3 VDC UART protocol and also enables self-powered (from the expansion board +V5P0V boost regulator) or bus-powered operation when powered from the micro-USB Type-C connector.

After the USB debug information is translated to the 3.3 VDC UART protocol, it is further shifted from 3.3 VDC to 1.8 VDC by the EU14 before reaching the module.

See the Intel® Joule™ Module Developers Kit Users Guide for details about configuring a workstation to communicate with the development kit over the serial debug port (SDP).

19.2 Troubleshooting

Guidance for troubleshooting can be found in the Intel® Joule™ Module Developers Kit Users Guide. Additional help can be found in the Troubleshooting and FAQ – Using the Intel® Joule™ development platform. Refer to Section 1.3 for the location of each of these documents.

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