

U1A

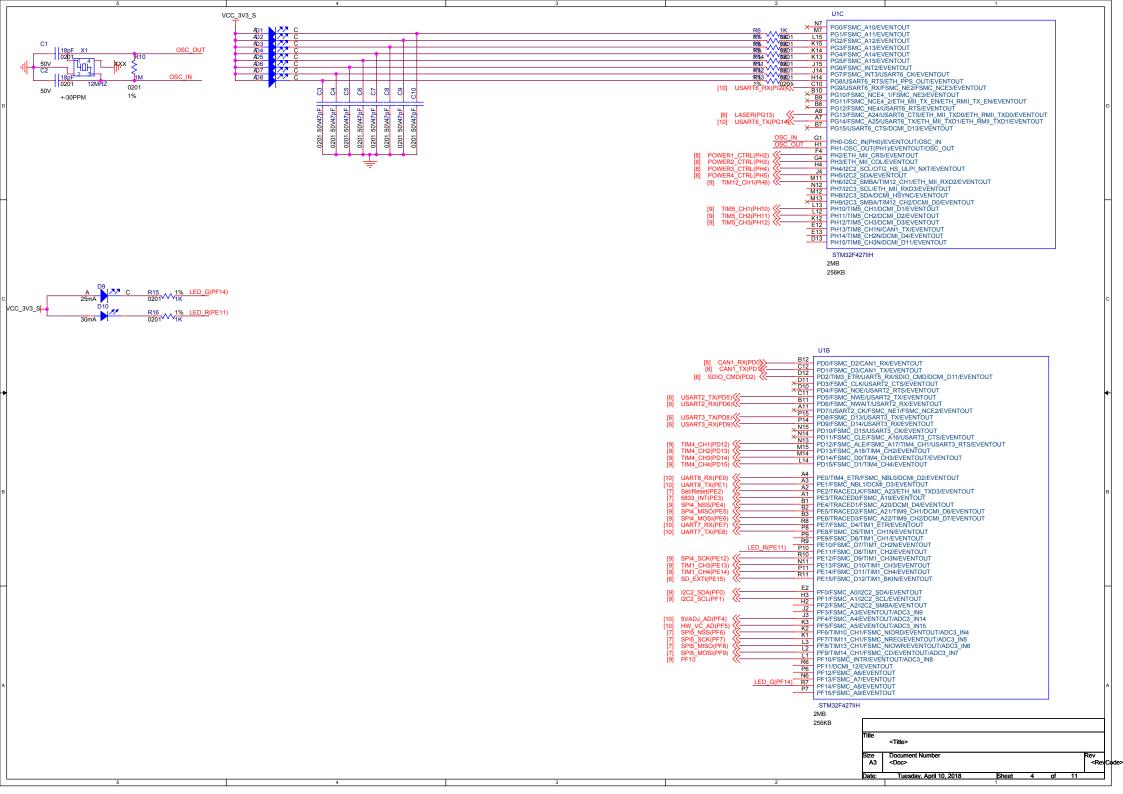
	TIM2_CH(PA0)	PAO_WKUP/USART2_CTS/UART4_TX/ETH_MIL_CRS/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR/EVENTOUT/ADC123_INOWKUP PA/IUSART2_TS/JUART4_TX/ETH_MIL_REF_CLK/ETH_MIL_RC_CK/ITM5_CH2/TIM2_CH2/EVENTOUT/ADC123_IN02 PA/IUSART2_TX/TIM5_CH4/TIM5_CH4/TIM2_CH4/ETH_MID/OVENTOUT/ADC123_IN12 PA/IUSART2_TX/TIM5_CH4/TIM5_CH4/TIM2_CH4/ETH_MID/OVENTOUT/ADC123_IN13 PA/ISPI1_NSS/SPI3_NSS/USART2_CK/DCM_HSYNC/OTG_HS_SOF/IZS3_WS/EVENTOUT/ADC12_IN4/DAC_OUT1 PA/ISPI1_NSS/SPI3_NSS/USART2_CK/DCM_HSYNC/OTG_HS_SOF/IZS3_WS/EVENTOUT/ADC12_IN4/DAC_OUT1 PA/ISPI1_MSO/TIM8_BKIN/TIM13_CH4/DCM_PIXCLK/TIM3_CH1/TIM1_BKIN/EVENTOUT/ADC12_IN6 PA/ISPI1_MSO/TIM8_BKIN/TIM13_CH2/ETH_MIL_RC_XDV/ITM1M1_CH1/INFAULT/ADC12_IN6 PA/ISPI1_MSO/TIM8_BKIN/TIM14_CH1/ING_CK1/ETH_MIL_RC_XDV/ITM1M1_CH1/INFAULT/ADC12_IN6 PA/ISPI1_MSO/TIM8_CH1/INFAULT/ADC12_IN7 PA/ISPI1_MSO/TIM8_CH2/ETH_MIL_RC_XDV/ITM1M1_CH1/INFAULT/ADC12_IN7 PA/ISPI1_MSO/TIM8_CH1/INFAULT/ADC12_INFAULT/ADC13_INFAULT/A
[9] [9] [9] [6] [7] [7] [6] [8] [8] [8]	ADC1_IN8(PB0)	PB0/TIM3_CH3/TIM8_CH2N/OTG_HS_ULPI_D1/ETH_MII_RXD2/TIM1_CH2N/EVENTOUT/ADC12_IN8 PB1/TIM3_CH4/TIM8_CH3N/OTG_HS_ULPI_D2/ETH_MII_RXD3/OTG_HS_INTN/IIM1_CH3N/EVENTOUT/ADC12_IN9 PB2/PB2_B00/TI/EVENTOUT PB3/JTD0/TRACES/WO/STD13_SCK/12S3_CK/ITM2_CH2/SPI1_SCK/EVENTOUT PB3/JTD0/TRACES/WO/STD1/STS/SPI3_SCK/12S3_CK/ITM2_CH2/SPI1_SCK/EVENTOUT PB3/JTD0/TRACES/WO/STD1/STS/SPI3_MSO/TIM3_CH3/SPI1_MSO/IXS3_SM_SEVENTOUT PB3/JTD1/TRACES/WO/STD1/STS/STS/STS/STS/STS/STS/STS/STS/STS/ST
[9] [9] [9] [9] [9] [6] [6] [6]	ADC1_IN10(PC0) ADC1_IN11(PC1) ADC1_IN11(PC1) ADC1_IN12(PC2) ADC1_IN13(PC3) ADC1_IN14(PC4) ADC1_IN14(PC4) ADC1_IN14(PC4) ADC1_IN15(PC5) ADC1_I	PC0/OTG HS_ULPI_STP/EVENTOUT/ADC123_IN10 PC1/ETH_MDC/EVENTOUT/ADC123_IN11 PC2/SPI2_MDS(O/TG HS_ULPI_DIR7H_MII_TXD2/I2S2ext_SD/EVENTOUT/ADC123_IN12 PC2/SPI2_MDS(O/TG HS_ULPI_DIR7H_MII_TXD2/I2S2ext_SD/EVENTOUT/ADC123_IN12 PC3/SPI2_MDS/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CL/EVENTOUT/ADC123_IN13 PC4/ETH_FMII_RX_DD/ETH_MII_RX_DV/EVENTOUT/ADC12_IN14 PC5/ETH_RMII_RX_DU/ETH_MII_RX_DV/EVENTOUT/ADC12_IN15 PC6/I2S2_MCK/TIMB_CH/I3SD/D_D6/USARTE_TX/DCM_D0/TIM3_CH/EVENTOUT PC6/I2S3_MCK/TIMB_CH/EVENTOUT/ADC12_IN13_CH/EVENTOUT PC3/IS33_MCK/TIMB_CH/EVENTOUT/ADC12_IN13_CH/EVENTOUT PC3/IS3_MCM/ISSD/D_D0/TIM3_CH/EVENTOUT PC3/IS3_CK/INMC02/TIM8_CH/EVENTOUT PC3/IS3_CK/INMC02/TIM8_CH/EVENTOUT PC10/SPI3_SCK/IZS3_CK/URARTA_TX/SDIO_D2/DCM_D0/EVENTOUT PC10/SPI3_SCK/IZS3_CK/URARTA_TX/SDIO_D2/DCM_D0/EVENTOUT PC11/UARTA_RX/SPI3_MISO/SD/D_D3/DCM_D4/ISA_T3_TX/EVENTOUT PC11/UARTA_TX/SDIO_D5/DCM_D9/SPI3_MOS/IJS3_SD/USART3_CK/EVENTOUT PC13/EVENTOUT/TCC_AF1 PC14-OSC32_UMPC14/EVENTOUT/OSC32_UN PC15-OSC32_OUT/PC15/EVENTOUT/OSC32_OUT

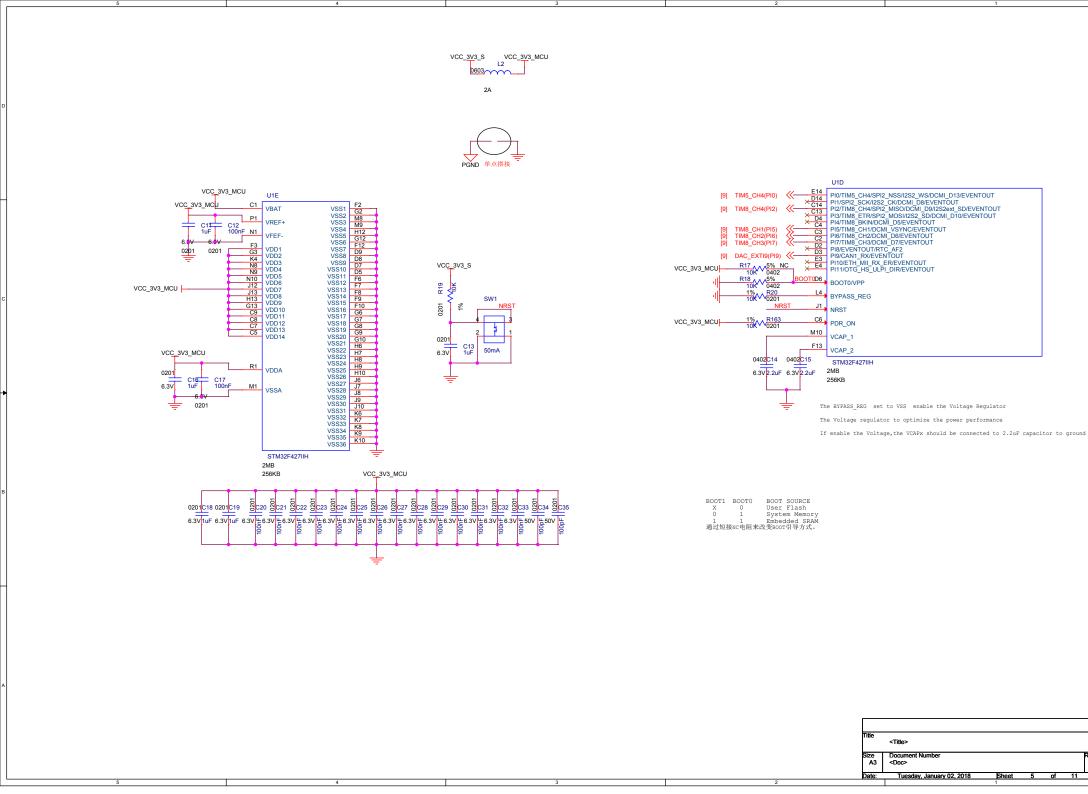
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