

# Lab: 5

*ES 204: Digital Systems*

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# 4-bit Comparator

## A) 4-Bit Comparator Circuit:

The screenshot shows a text editor window titled "comparator4bit.v" with the file path "F:/IITGN/ES 204 Digital Systems/LabAssignment5/LabAssignment5.srsc/sources\_1/new/comparator4bit.v". The code is as follows:

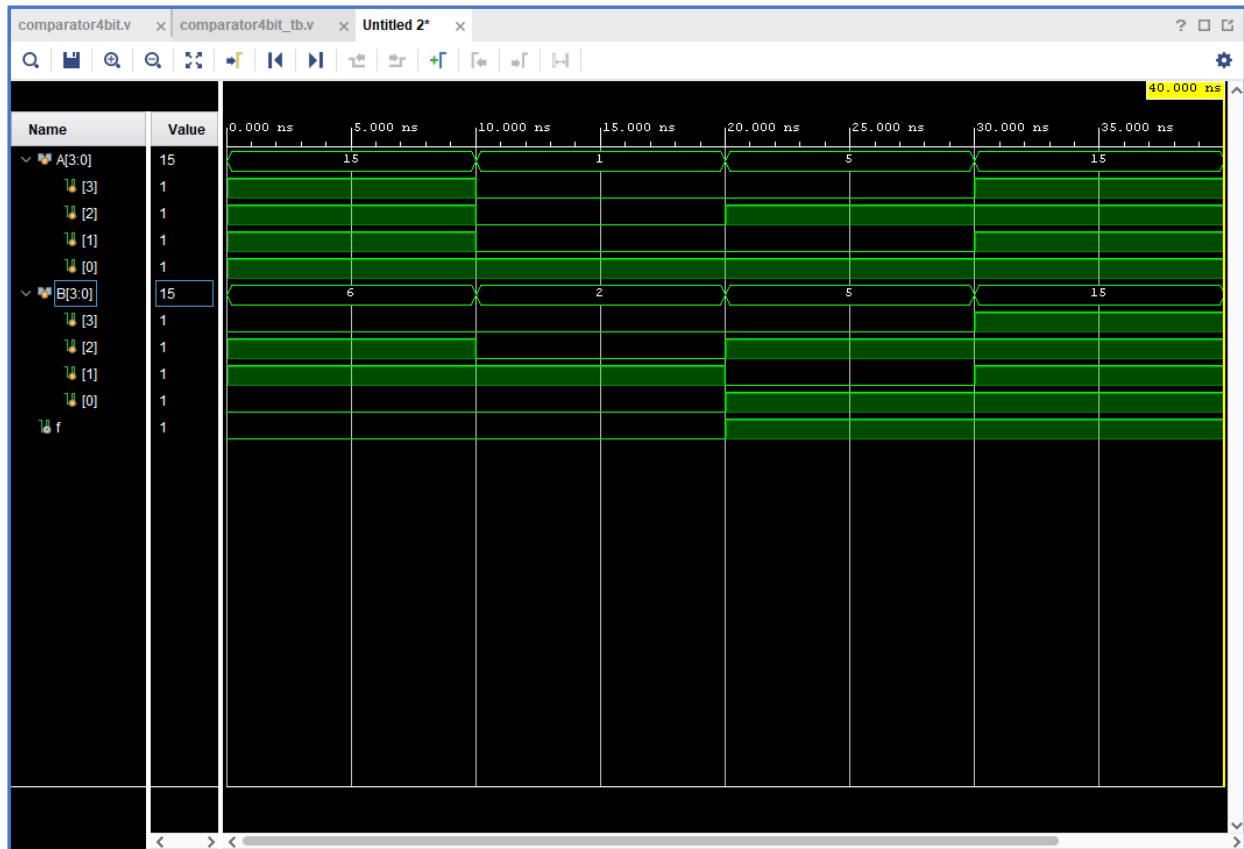
```
1 `timescale 1ns / 1ps
2
3 module comparator4bit(A, B, f);
4     input [3:0]A;
5     input [3:0]B;
6     output reg f;
7
8     always @ (*)
9     begin
10        if (A == B) f = 1;
11        else f = 0;
12    end
13 endmodule
14
```

## B) Test Bench Code :

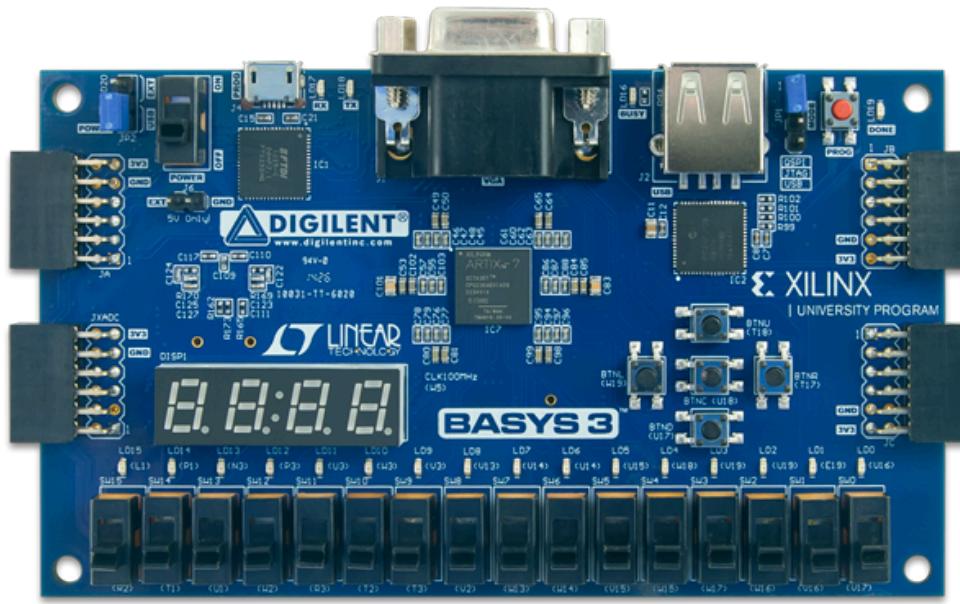
The screenshot shows a text editor window titled "comparator4bit\_tb.v" with the file path "F:/IITGN/ES 204 Digital Systems/LabAssignment5/LabAssignment5.srsc/sim\_1/new/comparator4bit\_tb.v". The code is as follows:

```
1 `timescale 1ns / 1ps
2
3 module comparator4bit_tb();
4     reg [3:0]A;
5     reg [3:0]B;
6     wire f;
7
8     comparator4bit uut(A,B,f);
9     initial
10    begin
11        A = 15; B = 6;
12        #10;
13        A = 1; B = 2;
14        #10;
15        A = 5; B = 5;
16        #10;
17        A = 15; B = 15;
18        #10;
19        $finish();
20    end
21 endmodule
22
```

### C) Stimulation Waveform:



#### D) Synthesis on Basys3 FPGA:



<b>Inputs:</b>	A3 - W17	B3 - R2	<b>Outputs:</b>	f - V13
	A2 - W16	B2 - T1		
	A1 - V16	B1 - U1		
	A0 - V17	B0 - W2		

#### E) Constrain File:

```

Project Summary | Device | comparator4bitv | comparator4bit_tb | comparator4bit_cons.xdc

F:\D\ITGN\ES 204 Digital Systems\LabAssignment5\LabAssignment5.srscs\constrs_1\new\comparator4bit_cons.xdc

Q | H | ← | → | X | E | F | X | // | E | Q |

1 : set_property IOSTANDARD LVCMOS33 [get_ports f]
2 : set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
3 : set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
4 : set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
5 : set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
6 : set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}]
7 : set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}]
8 : set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}]
9 : set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]
10 : set_property PACKAGE_PIN V13 [get_ports f]
11 : set_property PACKAGE_PIN W17 [get_ports {A[3]}]
12 : set_property PACKAGE_PIN W16 [get_ports {A[2]}]
13 : set_property PACKAGE_PIN V16 [get_ports {A[1]}]
14 : set_property PACKAGE_PIN V17 [get_ports {A[0]}]
15 : set_property PACKAGE_PIN R2 [get_ports {B[3]}]
16 : set_property PACKAGE_PIN T1 [get_ports {B[2]}]
17 : set_property PACKAGE_PIN U1 [get_ports {B[1]}]
18 : set_property PACKAGE_PIN W2 [get_ports {B[0]}]
19 :

```

F) Sample Outputs:

