ASSIGNMENT: 4

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Prof. Joycee Mekie

Indian Institute of Technology, Gandhinagar

Aditya N. Mehta

22110017

Hrriday V. Ruparel

22110099

Creating a 4-bit Asynchronous Counter with Asynchronous Reset

A) Toggle Flip Flop:

```
`timescale 1ns / 1ps

module TFF(T,Q,reset,clk);
input T,reset,clk;
output reg Q;

always @ (posedge clk or posedge reset)
begin
   if (reset)
       Q <= 0;
   else if (T)
       Q <= ~Q;
   else
       Q <= Q;
   end
endmodule
```

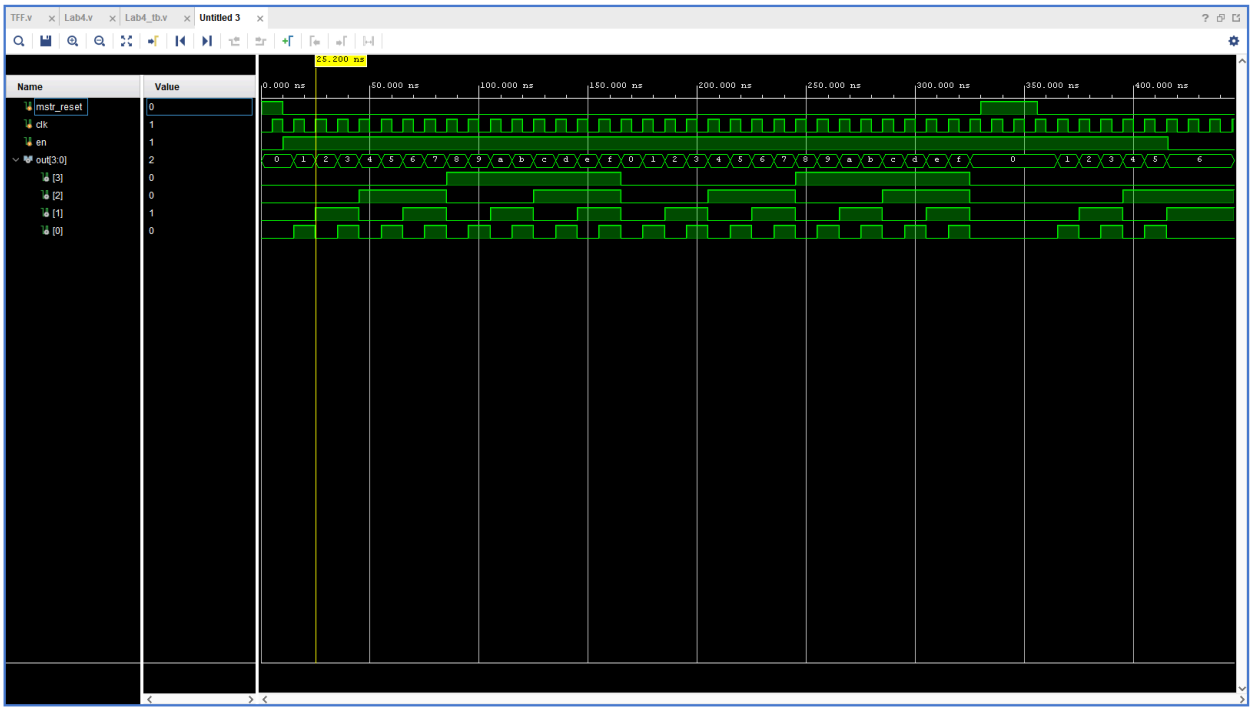
B) 4-bit Up Asynchronous Counter Code:

```
`timescale 1ns / 1ps

module Lab4(mstr_reset, clk, out, en);
input mstr_reset, clk, en;
output [3:0]out;

   and (clk_en, clk, en);
   TFF tff0(.T(1), .Q(out[0]), .reset(mstr_reset), .clk(clk_en));
   TFF tff1(.T(1), .Q(out[1]), .reset(mstr_reset), .clk(~out[0]));
   TFF tff2(.T(1), .Q(out[2]), .reset(mstr_reset), .clk(~out[1]));
   TFF tff3(.T(1), .Q(out[3]), .reset(mstr_reset), .clk(~out[2]));
endmodule
```

C) Test Beach Code for Counter:

```
`timescale 1ns / 1ps

module Lab4_tb();
reg mstr_reset, clk, en;
wire [3:0]out;

Lab4 uut(mstr_reset, clk, out, en);

initial
begin
   clk = 0;
   forever #5 clk = ~clk;
end

initial
begin
   mstr_reset = 1; en = 0;
   #10;
   mstr_reset = 0; en = 1;
   #320;
   mstr_reset = 1; en = 1;
   #26;
   mstr_reset = 0; en = 1;
   #50;
   mstr_reset = 0;
   #10;
   mstr_reset = 0; en = 0;
   #30;
   $finish();
end
endmodule
```

D) Simulation Waveform:



E) Schetamic: