

Lab: 6

ES 204: Digital Systems

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4-bit Combined BCD/Binary Up/Down Counter

A) Verilog Code:

```
'timescale 1ns / 1ps
///////////////////////////////
//00 = Binary Up
//01 = Binary Down
//10 = BCD Up
//11 = BCD Down
///////////////////////////////

module counter(clk, Out, Mode1, Mode2);
input clk;
input Mode1, Mode2;
output reg [3:0]Out;

//The next 2 lines are for implementation and should be commented out for
simulation purpose
wire slow_clk;
clock_divider inst(clk, slow_clk);

initial Out = 4'b0000;

always@ (posedge slow_clk) begin

if (Mode1 && Mode2)
    if (Out == 0)
        Out = 9;
    else
        Out <= (Out-1)%10;
else if (Mode1 && ~Mode2)
    Out <= (Out+1)%10;
else if (~Mode1 && Mode2)
    Out <= (Out-1);
else if (~Mode1 && ~Mode2)
    Out <= (Out+1);
end

endmodule
```

B) Test Bench Code :

```
'timescale 1ns / 1ps
///////////////////////////////
//00 = Binary Up
//01 = Binary Down
//10 = BCD Up
//11 = BCD Down
///////////////////////////////

module counter_tb();
reg Mode1, Mode2, clk;
wire [3:0]Out;

initial begin
clk = 0;
forever #5 clk = ~clk;
end

counter uut(.clk(clk), .Out(Out), .Mode1(Mode1), .Mode2(Mode2));
initial begin

Mode1 = 1; Mode2 = 1; #200;
Mode1 = 1; Mode2 = 0; #200;
Mode1 = 0; Mode2 = 1; #200;
Mode1 = 0; Mode2 = 0; #200;

end
endmodule
```

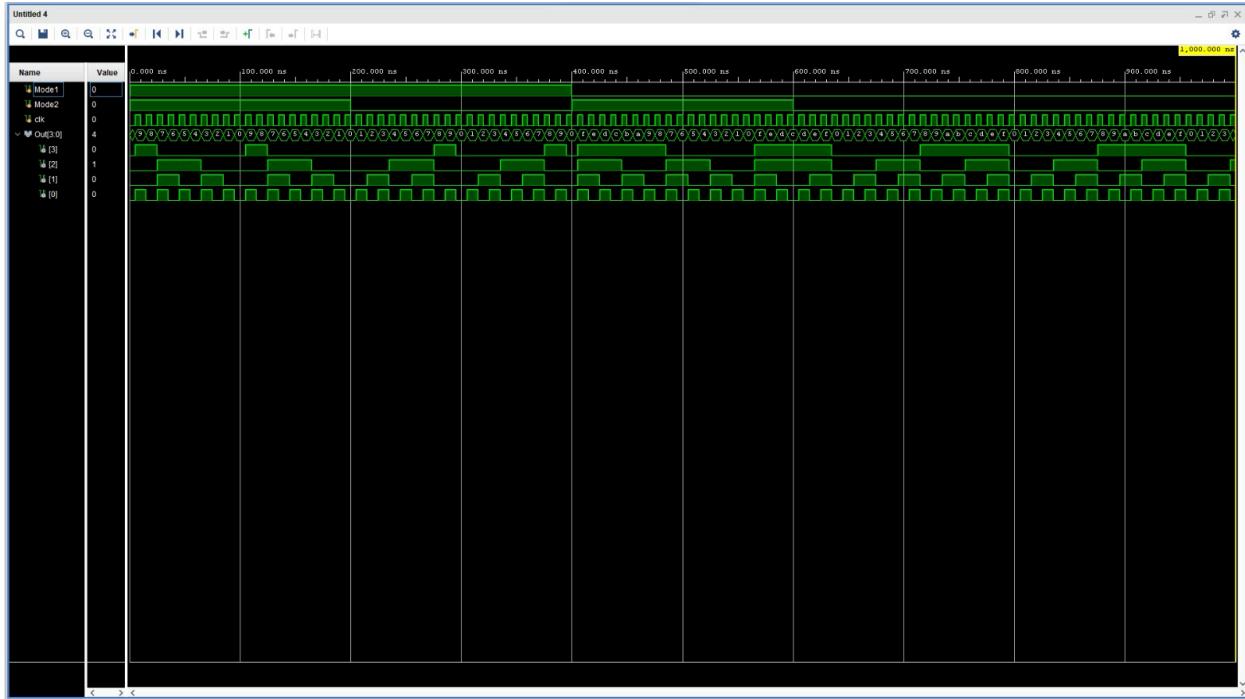
C) Clock Divider Code:

```
'timescale 1ns/1ps

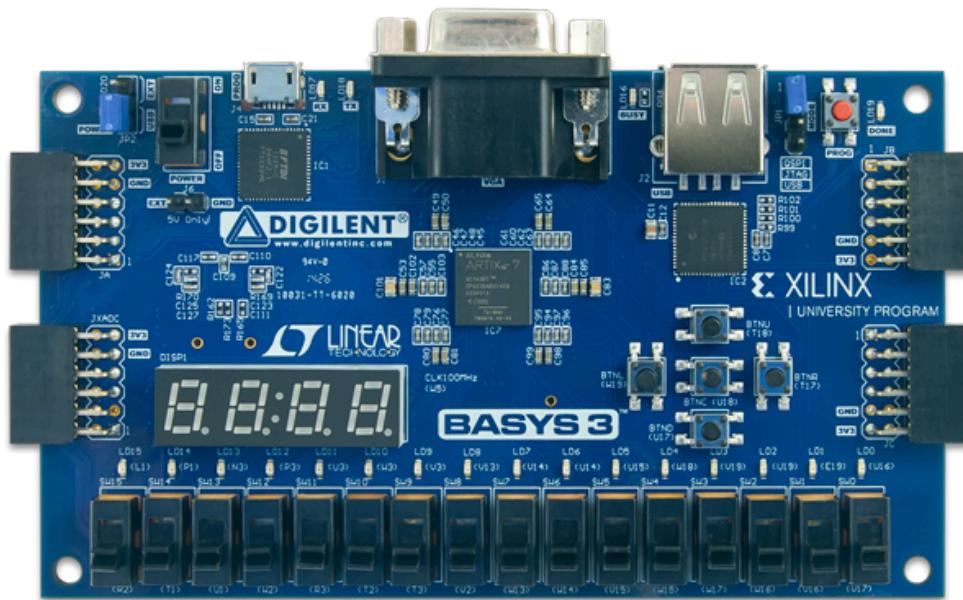
module clock_divider(main_clk, slow_clk);
input main_clk;
output slow_clk;
reg [31:0]counter;

always @ (posedge main_clk) begin
    counter <= counter + 1;
end
assign slow_clk = counter[27];
endmodule
```

D) Stimulation Waveform:



E) Synthesis on Basys3 FPGA:



Inputs: Model1 - T1 Mode2 - R2

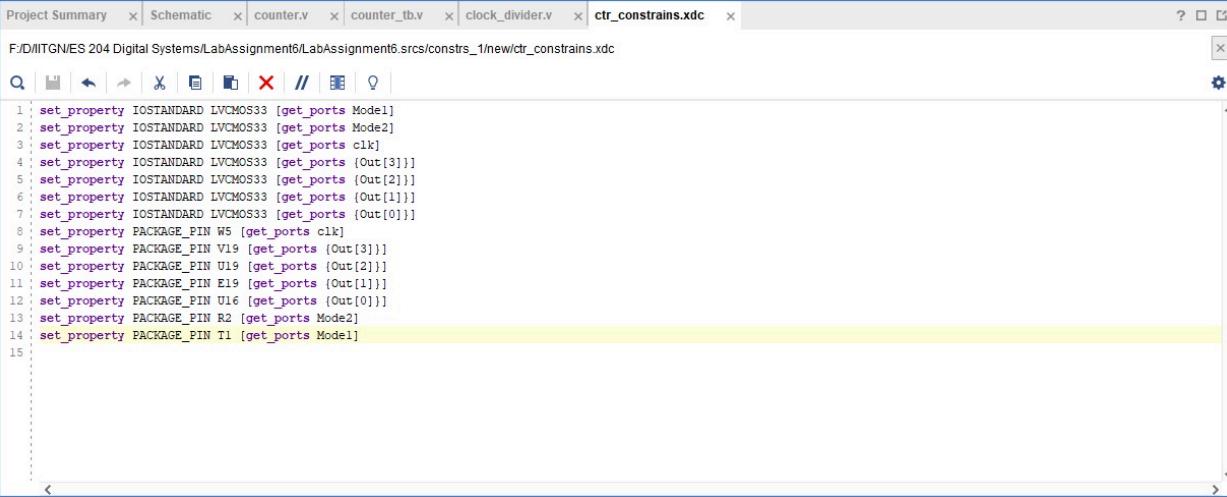
Outputs: Out[3] - V19

Out[2] - U16

Out[1] - E16

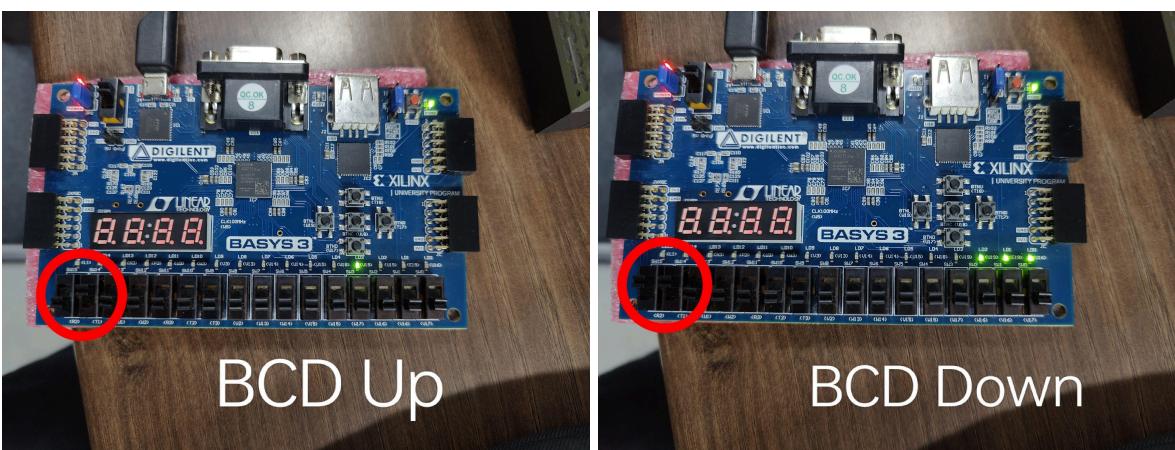
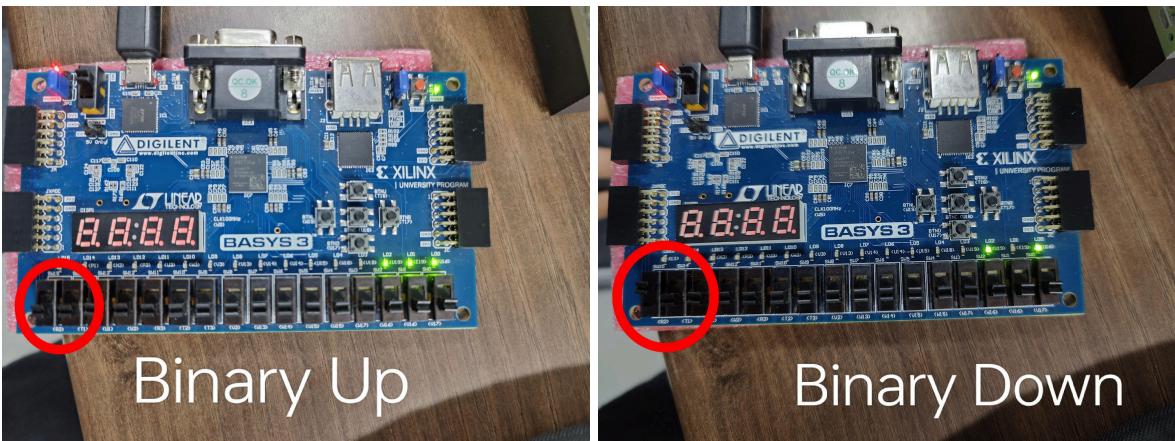
Out[0] - U16

F) Constrain File:



```
1: set_property IO_STANDARD LVCMOS33 [get_ports Model]
2: set_property IO_STANDARD LVCMOS33 [get_ports Mode2]
3: set_property IO_STANDARD LVCMOS33 [get_ports clk]
4: set_property IO_STANDARD LVCMOS33 [get_ports {Out[3]}]
5: set_property IO_STANDARD LVCMOS33 [get_ports {Out[2]}]
6: set_property IO_STANDARD LVCMOS33 [get_ports {Out[1]}]
7: set_property IO_STANDARD LVCMOS33 [get_ports {Out[0]}]
8: set_property PACKAGE_PIN W5 [get_ports clk]
9: set_property PACKAGE_PIN V19 [get_ports {Out[3]}]
10: set_property PACKAGE_PIN U19 [get_ports {Out[2]}]
11: set_property PACKAGE_PIN E19 [get_ports {Out[1]}]
12: set_property PACKAGE_PIN U16 [get_ports {Out[0]}]
13: set_property PACKAGE_PIN R2 [get_ports Mode2]
14: set_property PACKAGE_PIN T1 [get_ports Model]
15:
```

G) Sample Outputs:



H) Power Utilization:

Project Summary | Device | counter.v | clock_divider.v | ctr_constraints.xdc | synth_1_synth_report_utilization_0 - synth_1 | impl_1_route_report_power_0 - impl_1 | Read-only

```

29: 1. Summary
30: -----
31:
32: +-----+
33: | Total On-Chip Power (W) | 16.972 (Junction temp exceeded!) |
34: | Design Power Budget (W) | Unspecified* |
35: | Power Budget Margin (W) | NA |
36: | Dynamic (W) | 16.643 |
37: | Device Static (W) | 0.329 |
38: | Effective TJA (C/H) | 5.0 |
39: | Max Ambient (C) | 0.2 |
40: | Junction Temperature (C) | 109.8 |
41: | Confidence Level | Low |
42: | Setting File | --- |
43: | Simulation Activity File | --- |
44: | Design Nets Matched | NA |
45: +-----+
46: * Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>
47:
48:
49: 1.1 On-Chip Components
50: -----
51:
52: +-----+-----+-----+-----+
53: | On-Chip | Power (W) | Used | Available | Utilization (%) |
54: +-----+-----+-----+-----+
55: | Slice Logic | 2.638 | 207 | --- | --- |
56: | LUT as Logic | 2.467 | 111 | 20800 | 0.53 |
57: | CARRY4 | 0.159 | 30 | 8150 | 0.37 |
58: | BUFG | 0.006 | 1 | 32 | 3.13 |
59: | Register | 0.005 | 4 | 41600 | <0.01 |
60: | F7/F8 Muxes | 0.002 | 1 | 32600 | <0.01 |
61: | Others | 0.000 | 2 | --- | --- |
62: | Signals | 1.411 | 135 | --- | --- |
63: | I/O | 12.593 | 7 | 106 | 6.60 |
64: | Static Power | 0.329 | | | |
65: | Total | 16.972 | | | |
66: +-----+-----+-----+-----+

```

I) LUT Utilization:

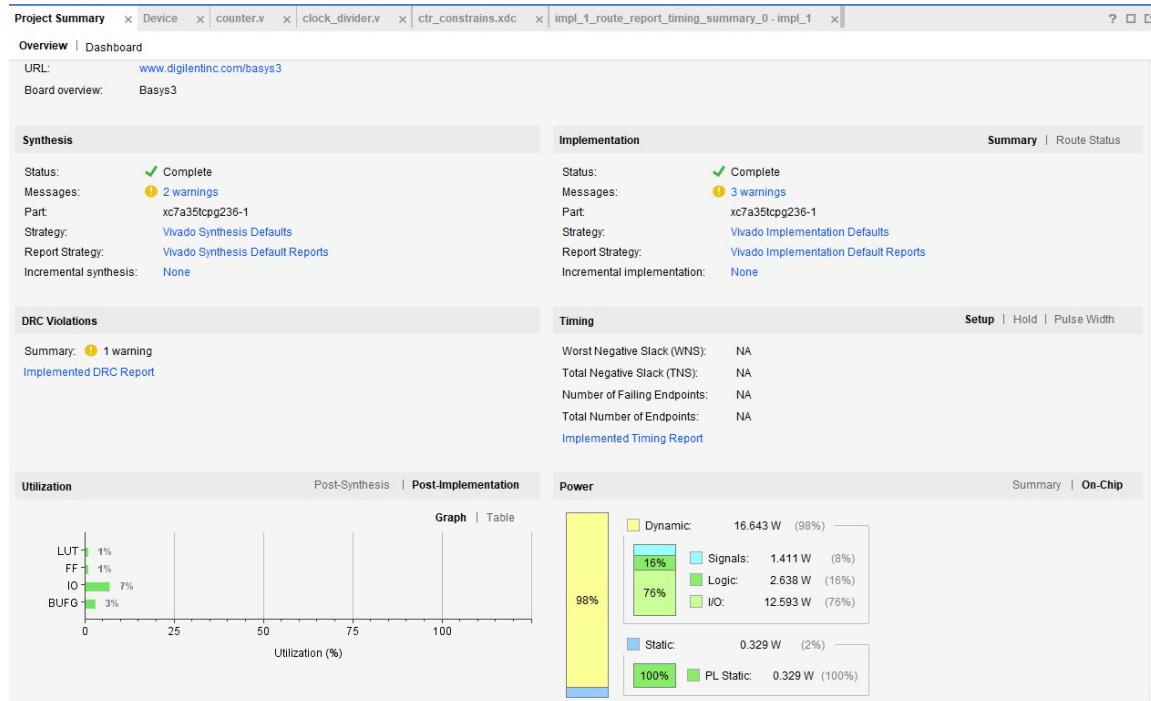
Project Summary | Device | counter.v | clock_divider.v | ctr_constraints.xdc | synth_1_synth_report_utilization_0 - synth_1 | Read-only

```

11:
12: Utilization Design Information
13:
14: Table of Contents
15: -----
16: 1. Slice Logic
17: 1.1 Summary of Registers by Type
18: 2. Memory
19: 3. DSP
20: 4. IO and GT Specific
21: 5. Clocking
22: 6. Specific Feature
23: 7. Primitives
24: 8. Black Boxes
25: 9. Instantiated Netlists
26:
27: 1. Slice Logic
28: -----
29:
30: +-----+-----+-----+-----+
31: | Site Type | Used | Fixed | Available | Util% |
32: +-----+-----+-----+-----+
33: | Slice LUTs* | 111 | 0 | 20800 | 0.53 |
34: | LUT as Logic | 111 | 0 | 20800 | 0.53 |
35: | LUT as Memory | 0 | 0 | 9600 | 0.00 |
36: | Slice Registers | 4 | 0 | 41600 | <0.01 |
37: | Register as Flip Flop | 4 | 0 | 41600 | <0.01 |
38: | Register as Latch | 0 | 0 | 41600 | 0.00 |
39: | F7 Muxes | 1 | 0 | 16300 | <0.01 |
40: | F8 Muxes | 0 | 0 | 8150 | 0.00 |
41: +-----+-----+-----+-----+
42: * Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a mo
43:
44:
45: 1.1 Summary of Registers by Type
46: -----
47:
48: +-----+-----+-----+
49: | Total | Clock Enable | Synchronous | Asynchronous |
50: +-----+-----+-----+

```

J) Project Summary:



K) Timing Report:

Tcl Console

Timing Report

Location	Delay type	Incr(ns)	Path(ns)	Netlist	Resource(s)
SLICE_X2Y36		inf	Out_req[1]/C		
Source:			(rising edge-triggered cell FIRE)		
Destination:			Out_req[1]/D		
Setup:					
Path Type:			Max at Slow Process Corner		
Data Path Delay:		15.765ns	(logic 6,301ns (39.960ns) route 9.464ns (60.032ns))		
Logic Levels:		19	(CARRY4#P FIRE#L LUT#1 LUT#3= LUT#4= LUT#2 LUT#4=L)		
SLICE_X2Y36		0.000	0.000 x Out_req[1]/C		
SLICE_X2Y36		0.000	0.010 x Out_req[1]/C		
		0.000	1.045 x Out_req[1]/C		
SLICE_X2Y31	LUT4 (Prop_int_12_0)	0.180	2.313 x Out[2]_1_n7/n70		
		0.180	1.192 x Out[2]_1_n7/n70		
		0.000	3.805 x Out[2]_1_n7/n70		
SLICE_X2Y28	LUT4 (Prop_int_14_0)	0.226	2.313 x Out[2]_1_n7/n70		
		0.000	1.192 x Out[2]_1_n7/n70		
		0.000	3.831 x Out[2]_1_n7/n70		
SLICE_X2Y28	CARRY4 (Prop_carry4_S[1]/CO[3])	0.550	4.381 x Out_req[2]_1_n31/CO[3]		
		0.000	4.381 x Out_req[2]_1_n31/n31		
SLICE_X2Y29	CARRY4 (Prop_carry4_C[1]/CO[1])	0.157	4.838 x Out_req[2]_1_n04/CO[1]		
		1.020	5.878 x Out_req[2]_1_n04/n04		
SLICE_X2Y33	LUT3 (Prop_int_11_0)	0.353	6.144 x Out[2]_1_n6/n60		
		0.353	2.194 x Out[2]_1_n6/n60		
SLICE_X2Y31	LUT4 (Prop_int_10_0)	0.328	7.748 x Out[2]_1_n3/n30		
		0.000	7.748 x Out[2]_1_n3/n30		
SLICE_X2Y31	CARRY4 (Prop_carry4_S[1]/CO[3])	0.533	8.301 x Out_req[2]_1_n32/CO[3]		
		0.000	8.301 x Out_req[2]_1_n32/n32		
SLICE_X2Y32	CARRY4 (Prop_carry4_C[2]/CO[2])	0.239	8.840 x Out_req[2]_1_n11/CO[2]		
		0.784	9.324 x Out_req[2]_1_n11/n11		
SLICE_X2Y32	LUT3 (Prop_int_12_0)	0.350	9.450 x Out[2]_1_n11/n11		
		0.350	20.759 x Out[2]_1_n11/n11		
SLICE_X2Y32	LUT4 (Prop_int_13_0)	0.327	11.036 x Out[2]_1_n3/n30		
		0.000	11.036 x Out[2]_1_n3/n30		
SLICE_X2Y32	CARRY4 (Prop_carry4_S[3]/CO[3])	0.401	11.437 x Out_req[2]_1_n19/CO[3]		
		0.000	11.437 x Out_req[2]_1_n19/n19		
SLICE_X2Y33	CARRY4 (Prop_carry4_C[1]/CO[1])	0.334	11.771 x Out_req[2]_1_n15/CO[1]		
		0.897	12.879 x Out_req[2]_1_n15/n15		
SLICE_X2Y35	LUT2 (Prop_int_11_0)	0.303	12.881 x Out[2]_1_n7/n70		
		0.000	12.881 x Out[2]_1_n7/n70		
SLICE_X2Y35	CARRY4 (Prop_carry4_S[1]/CO[3])	0.401	14.415 x Out_req[2]_1_n3/CO[3]		
		0.000	14.415 x Out_req[2]_1_n3/n3		
open_run impl1_1					
SLICE_X2Y37		0.000	14.415 x Out_req[2]_1_n2/n0		
		0.000	14.415 x Out_req[2]_1_n2/n0		
SLICE_X2Y36		0.232	14.437 x Out_req[2]_1_n3/CO[0]		
		0.232	15.484 x Out_req[2]_1_n3/n3		
SLICE_X2Y36	LUT6 (Prop_int_10_0)	0.299	15.765 x Out[2]_1_n1/n7		
		0.000	15.765 x Out[2]_1_n1/n7		
SLICE_X2Y36		0.000	15.765 x Out[2]_1_n1/n7		
		0.000	15.765 x Out[2]_1_n1/n7		
open_run impl1_1					