

Lab Assignment 4

ES 204: Digital Systems

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N-bit Parameterized Binary Multiplier Circuit

A) Verilog Code:

```
'timescale 1ns / 1ps
module bin_mul(A,B,OUT);

parameter n=8;
input [n-1:0] A;
input [n-1:0] B;
output reg [2*n-1:0] OUT;
integer i;

always @(*)
Begin
    OUT = 0;
    for(i=0;i<n;i=i+1)
    begin
        if(B[i]==1) begin
            OUT = OUT + (A<<i);
        end
    end
end
endmodule
```

B) Test Bench Code (8 bit x 8 bit) :

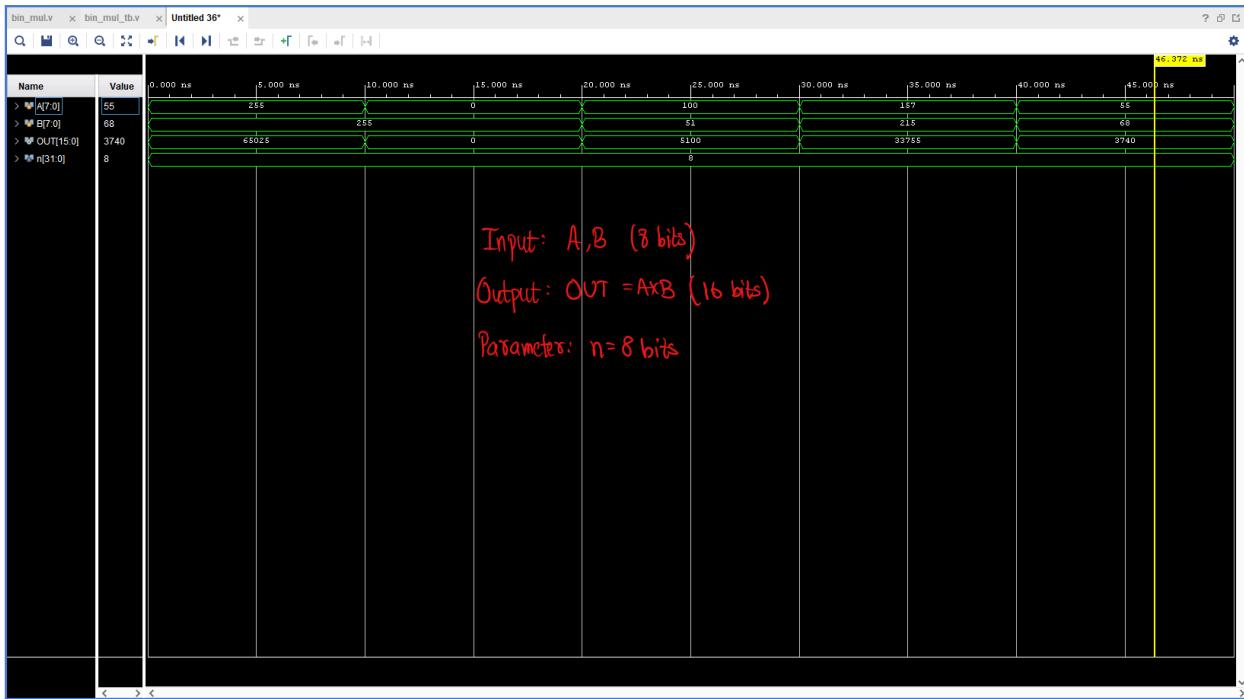
```
'timescale 1ns / 1ps

module bin_mul_tb();
parameter n = 8;
reg [n-1:0]A;
reg [n-1:0]B;
wire [2*n-1:0]OUT;

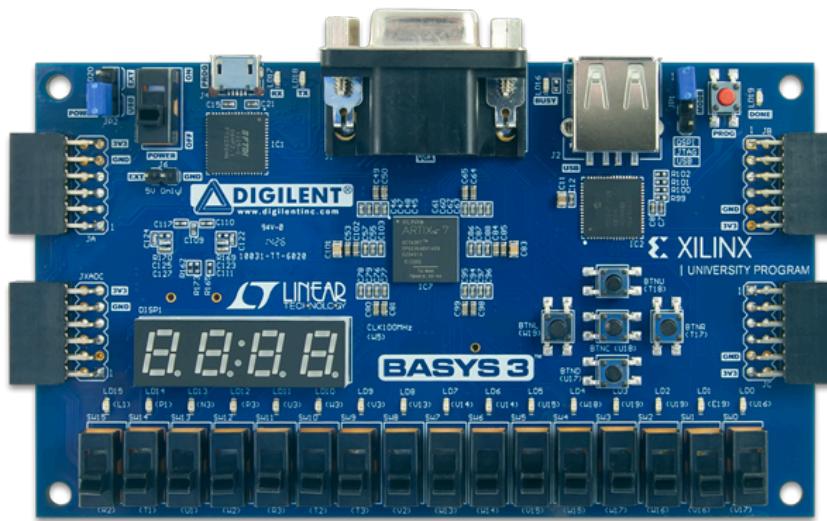
bin_mul uut(A, B, OUT);

initial
begin
    A = 255; B = 255;
    #10;
    A = 0; B = 255;
    #10;
    A = 100; B = 51;
    #10;
    A = 157; B = 215;
    #10;
    A = 55; B = 68;
    #10;
    $finish();
end
endmodule
```

C) Stimulation Waveform:

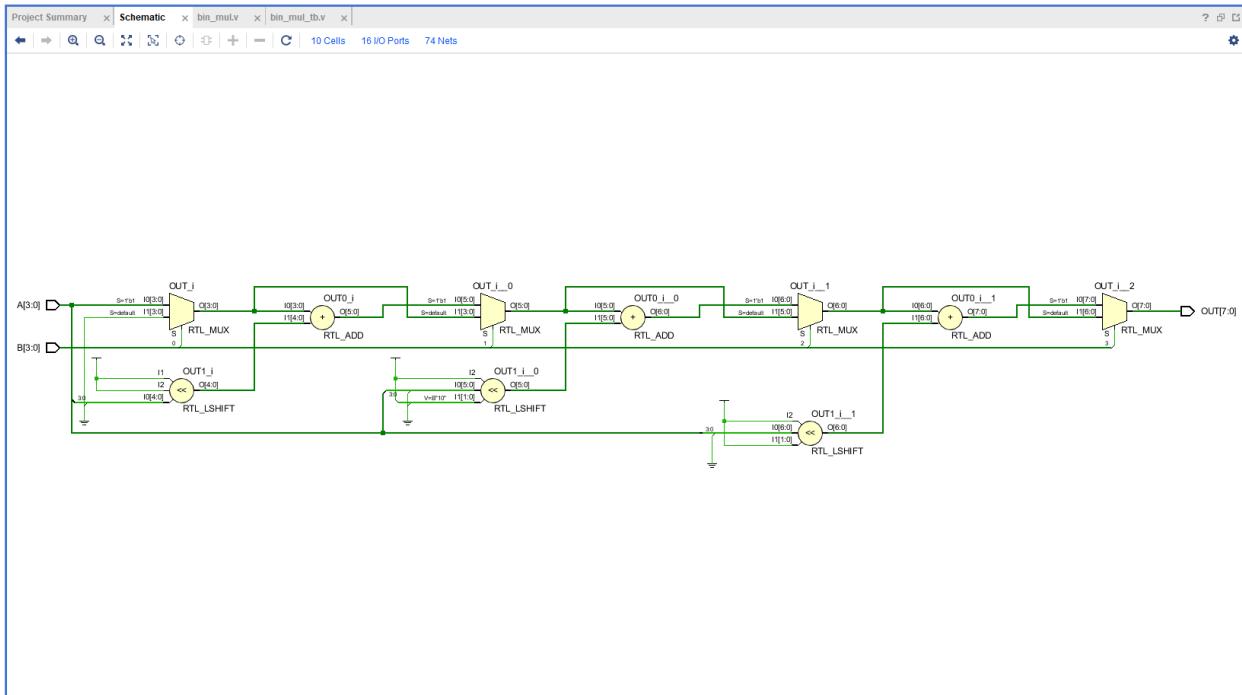


D) Synthesis on Basys3 FPGA (4 bit x 4 bit):



Inputs: A - R2 to W2 Switches
 B - W17 to U17 Switches
Outputs: OUT - U14 to U16 LEDs

E) Schematic Diagram:



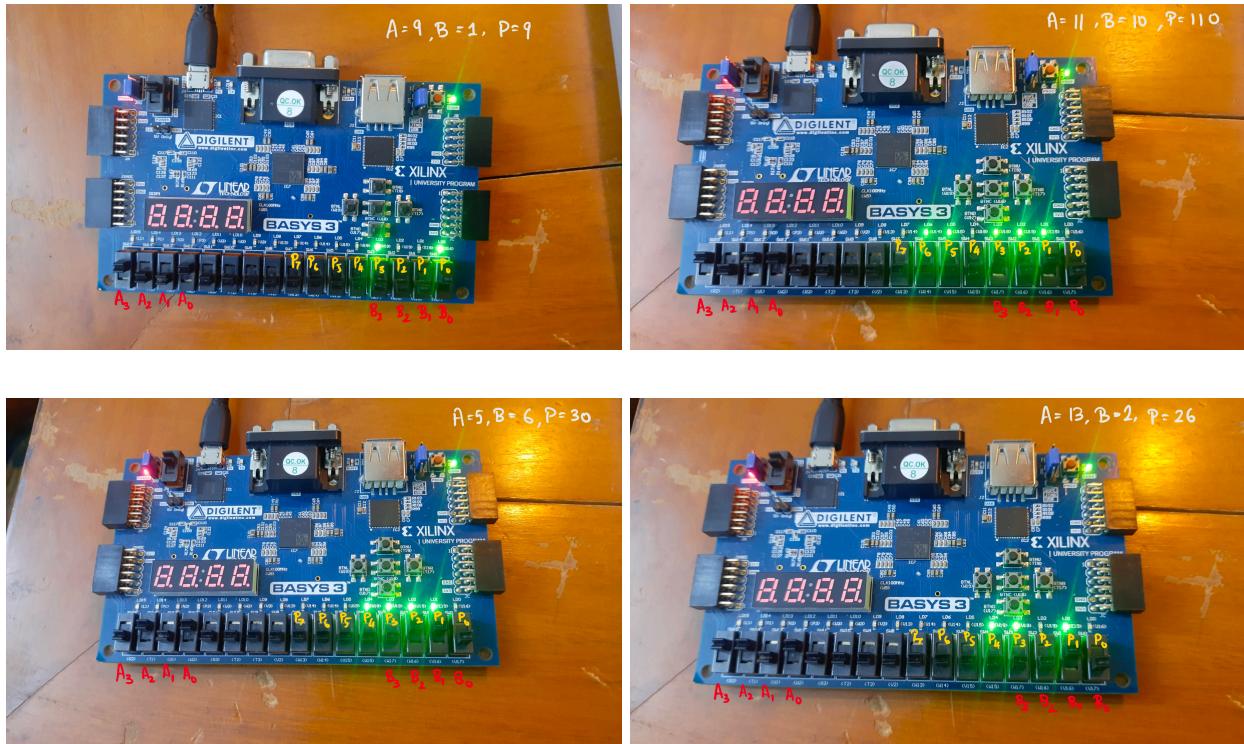
F) Constrain File:

```

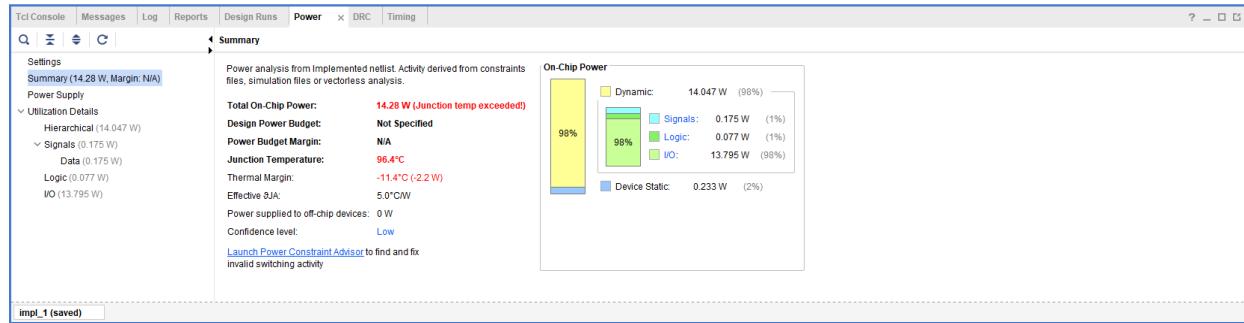
Schematic x arr_mul.v x arr_mul_tb.v x constraints.xdc x
F:\IITGN\ES 204 Digital Systems\Assignment\Assignment4\srcs\constrs_1\new\constraints.xdc
? x
1 :set_property ISSTANDARD LVCMOS33 [get_ports {A[3]}]
2 :set_property ISSTANDARD LVCMOS33 [get_ports {A[2]}]
3 :set_property ISSTANDARD LVCMOS33 [get_ports {A[1]}]
4 :set_property ISSTANDARD LVCMOS33 [get_ports {A[0]}]
5 :set_property ISSTANDARD LVCMOS33 [get_ports {B[3]}]
6 :set_property ISSTANDARD LVCMOS33 [get_ports {B[2]}]
7 :set_property ISSTANDARD LVCMOS33 [get_ports {B[1]}]
8 :set_property ISSTANDARD LVCMOS33 [get_ports {B[0]}]
9 :set_property ISSTANDARD LVCMOS33 [get_ports {OUT[7]}]
10 :set_property ISSTANDARD LVCMOS33 [get_ports {OUT[6]}]
11 :set_property ISSTANDARD LVCMOS33 [get_ports {OUT[5]}]
12 :set_property ISSTANDARD LVCMOS33 [get_ports {OUT[4]}]
13 :set_property ISSTANDARD LVCMOS33 [get_ports {OUT[3]}]
14 :set_property ISSTANDARD LVCMOS33 [get_ports {OUT[2]}]
15 :set_property ISSTANDARD LVCMOS33 [get_ports {OUT[1]}]
16 :set_property ISSTANDARD LVCMOS33 [get_ports {OUT[0]}]
17 :set_property PACKAGE_PIN R2 [get_ports {A[3]}]
18 :set_property PACKAGE_PIN T1 [get_ports {A[2]}]
19 :set_property PACKAGE_PIN U1 [get_ports {A[1]}]
20 :set_property PACKAGE_PIN W2 [get_ports {A[0]}]
21 :set_property PACKAGE_PIN W17 [get_ports {B[3]}]
22 :set_property PACKAGE_PIN W16 [get_ports {B[2]}]
23 :set_property PACKAGE_PIN V16 [get_ports {B[1]}]
24 :set_property PACKAGE_PIN V17 [get_ports {B[0]}]
25 :set_property PACKAGE_PIN V14 [get_ports {OUT[7]}]
26 :set_property PACKAGE_PIN V14 [get_ports {OUT[6]}]
27 :set_property PACKAGE_PIN V15 [get_ports {OUT[5]}]
28 :set_property PACKAGE_PIN W18 [get_ports {OUT[4]}]
29 :set_property PACKAGE_PIN V19 [get_ports {OUT[3]}]
30 :set_property PACKAGE_PIN V19 [get_ports {OUT[2]}]
31 :set_property PACKAGE_PIN E19 [get_ports {OUT[1]}]
32 :set_property PACKAGE_PIN V16 [get_ports {OUT[0]}]
33 :

```

G) Sample Outputs:



H) Power Report:



I) LUT Utilization:

Utilization Design Information

Table of Contents

-
- 1. Slice Logic
 - 1.1 Summary of Registers by Type
 - 2. Memory
 - 3. DSP
 - 4. IO and GT Specific
 - 5. Clocking
 - 6. Specific Feature
 - 7. Primitives
 - 8. Black Boxes
 - 9. Instantiated Netlists

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	16	0	20800	0.08
LUT as Logic	16	0	20800	0.08
LUT as Memory	0	0	9600	0.00
Slice Registers	0	0	41600	0.00
Register as Flip Flop	0	0	41600	0.00
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

J) Timing Report:

Timing Report

Slack: inf
 Source: A[2]
 (input port)
 Destination: OUT[6]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 13.533ns (logic 6.027ns (44.540%) route 7.505ns (55.460%))
 Logic Levels: 6 (CARRY4=2 IBUF=1 LUT6=2 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
T1		0.000	0.000	r A[2] (IN)
T1	net (fo=0)	0.000	0.000	A[2]
T1	IBUF (Prop_ibuf_I_0)	1.455	1.455	r A_IBUF[2]_inst/0
	net (fo=9, routed)	4.418	5.873	A_IBUF[2]
SLICE_X1Y15	LUT6 (Prop_lut6_I4_0)	0.124	5.997	r OUT_OBUF[3]_inst_i_2/0
	net (fo=2, routed)	0.807	6.804	OUT_OBUF[3]_inst_i_2_n_0
SLICE_X0Y15	LUT6 (Prop_lut6_I0_0)	0.124	6.928	r OUT_OBUF[3]_inst_i_5/0
	net (fo=1, routed)	0.000	6.928	OUT_OBUF[3]_inst_i_5_n_0
SLICE_X0Y15	CARRY4 (Prop_carry4_S[3]_CO[3])	0.401	7.329	r OUT_OBUF[3]_inst_i_1/CO[3]
	net (fo=1, routed)	0.000	7.329	OUT_OBUF[3]_inst_i_1_n_0
SLICE_X0Y16	CARRY4 (Prop_carry4_CI_0[2])	0.239	7.568	r OUT_OBUF[7]_inst_i_1/0[2]
	net (fo=1, routed)	2.280	9.848	OUT_OBUF[6]
U14	OBUF (Propobuf_I_0)	3.684	13.533	r OUT_OBUF[6]_inst/0
	net (fo=0)	0.000	13.533	OUT[6]
U14			r	OUT[6] (OUT)

N-bit Parameterized Array Multiplier Circuit

A) Verilog Code:

```
'timescale 1ns / 1ps

module arr_mul(A,B,OUT);

parameter n = 8;
input [n-1:0]A;
input [n-1:0]B;
output reg [2*n-1:0]OUT;
reg [n-2:0]P;
reg [n:0]PP1;
reg [n-1:0]PP2;
integer k;

always @ (*) begin
    if (B[0] == 1 && B[1] == 1)
    begin
        PP1 = {1'b0,A};
        PP2 = A;
    end
    else if (B[0] == 1 && B[1] == 0)
    begin
        PP1 = {1'b0,A};
        PP2 = 0;
    end
    else if (B[0] == 0 && B[1] == 1)
    begin
        PP1 = 0;
        PP2 = A;
    end
    else
    begin
        PP1 = 0;
        PP2 = 0;
    end
    P[0] = PP1[0];
    PP1[n:0] = PP1[n:1] + PP2[n-1:0];
    P[1] = PP1[0];
    for(k = 2; k < n; k = k + 1)
    begin
        if (B[k] == 1)
        begin
            PP2 = A;
            PP1[n:0] = PP1[n:1] + PP2[n-1:0];
            P[k] = PP1[0];
        end
        else
        begin
            PP1 = PP1 >> 1;
            P[k] = PP1[0];
        end
    end
    OUT = {PP1,P};
end
endmodule
```

B) Test Bench Code (8 bit x 8 bit) :

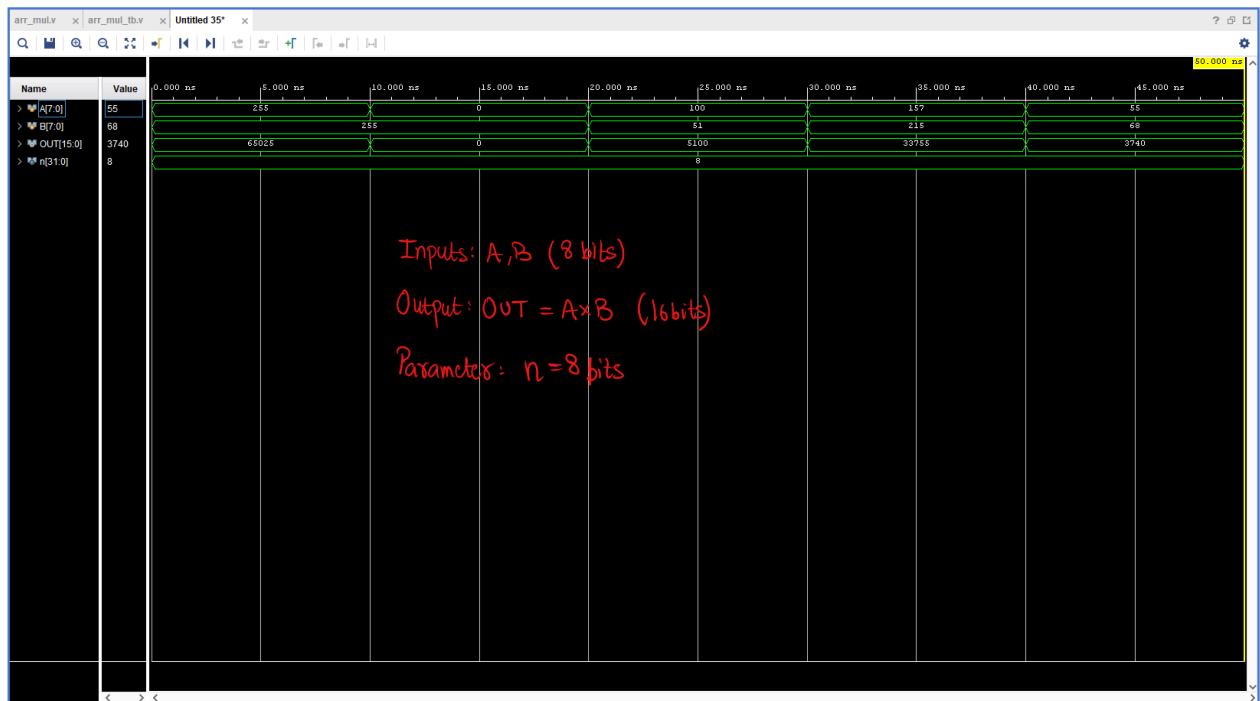
```
'timescale 1ns / 1ps

module arr_mul_tb();
parameter n = 8;
reg [n-1:0]A;
reg [n-1:0]B;
wire [2*n-1:0]OUT;

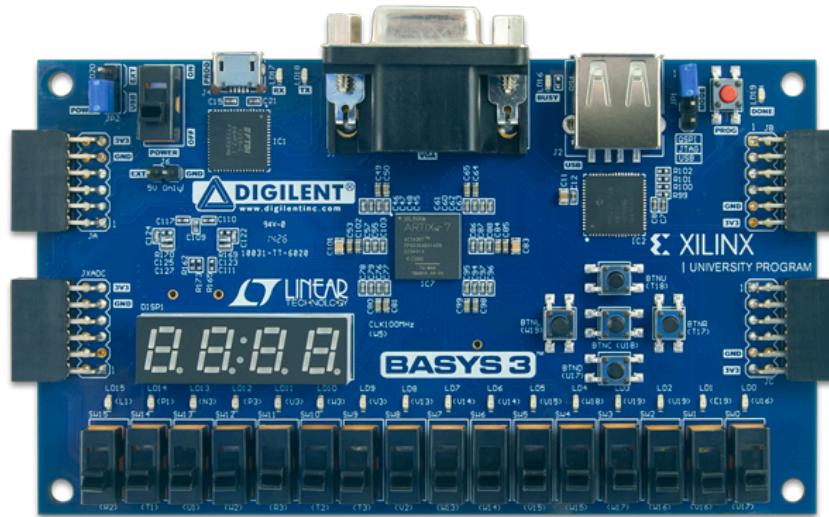
arr_mul uut(A, B, OUT);

initial
begin
    A = 255; B = 255;
    #10;
    A = 0; B = 255;
    #10;
    A = 100; B = 51;
    #10;
    A = 157; B = 215;
    #10;
    A = 55; B = 68;
    #10;
    $finish();
end
endmodule
```

C) Stimulation Waveform:

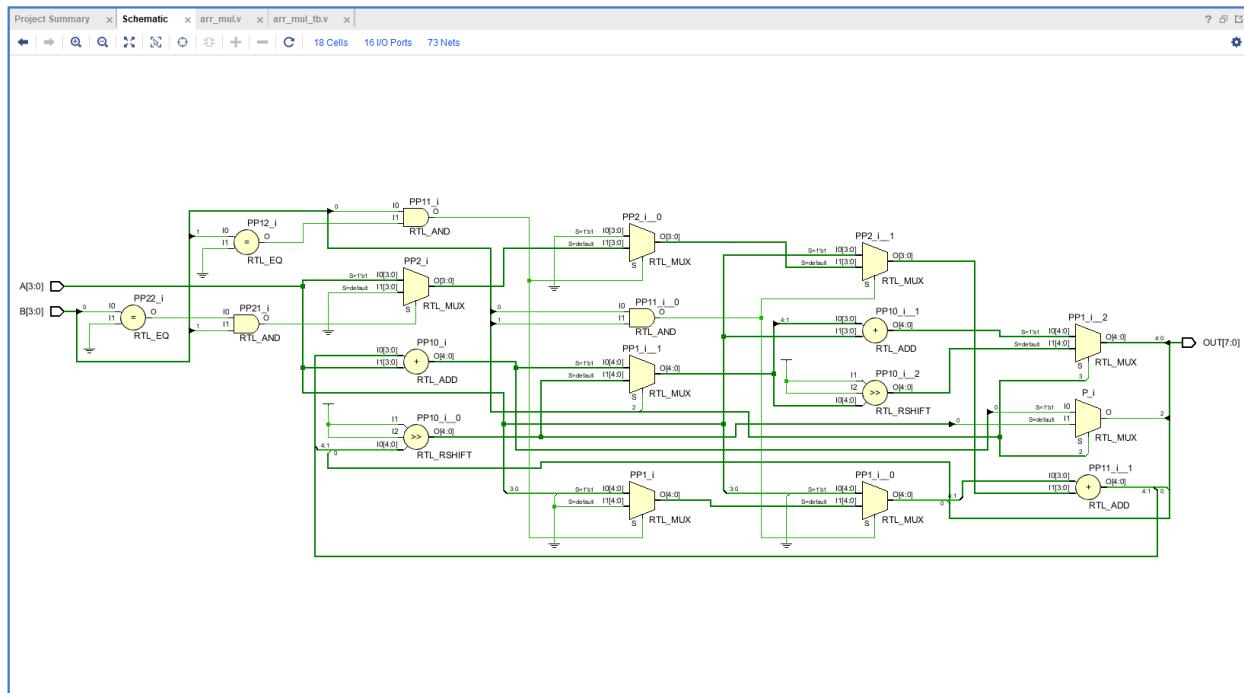


D) Synthesis on Basys3 FPGA (4 bit x 4 bit):



Inputs: A - R2 to W2 Switches
B - W17 to U17 Switches
Outputs: OUT - U14 to U16 LEDs

E) Schematic Diagram:



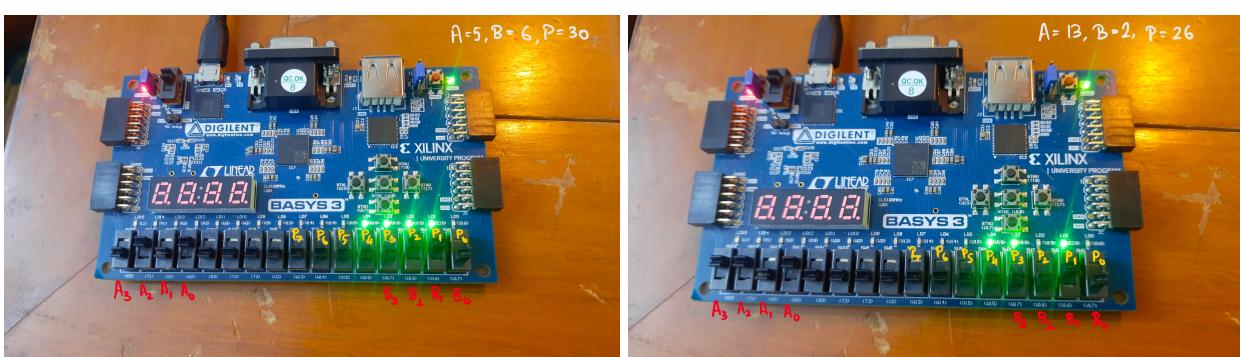
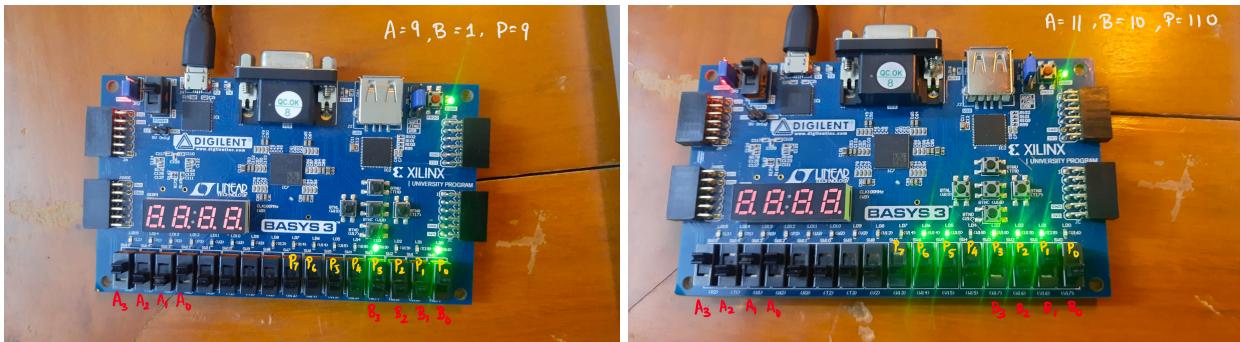
F) Constrain File:

```

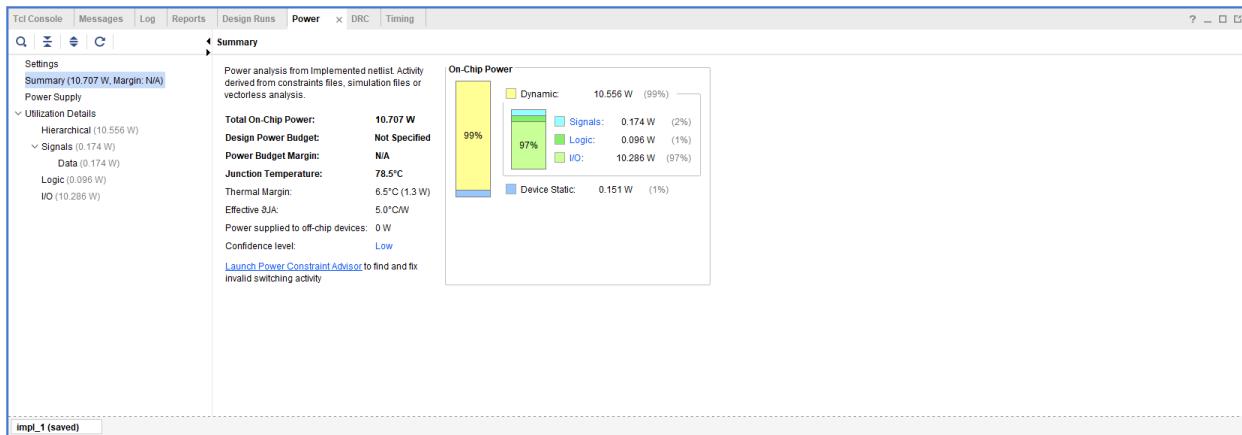
Schematic | arr_mult.v | arr_mult_tb.v | constraints.xdc | 
F:\DITGNMES 204 Digital Systems\Assignment4\Assignment4 srcs\constrs_1\new\constraints.xdc
Q | L | ← | → | X | E | D | X | // | ■ | Q |
1 : set_property IOSTANDARD LVCMS33 [get_ports A[3]]
2 : set_property IOSTANDARD LVCMS33 [get_ports A[2]]
3 : set_property IOSTANDARD LVCMS33 [get_ports A[1]]
4 : set_property IOSTANDARD LVCMS33 [get_ports A[0]]
5 : set_property IOSTANDARD LVCMS33 [get_ports B[3]]
6 : set_property IOSTANDARD LVCMS33 [get_ports B[2]]
7 : set_property IOSTANDARD LVCMS33 [get_ports B[1]]
8 : set_property IOSTANDARD LVCMS33 [get_ports B[0]]
9 : set_property IOSTANDARD LVCMS33 [get_ports OUT[7]]
10 : set_property IOSTANDARD LVCMS33 [get_ports OUT[6]]
11 : set_property IOSTANDARD LVCMS33 [get_ports OUT[5]]
12 : set_property IOSTANDARD LVCMS33 [get_ports OUT[4]]
13 : set_property IOSTANDARD LVCMS33 [get_ports OUT[3]]
14 : set_property IOSTANDARD LVCMS33 [get_ports OUT[2]]
15 : set_property IOSTANDARD LVCMS33 [get_ports OUT[1]]
16 : set_property IOSTANDARD LVCMS33 [get_ports OUT[0]]
17 : set_property PACKAGE_PIN R2 [get_ports A[3]]
18 : set_property PACKAGE_PIN T1 [get_ports A[2]]
19 : set_property PACKAGE_PIN U1 [get_ports A[1]]
20 : set_property PACKAGE_PIN W2 [get_ports A[0]]
21 : set_property PACKAGE_PIN W17 [get_ports B[3]]
22 : set_property PACKAGE_PIN W16 [get_ports B[2]]
23 : set_property PACKAGE_PIN V16 [get_ports B[1]]
24 : set_property PACKAGE_PIN V17 [get_ports B[0]]
25 : set_property PACKAGE_PIN V14 [get_ports OUT[7]]
26 : set_property PACKAGE_PIN V14 [get_ports OUT[6]]
27 : set_property PACKAGE_PIN U15 [get_ports OUT[5]]
28 : set_property PACKAGE_PIN W18 [get_ports OUT[4]]
29 : set_property PACKAGE_PIN V19 [get_ports OUT[3]]
30 : set_property PACKAGE_PIN U19 [get_ports OUT[2]]
31 : set_property PACKAGE_PIN E19 [get_ports OUT[1]]
32 : set_property PACKAGE_PIN U16 [get_ports OUT[0]]
33 :

```

G) Sample Outputs:



H) Power Report:



I) LUT Utilization:

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1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	21	0	20800	0.10
LUT as Logic	21	0	20800	0.10
LUT as Memory	0	0	9600	0.00
Slice Registers	0	0	41600	0.00
Register as Flip Flop	0	0	41600	0.00
Register as Latch	0	0	41600	0.00
F7 Muxes	6	0	16300	0.04
F8 Muxes	3	0	8150	0.04

J) Timing Report:

Timing Report

Slack: inf
 Source: A[3]
 (input port)
 Destination: OUT[6]
 (output port)
 Path Group: (none)
 Path Type: Max at Slow Process Corner
 Data Path Delay: 12.620ns (logic 5.210ns (41.287%) route 7.409ns (58.713%))
 Logic Levels: 4 (IBUF=1 LUT5=1 LUT6=1 OBUF=1)

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
R2		0.000	0.000	r A[3] (IN)
	net (fo=0)	0.000	0.000	A[3]
R2	IBUF (Prop_ibuf_I_0)	1.456	1.456	r A_IBUF[3]_inst/0
	net (fo=17, routed)	4.471	5.927	A_IBUF[3]
SLICE_X1Y17	LUT6 (Prop_lut6_I5_0)	0.124	6.051	r OUT_OBUF[6]_inst_i_2/0
	net (fo=1, routed)	0.670	6.721	OUT_OBUF[6]_inst_i_2_n_0
SLICE_X1Y17	LUT5 (Prop_lut5_I0_0)	0.124	6.845	r OUT_OBUF[6]_inst_i_1/0
	net (fo=1, routed)	2.268	9.114	OUT_OBUF[6]
U14	OBUF (Propobuf_I_0)	3.506	12.620	r OUT_OBUF[6]_inst/0
	net (fo=0)	0.000	12.620	OUT[6]
U14			r	OUT[6] (OUT)