LAB ASSIGNMENT: 3

ES 204: DIGITAL SYSTEMS

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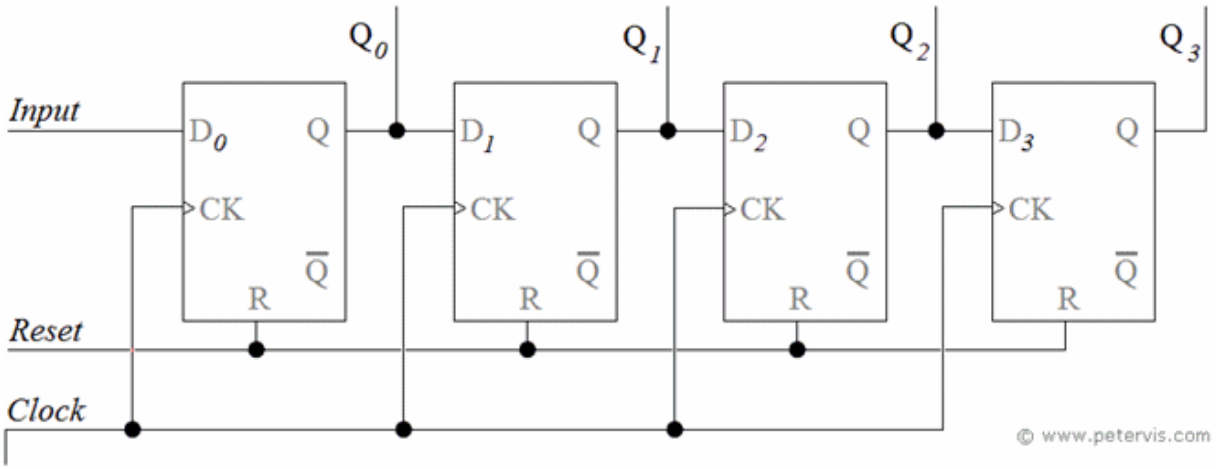
Creating a 4-bit Shift Register

A) Diagram Representation:



B) Verilog Code using Non-Blocking Assignment

```
`timescale 1ns / 1ps
module Lab3a(D, clk, Q, reset);

input D;
input clk, reset;
output reg [3:0]Q;

always @(posedge clk or posedge reset)
begin
   if (reset)
   begin
      Q[3] <= 0;
      Q[2] <= 0;
      Q[1] <= 0;
      Q[0] <= 0;
   end
   else
   begin
      Q[3] <= D;
      Q[2] <= Q[3];
      Q[1] <= Q[2];
      Q[0] <= Q[1];
```

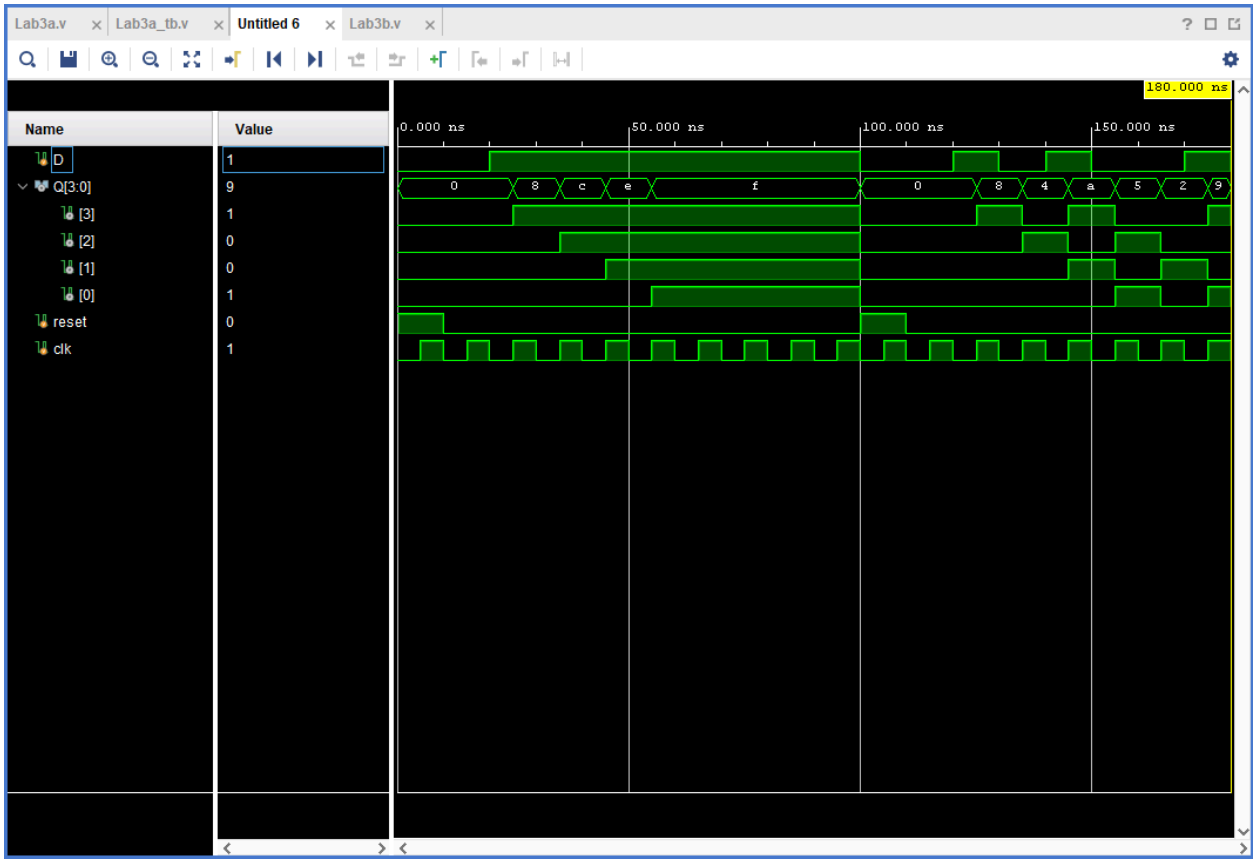
```
    end
endmodule
```

C) Test Bench Code:

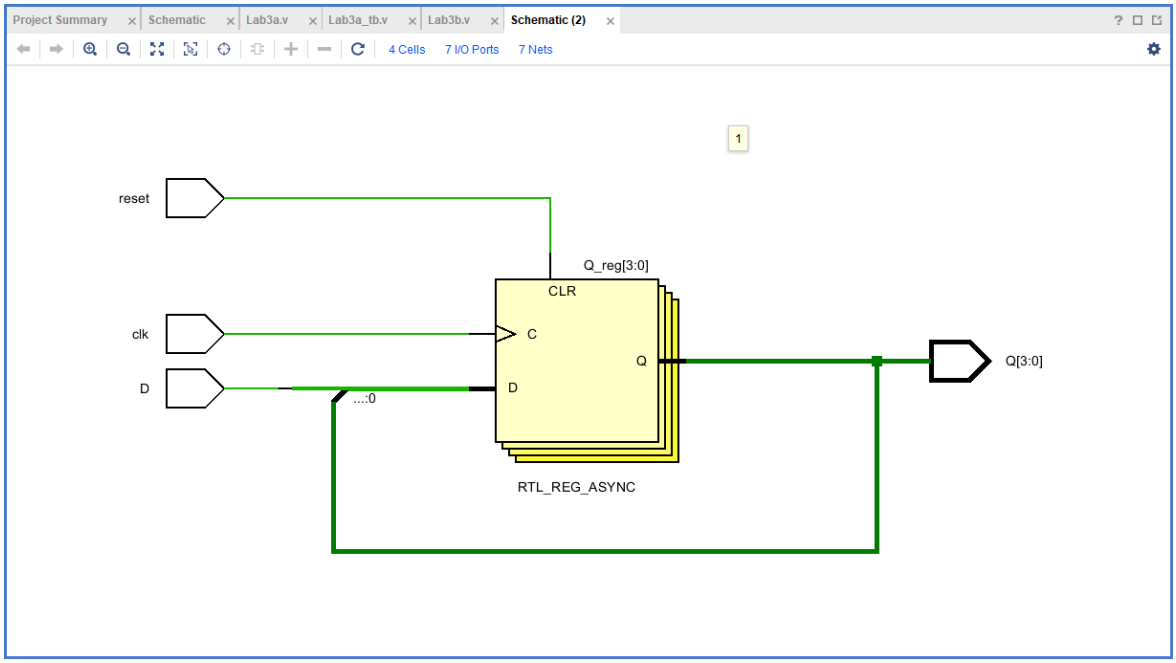
```
`timescale 1ns / 1ps
module Lab3a_tb();
reg D;
wire [3:0]Q;
reg reset;
reg clk;

Lab3a uut(D, clk, Q, reset);

initial
begin
clk = 0;
    forever #5 clk = ~clk;
end

initial
begin
    // Pattern 1
    D = 0; reset = 1;
    #10;
    D = 0; reset = 0;
    #10;
    D = 1; reset = 0;
    #80;

    // Pattern 2
    D = 0; reset = 1;
    #10;
    D = 0; reset = 0;
    #10;
    D = 1; reset = 0;
    #10;
    D = 0; reset = 0;
    #10;
    D = 1; reset = 0;
    #10;
    D = 0; reset = 0;
    #10;
    D = 0; reset = 0;
    #10;
    D = 1; reset = 0;
    #10;

    $finish();
```

```
end
endmodule
```

D) Simulation Waveform



E) Schematic Representation:



F) Verilog Code using Blocking Assignment

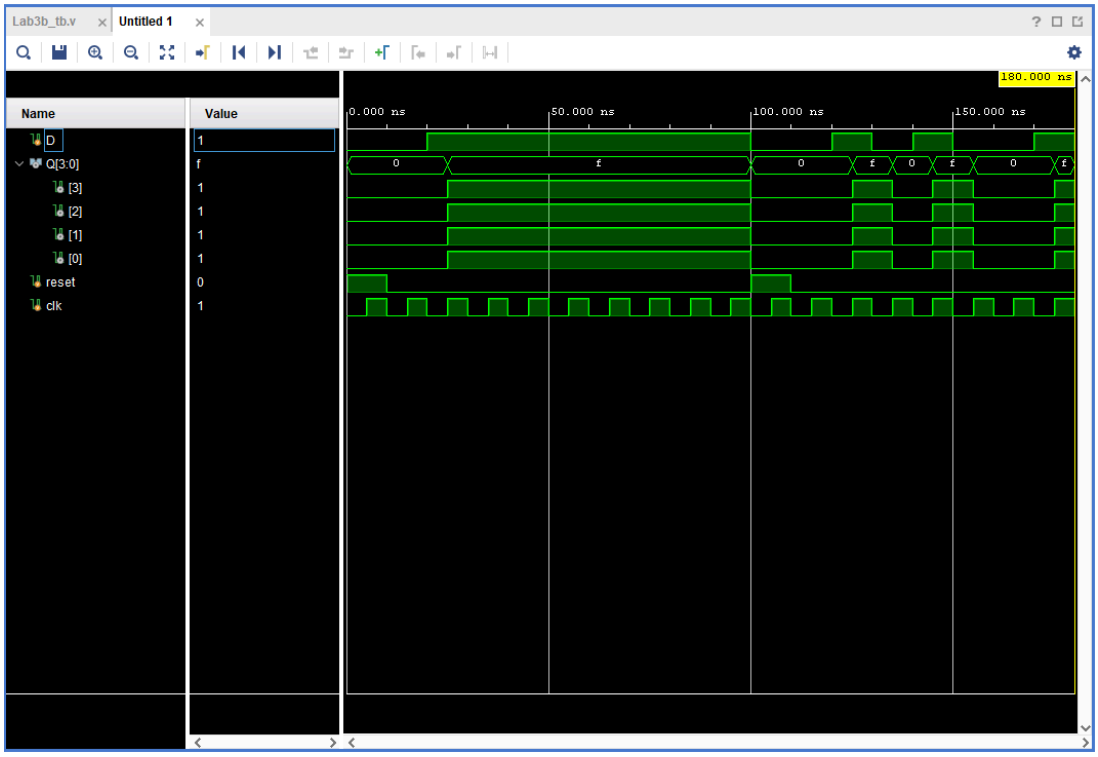
```
`timescale 1ns / 1ps

module Lab3b(D, clk, Q, reset);

input D;
input clk, reset;
output reg [3:0]Q;

always @(posedge clk or posedge reset)
begin
   if (reset)
   begin
      Q[3] = 0;
      Q[2] = 0;
      Q[1] = 0;
      Q[0] = 0;
   end
   else
   begin
      Q[3] = D;
      Q[2] = Q[3];
      Q[1] = Q[2];
      Q[0] = Q[1];
   end

end
endmodule
```

G) Test Bench Code:

```
`timescale 1ns / 1ps
module Lab3b_tb();
reg D;
wire [3:0]Q;
reg reset;
reg clk;

Lab3b uut(D, clk, Q, reset);

initial
begin
clk = 0;
   forever #5 clk = ~clk;
end

initial
begin
```

```
    // Pattern 1
    D = 0; reset = 1;
    #10;
    D = 0; reset = 0;
    #10;
    D = 1; reset = 0;
    #80;

    // Pattern 2
    D = 0; reset = 1;
    #10;
    D = 0; reset = 0;
    #10;
    D = 1; reset = 0;
    #10;
    D = 0; reset = 0;
    #10;
    D = 1; reset = 0;
    #10;
    D = 0; reset = 0;
    #10;
    D = 0; reset = 0;
    #10;
    D = 1; reset = 0;
    #10;

    $finish();
end
endmodule
```

H) Simulation Waveform



I) Schematic Representation