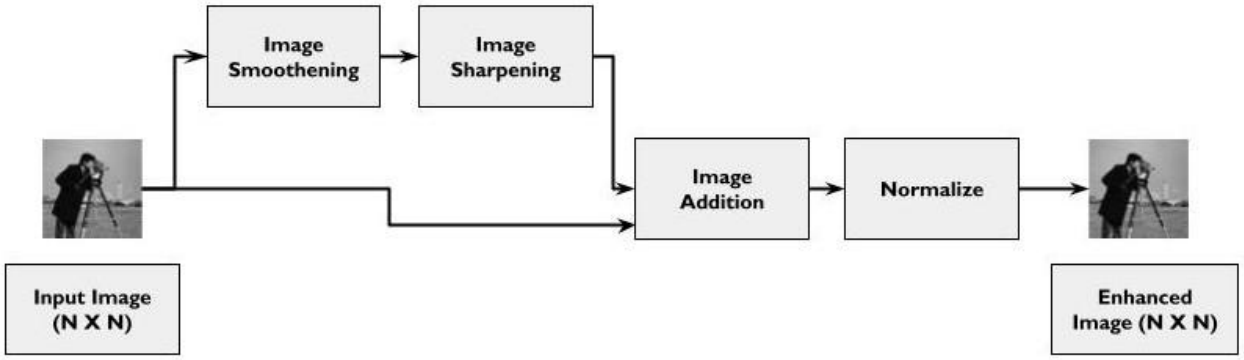
Weekly Plan Digital Systems

Image processing toolkit1

Week 1. Establish the UART communication between the system and the FPGA.

a. This can be shown by implementing a simple adder.
    i. To make a more robust reception and transmission system, the receiver and the transmitter modules will be first made separately.
    ii. Then a controller or topmodule of sorts that instantiates the receiver and transmitter module will have the adder logic.
b. The input from the user can be taken by a python program that wraps it into binary and sends the data packet to Basys3.
c. The output from the Basys3 will be again read using a python program.
d. Pyserial is the library we are going to use for making the python wrapper.

Week 2. Design an Image Enhancement hardware in Verilog. The Block Diagram is shown below. **This has to be done before Week-2.**



a. Designing the blocks individually.
b. Transferring 131072 (128*128*8) bits to the FPGA BRAM
c. Identifying a smoothening filter (3 X 3) for producing a smoothened image optimally
d. For Image Sharpening, use a 3 X 3 Laplacian Kernel. Make sure that you are handling negative numbers properly.
e. The addition of sharpened and Enhanced Image is to be performed.
f. Normalising the image pixels between 0 and 255 to get the final enhanced image.

Week 3. Looking further into the image processing toolkit operations so as to perform circle detection/identification and boundary detection. For this a deeper understanding of image processing filters/kernels and various algorithms will be needed.