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PUNJAB ENGINEERING COLLEGE (DEEMED TO BE UNIVERSITY)

End-Term Examination

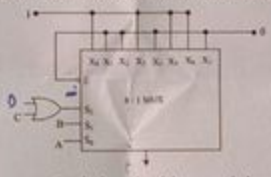
Dec, 2021

Programme: **B.E (CSE)**
Course Name: **COMPUTER ARCHITECTURE AND ORGANIZATION**
Maximum Marks: **50**

Year/Semester: **2021/5th**
Course Code: **CSN202**
Time allowed: **2 hrs.**

Notes:

- All questions are compulsory.
- Unless stated otherwise, the symbols have their usual meanings in context with subject. Assume suitably and state, additional data required, if any.
- The candidates, before starting to write the solutions, should please check the question paper for any discrepancy, and also ensure that they have been delivered the question paper of right course code.

Sr. No	Question	Marks
1.(a)	In the TTL circuit in the figure, S2 and S0 are select lines and X7 and X0 are input lines. S0 and X0 are Least Significant Bits. Give the expression for output Y. 	[6 each]
(b)	Suppose we are using 4-bit carry lookahead adder modules to build a 64-bit adder with two-level carry lookahead, with ripple carry between the modules. If the delay of a basic gate (AND, OR, NOT) is 2 nanoseconds. Find the worst-case delay of the 64-bit adder in nanoseconds.	
(c)	Suppose that a disk is rotating at a speed of 10,000 rpm, and there are 120 Kbytes of data recorded in every track. Once the disk head reaches the desired track, what is the sustained data transfer rate in Mbytes/sec.	
(d)	Let the address stored in the program counter be designated by the symbol X1. The Instruction stored in X1 has an address part (operand reference) X2. The operand needed to execute the instruction is stored in the memory word with address X3. An index register contains the value X4. What is the relationship between these various quantities if the addressing mode of the instruction is (a) direct; (b) indirect; (c) PC relative; (d) indexed?	
2.(a)	Why do we need a sequence counter and an extra decoder for it inside the basic hardwired control unit? Use diagram to support your answer.	[7 each]
(b)	A cache may be organized such that: -In one case, there are more data elements per block and fewer blocks - In another case, there are fewer elements per block but more blocks However, in both cases – i.e. larger blocks but fewer of them OR shorter blocks, but more	

	of them – the cache's total capacity (amount of data storage) remains the same. What are the pros and cons of each organization? Support your answer with a short example assuming that the cache is direct mapped.	
3. (a)	Consider a 16-way set-associative cache - Data words are 64 bits long - Words are addressed to the half-word - The cache holds 2 Mbytes of data - Each block holds 16 data words - Physical addresses are 64 bits long How many bits of tag, index, and offset are needed to support references to this cache?	[6 each]
(b)	What are the various memories that are used in computer organization? Discuss a hierarchy model covering all types of memories.	