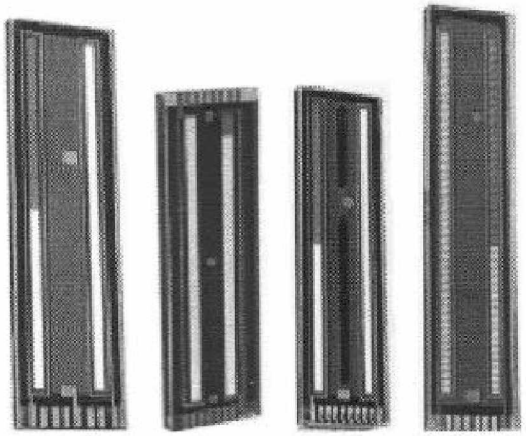
Plasma Panel Displays

Dual Linear Bar Graph



PBG- PBG- PBG- PBG-

FEATURES

- Two separate bar graphs, each including reset for 1/2% or 1% resolution (see chart)
- At normal viewing distances glow blends into continuous, but precisely controlled bar length
- Unique scanning technique minimizes the number of drivers required
- PBG-12203 bars may be scanned from either direction or both directions simultaneously
- PBG-12203 can display four separate columns of information, providing combined total of information does not exceed 201 clock counts per bar

ENVIRONMENTAL SPECIFICATIONS

Altitude: 0 to 70,000 feet.
Operating Temperature: 0°C to + 55°C.
Storage Temperature: - 55°C to + 85°C.
Relative Humidity (No Condensation): 85% maximum.
Vibration: .018 inches DA, 10 to 50 Hz, 2G, 50 to 2000 Hz.
Shock: 50G, 1/2 sine wave, 11 mS duration.

ELECTRICAL SPECIFICATIONS

OPERATING PARAMETERS	PBG-12201				PBG-12203				PBG-12205				PBG-16101			
Parameter	Min.	Max.	Rec.	Units	Min.	Max.	Rec.	Units	Min.	Max.	Rec.	Units	Min.	Max.	Rec.	Units
Anode Supply Voltage	235	265	250	V	235	265	250	V	235	265	250	V	235	265	250	V
Cathode Off Bias Voltage	68	76	72	V	68	76	72	V	68	76	72	V	68	76	72	V
Anode Off Bias Voltage	80	120	100	V	80	120	100	V	80	120	100	V	80	120	100	V
Anode Sustaining Voltage (Typical)	—	—	150	V	—	—	150	V	—	—	150	V	—	—	150	V
Refresh Rate	—	—	70	Hz	—	—	70	Hz	—	—	70	Hz	—	—	70	Hz
Keep Alive Anode Resistor	—	—	1M	Ω	—	—	1M	Ω	—	—	1M	Ω	—	—	1M	Ω
Keep Alive Cathode Resistor	—	—	1M	Ω	—	—	1M	Ω	—	—	1M	Ω	—	—	1M	Ω
Keep Alive Current (Typical)	—	—	50	µA	—	—	50	µA	—	—	50	µA	—	—	50	µA
Display Anode Resistor	—	—	36k	Ω	—	—	24k	Ω	—	—	24k	Ω	—	—	20k	Ω
Display Peak Anode Current	2.5	3.0	2.8	mA	3.7	4.5	4.2	mA	3.5	5.0	4.0	mA	4.0	6.0	5.0	mA
Scan Time per Cathode	70	90	70	µS	70	90	70	µS	60	90	70	µS	120	180	140	µS
Applied Reset Pulse Width	140	180	140	µS	140	180	140	µS	70	180	140	µS	120	180	140	µS

OPTICAL SPECIFICATIONS

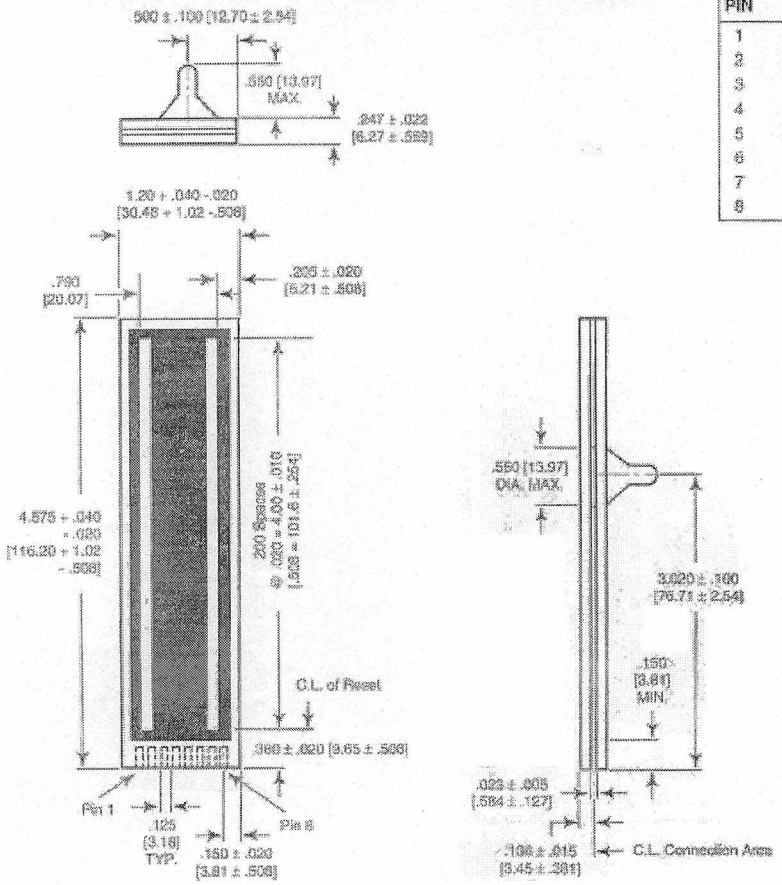
	PBG-12201	PBG-12203	PBG-12205	PBG-16101
Elements	201	203	201	101
Resolution	1/2%	1/2%	1/2%	1%
Segment Length	.100"	.150"	.100"	.100"
Segment Width	.011"	.010"	.011"	.020"
Segment Spacing	.020"	.020"	.020"	.050"
Drivers Required	6	12	8	6
Luminance	35 fl	30 fl	70 fl	60 fl
Viewing Angle	120°	120°	120°	120°
Color	Neon Orange	Neon Orange	Neon Orange	Neon Orange

Document Number: 37027
Revision 08-Nov-00

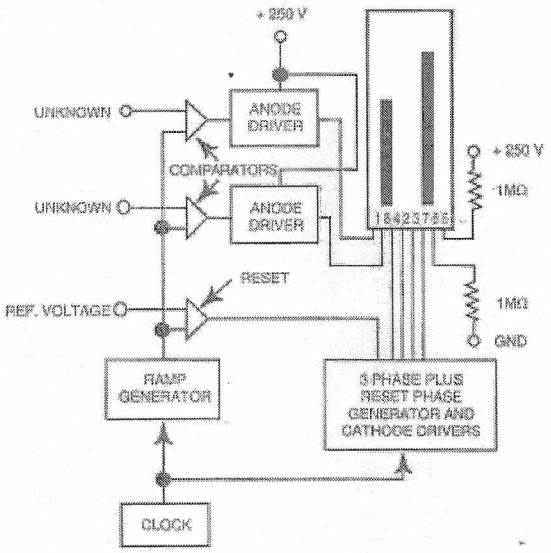
DIMENSIONAL CONFIGURATIONS [Numbers in brackets indicate millimeters]

PBG-12201

PIN	CONNECTION
1	Channel No. 1 Anode
2	Phase 1 Cathode
3	Phase 3 Cathode
4	Reset Cathode
5	Keep Alive Anode
6	Keep Alive Cathode
7	Phase 2 Cathode
8	Channel No. 2 Anode



Block Diagram of Typical Drive Circuit



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United States Patent [19]

Schoenfeld et al.

[11] 4,078,252

[45] Mar. 7, 1978

[54] RAMP GENERATOR

[75] Inventors: Simon L. Schoenfeld; Eugene C. Coussens, both of San Jose, Calif.

[73] Assignee: Signetics Corporation, Sunnyvale, Calif.

[21] Appl. No.: 757,767

[22] Filed: Jan. 10, 1977

Related U.S. Application Data

[63] Continuation of Ser. No. 602,570, Aug. 7, 1975, abandoned.

[51] Int. Cl.² G06F 15/34; H03K 1/14

[52] U.S. Cl. 364/858; 307/264; 307/269; 364/518; 364/829

[58] Field of Search 235/150.53, 183, 197; 328/181, 185; 307/246, 294, 264–269

[56] References Cited

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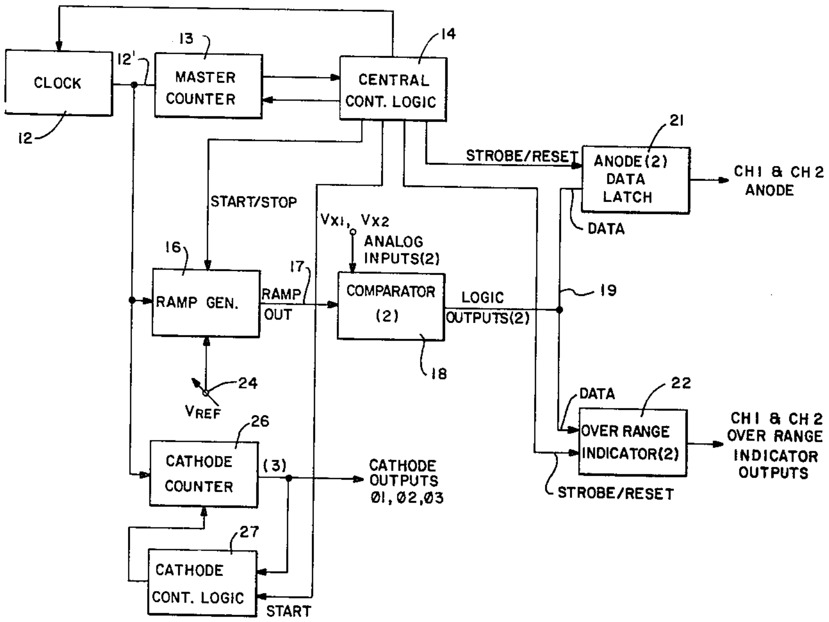
Primary Examiner—Malcolm A. Morrison
Assistant Examiner—Errol A. Krass
Attorney, Agent, or Firm—C. Richard Pfeiffer; William H. Dana; Jerry A. Dinardo

[57] ABSTRACT

A ramp generator for driving a bar graph display which utilizes a feedback circuit to set its maximum level of the ramp.

4 Claims, 5 Drawing Figures



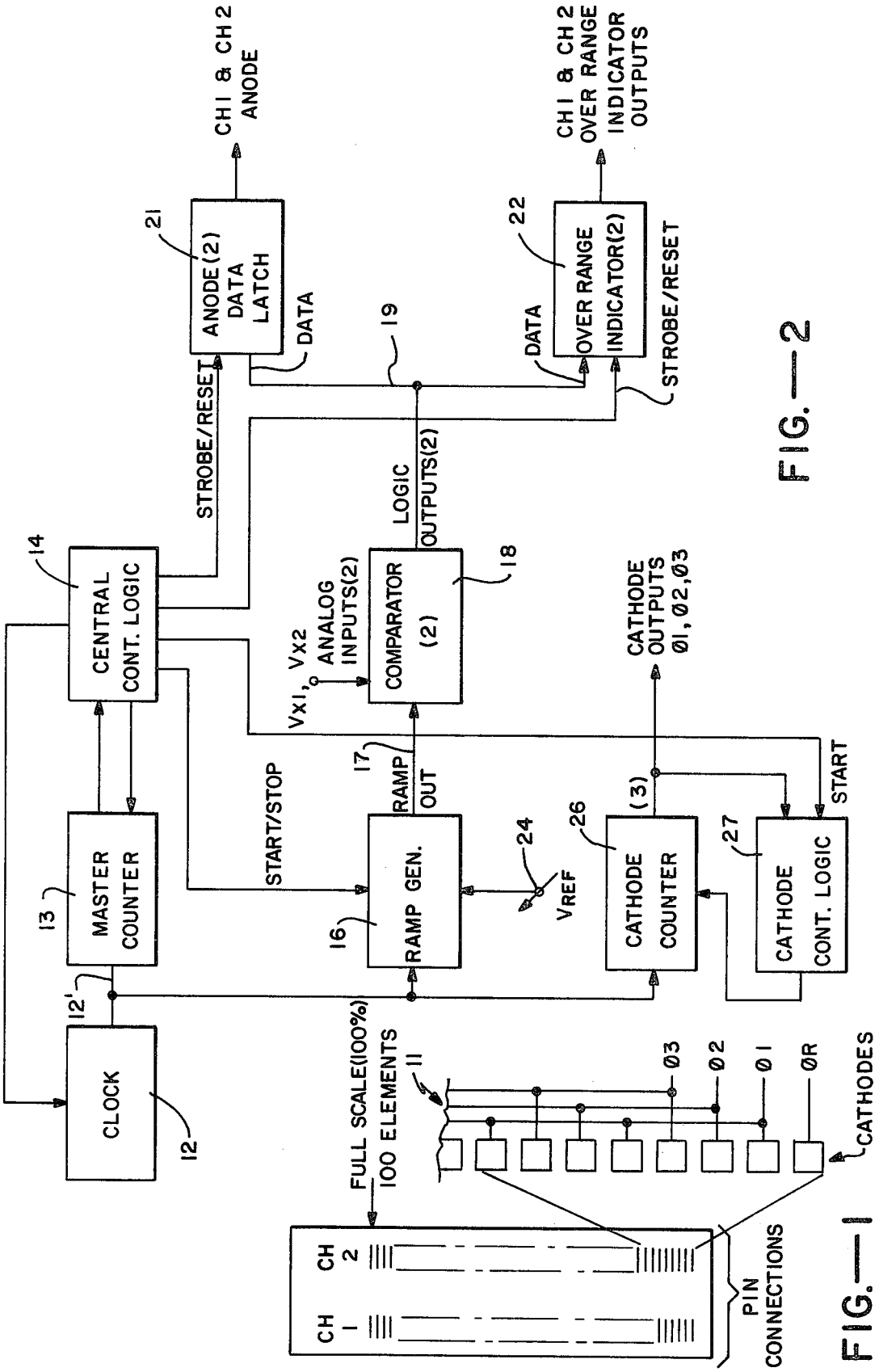


FIG.—2

FIG.—1

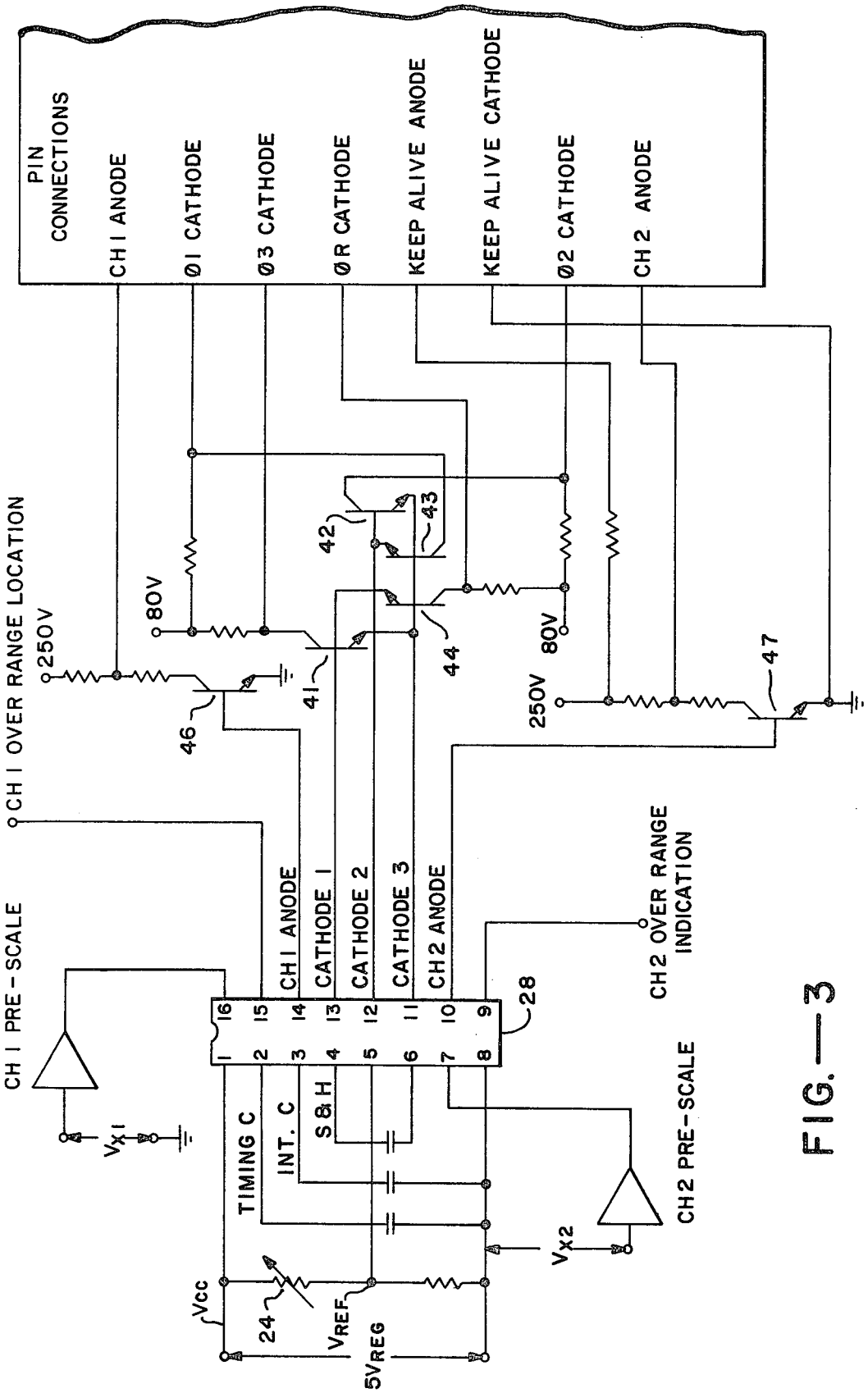

PIN CONNECTIONS
CH 1 ANODE
Ø1 CATHODE
Ø3 CATHODE
ØR CATHODE
KEEP ALIVE ANODE
KEEP ALIVE CATHODE
Ø2 CATHODE
CH 2 ANODE
CH 1 OVER RANGE LOCATION
250V
80V
80V
250V
42
43
44
41
46
47
CH 1 PRE-SCALE
CH 2 OVER RANGE INDICATION
CH 1 ANODE
CATHODE 1
CATHODE 2
CATHODE 3
CH 2 ANODE
28
TIMING C
INT. C
S & H
VX1
VX2
CH 2 PRE-SCALE
Vcc
24
VREF
5VREG

FIG. — 3

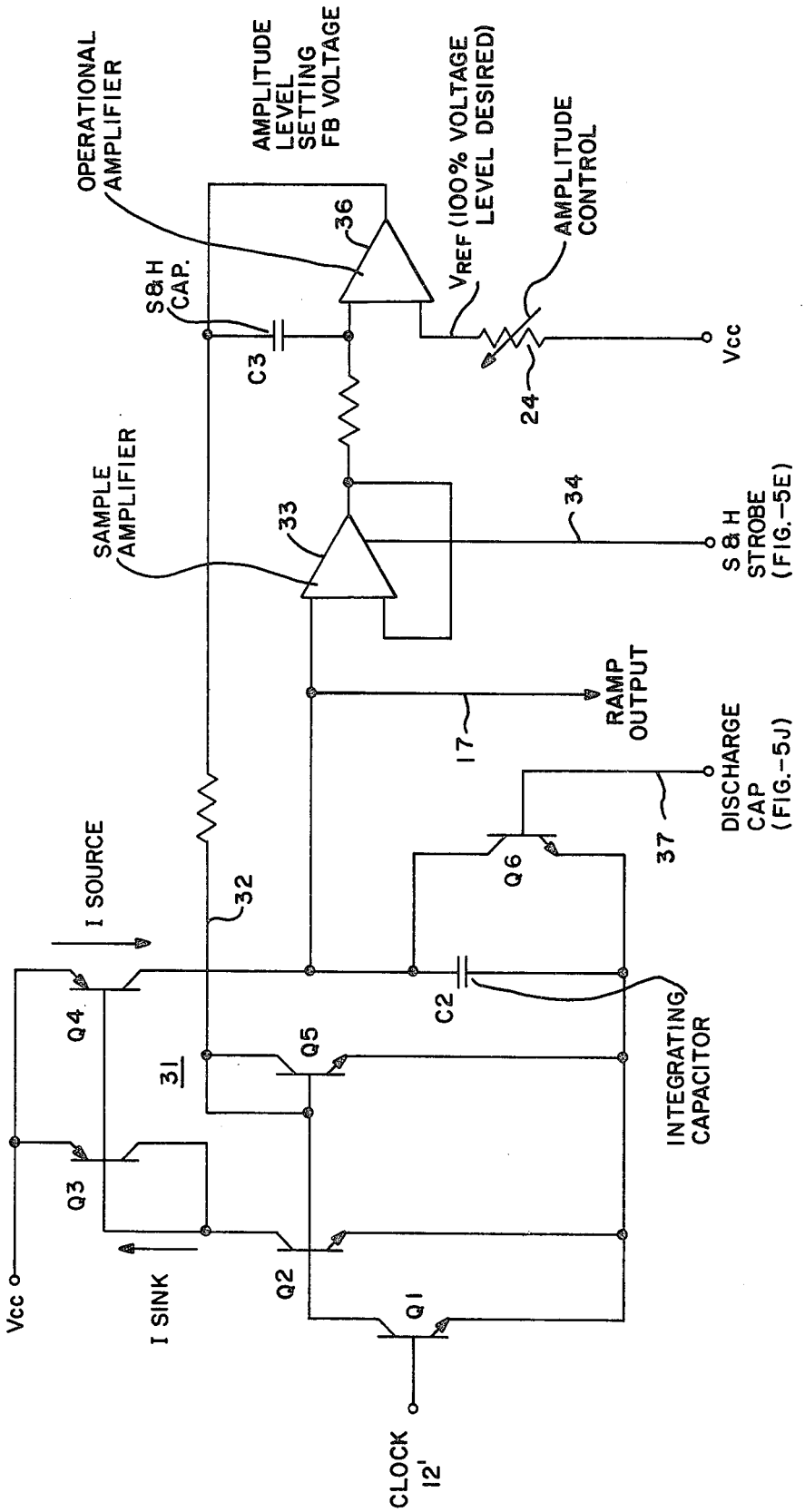

OPERATIONAL AMPLIFIER
AMPLITUDE LEVEL SETTING FB VOLTAGE
VREF (100% VOLTAGE LEVEL DESIRED)
AMPLITUDE CONTROL
S&H CAP.
36
C3
24
Vcc
SAMPLE AMPLIFIER
33
34
S & H STROBE (FIG.-5E)
RAMP OUTPUT
17
DISCHARGE CAP (FIG.-5J)
37
Q6
I SOURCE
32
Q4
C2
INTEGRATING CAPACITOR
Q5
31
Q3
Vcc
I SINK
Q2
Q1
CLOCK
12'

FIG.—4

Time for full scan = (1/70Hz)*103 = 1,47s

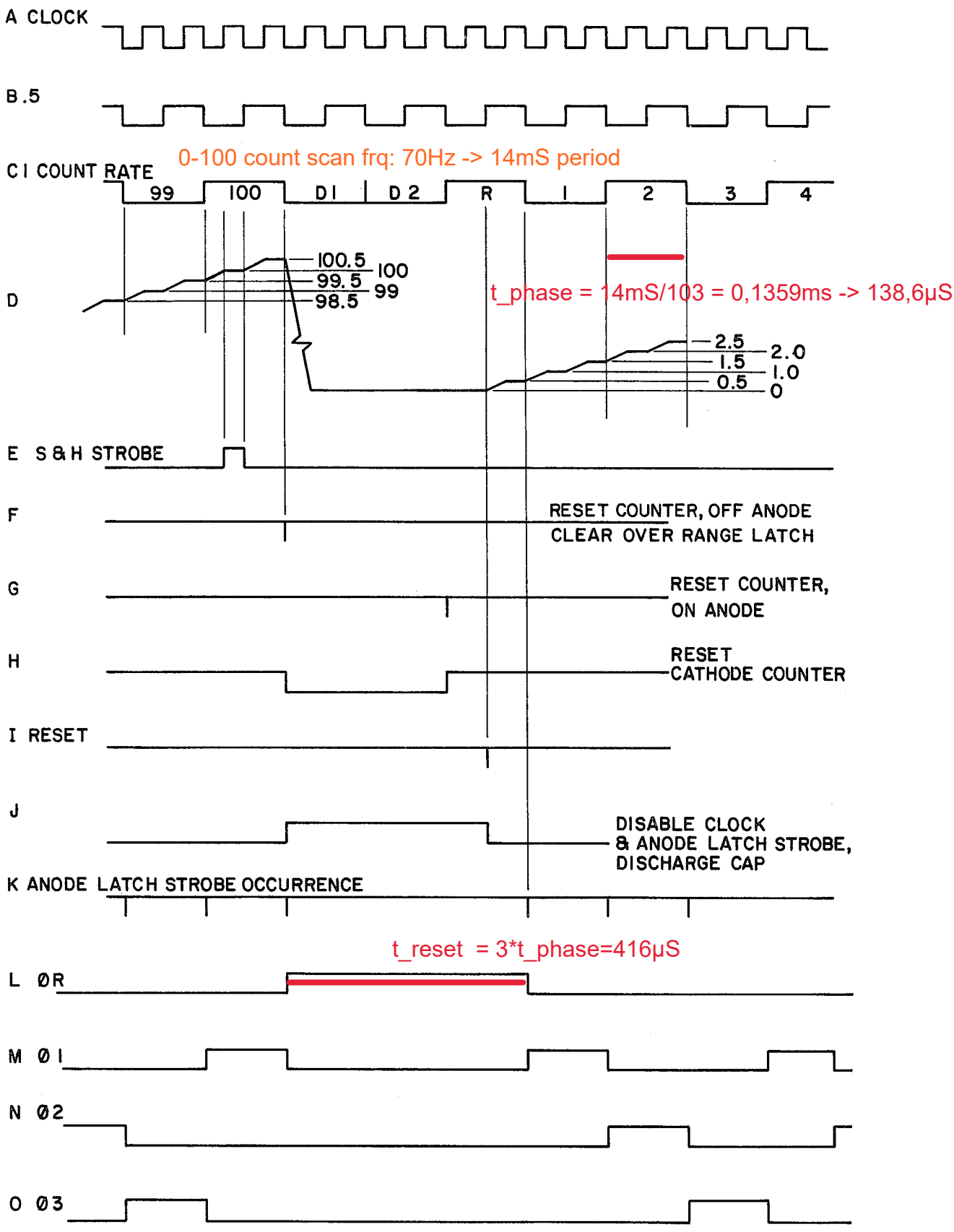


FIG.—5

RAMP GENERATOR

This is a continuation, of application Ser. No. 602,570 filed Aug. 7, 1975, and now abandoned.

BACKGROUND OF THE INVENTION

The present invention is directed to a ramp generator and more particularly to a ramp generator for use in a signal processing system for a bar graph display.

In a typical bar graph display as shown in FIG. **1**, two separate bar graphs #**1** and #**2**, have **100** elements. These elements are in actuality gas tubes which may be activated to produce a glowing or illuminated bar length which is proportional to an unknown analog input signal. The display elements are activated by a three phase system indicated at **11** where in the scanning mode of, for example, 70 hertz or greater the three phases are successively activated. A particular segment or element can only be activated if the previous element has already been activated. Thus, the display will produce at a normal viewing distance a continuous but precisely controlled bar length. The display anodes are switched on and off at an appropriate clock count to determine the heighth of the bar. Such switching is determined by comparing the unknown analog signal with a reference voltage ramp.

All of the foregoing is produced and sold by the Burroughs Corporation, Electronic Component Division, P.O. Box 1226, Plainfield, New Jersey 07061.

One of the difficulties in the foregoing circuit is the ramp generator. Normally, the generator must be frequently calibrated and other efforts must be made to insure its accuracy. In the case of an integrating circuit where tolerance variations must be accommodated, it is very difficult ot economically construct a sufficient ramp generator.

OBJECTS AND SUMMARY OF THE INVENTION

It is, therefore, a general object of the present invention to provide a ramp generator which is especially suited for integration.

It is another object of the invention to provide an integrated ramp generator which is suitable for driving a bar graph display.

In accordance with the above objects there is provided a ramp generator with a clock. A constant current source has an output signal turned on and off by the clock and includes means for adjusting the magnitude of the output signal. An integrating capacitor is connected to the current source and integrates the output signal to produce a voltage ramp. Sample and hold means sample and hold the voltage ramp at a time determined by a predetermined clock count and compare the held votage with a reference voltage to produce an error signal indicating a lack of comparison. Adjusting means are coupled to the sample and hold means and are responsive to the error signal for changing the magnitude of the current output signal to minimize the error signal. Means are responsive to the predetermined count for discharging the capacitor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view of a bar graph display;

FIG. **2** is a block diagram of the signal processing system for driving the display of FIG. **1**;

FIG. **3** shows the novel integrated circuit of the present invention along with suitable circuits for interfacing to the bar graph of FIG. **1**;

FIG. **4** is a more detailed circuit schematic of a ramp generator shown in FIG. **2**; and

FIGS. **5A** through **5O** is a timing diagram useful in understanding the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The bar graph of FIG. **1** has alread been discussed in conjunction with the prior art. Moreover, the pin connections at the lower portion of the figure will be discussed in conjunction with FIG. **3**.

FIG. **2** is a generalized block diagram of the driving circuit for the bar graph of FIG. **1** and comprises a clock **12** for driving a master counter **13** which in turn drives a central control logic unit **14**. The ramp generator **16** is activated by the control logic unit **14** to produce a voltage ramp output signal on line **17** which is connected to a comparator **18**. The comparator compares a pair of unknown analog voltage inputs V_{X1} and V_{X2} and upon comparison produces a pair of logic outputs on lines **19**. These are coupled to a pair of anode data latches **21** which drive channel **1** and channel **2** anodes of the bar graph display. If no comparison results, over range indicators **22** are activated.

Ramp generator **16** has its reference voltage adjusted by a variable input **24** in accordance with the maximum full scale analog signal V_{X1} and V_{X2} which is to be received. Cathode counter **26** in conjunction with cathode control logic unit **27** provides three cathode outputs which sequentially drive the bar graph display of FIG. **1** as discussed above.

The interface between the display drive and the bar graph is shown. In FIG. **3** all of the components of FIG. **2** are contained in the integrated circuit package **28**. As is apparent it has channel **1** and channel **2** anode outpus, three cathode outputs ϕ**1**, ϕ**2** and ϕ**3** and channel **1** and channel **2** Over Range Indicators. From an input standpoint the unkown voltages V_{X1} and V_{X2} are applied to channel **1** and channel **2** inputs through external prescale amplifiers. $V_{reference}$ is obtained by the use of the potentiometer **24** which utilizes the regulated **5** volt V_{cc}. Lastly, various timing capacitors, integrating capacitors and sample and hold capacitors are externally connected to circuits which will be described in detail in FIG. **4**. The three phase cathode outputs, Q**1-3**, provide coded timing information which is decoded by external base-emitter diodes of cathode drive transistors **41–44** to provide the timing as indicated by the collector waveform shown in FIGS. **5**L, M, N and O. The channel **1** and channel **2** anode outputs provide the drive to the high voltage interface transistors **46** and **47**.

FIG. **4** illustrates the specific details of the ramp generator **16** in accordance with the present invention. Clock input **12**′ drives constant a current source **31** which is of the current mirror type. It has an input transistor Q**1** which is response to an on condition of the clock signal inhibits I_{sink} current through transistor Q2 and diode connected transistor Q3 by pulling the base of transistors Q2 and Q5 below their level of operation. I_{sink} is the reflection of current in Q5. Such current is reflected at V_{cc} as I_{source} through the transistor Q4, which has its base connected to Q3, by the current mirror effect. I_{source} is coupled to integrating capacitor C2 which produces a voltage ramp output on the line **17** (see FIG. **2**). The constant current source **31** also in-

cludes means for adjusting the magnitude of the I_{sink} and I_{source} by means of a diode connected transistor Q5 which has its base in common with the base of Q2. Thus, the level of the voltage signal on collector line **32** affects the amplitude of the current source.

Ramp output line **17** is connected to sample and hold means which include a sample amplifier **33** which samples as determined by the strobe input on line **34**. The output of amplifier **33** or the sampled signal is stored in sample and hold capacitor C3, the sampled signal drives the operational amplifier **36**. Such amplifier acts as a comparator to compare the sampled ramp voltage on capacitor C2 to a reference voltage, V_{ref}, produced by amplitude control unit **24** to produce on line **32** a feedback voltage which tends to minimize any error.

Lastly, the discharge capacitor input control line **37** activates a transistor Q6 to short out integrating capacitor C2 and in essence dump its charge at an appropriate time in the sequence.

FIGS. **5**A through **50** illustrate the timing of all of the foregoing. The clock frequency of clock **12** is indicated at FIG. **5**A, is partially divided at **5**B and finally at **5**C is shown the count rate which corresponds to the number of segments of the display. It is also one-half the clock frequency. This clock rate is provided by a divider, referring to FIG. **2**, in the central control logic unit **14**. Typical ramps are indicated in FIG. **5**D. The end of one ramp is indicated as occurring at 100 or more accurately 100.5 and the beginning of a second ramp is indicated starting at zero and going to 2.5 in relation to FIG. **5**C. By use a clock count as in FIG. **5**A which is double the number of segments, comparison decisions can be made in an intermediate point on the ramp as shown by the sample and hold strobe of FIG. **5**E (the input **34** of FIG. **4**).

At the predetermined count of **100** shown in FIG. **5**C a general resetting of all circuits occurs since the ramp has reached its full scale value. Thus, in FIG. **5**F the falling edge of FIG. **5**C causes a reset pulse to reset the master counter **13** (FIG. **2**), the over range indicator circuit **22** and causes the anode channel to switch an off condition. FIG. **5**H shows a reset of the cathode counter **26**; in FIG. **5**J the clock **12** is disabled along with the anode latch strobe and in addition the integrating capacitor is discharged as illustrated by the input **37** of FIG. **4**. FIG. **5**K illustrates the occurrence of the anode latch strobe at the count rate and how it is inhibited as illustrated in FIG. **5**J during the deadtime D1, D2. Lastly, FIG. **5**L indicates that only the reset phase (see FIG. **1**) of the bar graph is activated in the deadtime but in view of no anode voltage there cannot be any illumination.

Initiation of the next succeeding ramp occurs after the deadtimes D1 and D2 illustrated in FIG. **5**C by the reset period R which is provided by the central control logic unit **14**. The leading edge of this period causes the reset pulse of **5**G which again resets the master counter **13**. The cathode counter is also reset as shown in FIG. **5**H. One half period later in FIG. **5**I a reset pulse is produced which activates circuitry such as a flip-flop (not shown) as illustrated in FIG. **5**J to enable the clock and anode latch strobe and disable the discharge capacitor circuit. Thus as shown in FIG. **5**K the anode voltage is again applied to produce illuminated bar segments. Also at this time the C1, **2** and **3** scanning signals of FIGS. **5**M, N and O are allowed to sequence.

The ramp generator of FIG. **4** in operation provides a circuit of the type which may be easily integrated as shown by the package **28** of FIG. **3**. This is true because of the noncriticality of the components in view of the feedback circuits used to set the maximum level of the ramp. The ramp being produced in this manner dramatically corrects for temperature variations and excessive tolerance variations. The only critical portion is that the reference voltage must be carefully controlled. Also the reference voltage would be adjusted for each specific full scale voltage range desired.

The clock frequency of clock **12** is also adjusted for the particular number of segments of a bar graph display. Thus, for a **200** segment display its frequency would be doubled.

What is claimed is:

1. A ramp generator system providing an output proportional to an analog signal input comprising a clock having a predetermined frequency, a constant current source having an ouput signal turned on and off by said clock, said source including means for adjusting the magnitude of said output signal, an integrating capacitor connected to said current source and integrating said output signal to produce a voltage ramp, sample and hold means for sampling and holding said voltage ramp at a time determined by a predetermined clock count and for comparing said held voltage amplitude with a reference voltage input amplitude to produce an error signal defined by the difference in the respective amplitudes, said adjusting means being coupled to said sample and hold means and responsive to said error signal for changing said magnitude of said current source output signal to minimize said error signal, and means responsive to said predetermined count for discharging said capacitor.

2. A signal processing system for a bar graph display having a predetermined number of elements which displays an analog input signal as a proportional bar length and includes a ramp generator providing an output proportional to a reference voltage input and a comparator for comparing said analog signal to said ramp generator output for activating a corresponding number of said elements, said ramp generator comprising a clock having a predetermined frequency, a constant current source having an output signal turned on and off by said clock, said source including means for adjusting the magnitude of said output signal, an integrating capacitor connected to said current source and integrating said output signal to produce a voltage ramp, sample and holding means for sampling and holding said voltage ramp at a time determined by a predetermined clock count and for comparing said held voltage amplitude with the reference voltage input amplitude to produce an error signal defined by the difference in the respective amplitude, said adjusting means being coupled to said sample and hold means and responsive to said error signal for changing said magnitude of said current output signal to minimize said error signals, and means responsive to said predetermined count for discharging said capacitor.

3. A system as in claim **2** where said predetermined clock count is directly proportional to said predetermind number of elements.

4. A system as in claim **3** where said clock count is twice said number of elements.

* * * * *

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Bar Graph Products

DESIGNER'S GUIDE

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INTRODUCTION

This manual provides controller design information pertaining to four standard Dale bar graphs: PBG-16101, PBG-12201, PBG-12205 and PBG-12203. A typical drive circuit is included to illustrate the type of interface required and to act as an aid in initial product evaluation.

To simplify understanding of the interface requirements a brief description of bar graph construction and operation is included.

TERMINOLOGY

To minimize confusion in the descriptions contained in this manual the following terminology will be used:

Bar Graph — Refers to the complete product — the glass envelope and its contents.

Channel — Refers to one display column of a bar graph. Some bar graphs have more than one channel.

Bar — Refers to one element of a channel. A channel has typically 100 or more bars.

CONSTRUCTION AND OPERATION

Dale bar graphs combine advanced thick film manufacturing technology with a patented internal addressing technique. This provides high reliability and minimized drive circuitry requirements.

Bar graphs consist of a rear glass substrate on to which is screen printed individual conductive cathode elements for each channel. These cathodes are bussed internally in groups of 3 or 5, dependent on the particular model. The groups are known as phases. A black dielectric is then applied to improve contrast.

A further piece of the unit, the front plate, has two transparent anodes applied, each covering the entire surface of a given channel area. The two pieces of glass are placed together, sealed and filled with neon gas. This provides a soft-orange glow when illuminated.

Figure 1 shows the construction of the linear bar graph.

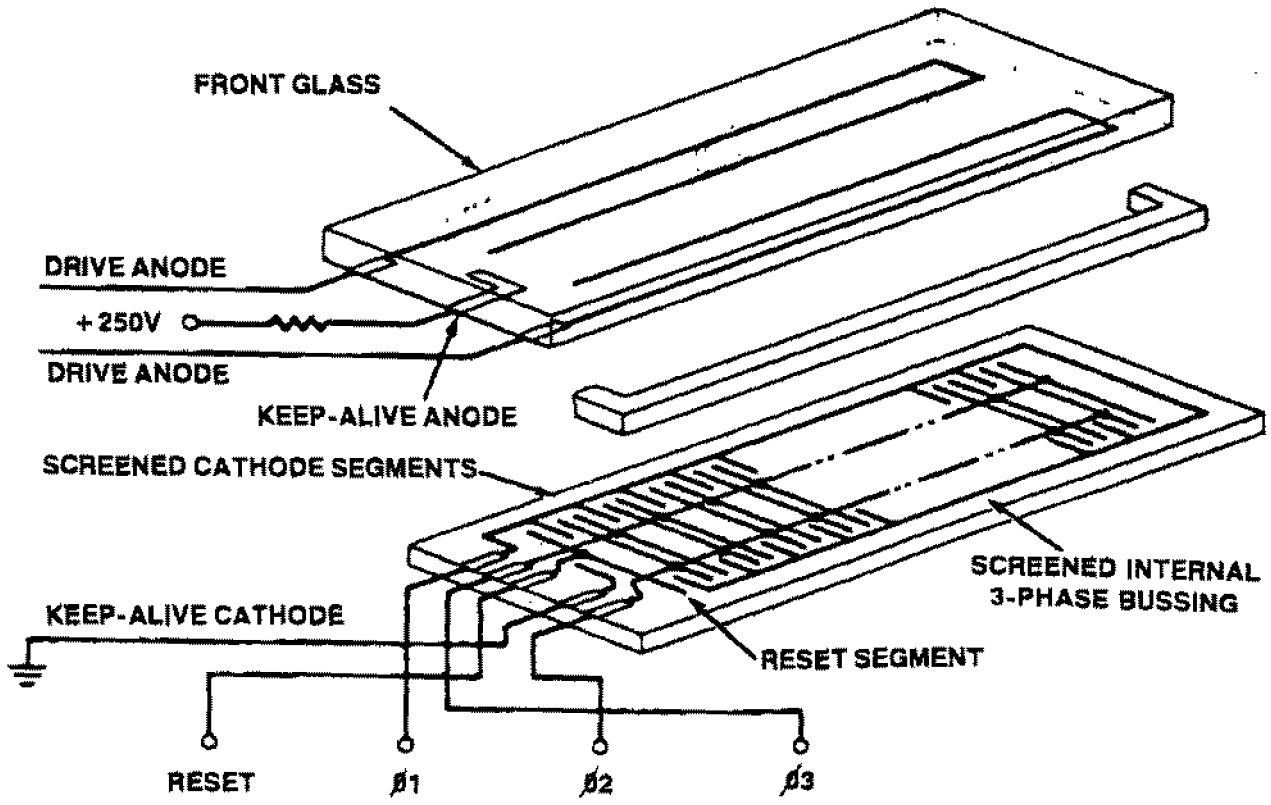

Figure 1: LINEAR BAR GRAPH CONSTRUCTION

The bar graphs operate on a patented principle known as Glow Transfer. This employs the use of grouped cathodes, each group being called a phase. A phase is formed by internally connecting every Nth cathode. Depending on the bar graph style, N can have value 3 or 5. Discharge occurs between a negative cathode and the positively charged anode.

Located at one end of the panel is a pair of electrodes known as a "keep alive." For models addressable from either end a "keep alive" is provided at each end. "Keep alives" are not visible from the front of the panel but are used to produce the initial ionization in a scan sequence. They are permanently ionized when the tube is operating.

To commence a scanning sequence, a non-bussed cathode, the reset cathode, is energized to a negative potential. The reset cathode is located close to the ionized "keep alive" and thus also becomes ionized. After a period of time, known as the reset duration, each cathode bus (phase) is sequentially energized by placing it at a negative potential and by returning all other phases to any off bias potential (voltage too low to sustain an ionization). The ionization is therefore established on each phase in sequence. In practive only one cathode on a phase is ever ionized at any one time. This is because immediately one cathode becomes ionized and the potential on the phase drops to a level which is too low to ionize any further cathodes. Further, the cathode which does ionize is always adjacent to the one last previously ionized on the adjacent phase. This feature is the unique principle of Glow Transfer and occurs because the concentration of ionized particles around a cathode is always greater when it is close to another cathode that has just been ionized. These particles speed up the ionization of that particular cathode and cause it to ionize before any other on the same bus. The ionization thus proceeds up or down the tube as each cathode bus is sequentially energized.

Only one bar of information is illuminated at any instant of time but the scan cycle is repeated many times per second. Due to the persistance of human vision the scan appears as a flicker-free display.

An obvious advantage of this principle is the large reduction in the number of external connections and drivers required. The number of cathode drivers is reduced to N + 1 giving a very significant improvement in cost and reliability.

GENERAL PRODUCT INFORMATION

Each linear bar graph contains two independent channels. There is a separate anode for each channel to allow independent channel control.

Bar graphs have three or five phases.

One hundred or 200 bars per channel are provided, depending on the model. These give a resolution of 1% or ½% respectively.

Use of the Glow Transfer internal addressing system minimizes both the number of connections and the number of electronics drivers required.

FUNCTIONAL CHARACTERISTICS

Functional characteristics for each model are shown in **Table 1.**

Table 1. FUNCTIONAL CHARACTERISTICS

Bar Graph	No. of Channels Per Device	No. of Display Elements/Channel	No. of Phases
PBG-16101	2	100	3
PBG-12201	2	200	3
PBG-12205	2	200	5
PBG-12203	2	201	3

ELECTRICAL CHARACTERISTICS

Design Information			PBG-16101			PBG-12201			PBG-12205			PBG-12203		
PARAMETER	SYM	UNIT	MIN	REC	MAX	MIN	REC	MAX	MIN	REC	MAX	MIN	REC	MAX
Supply Voltage	E_S	V_{DC}	235	250	265	235	250	265	235	250	265	235	250	265
Supply Current	—	mA	10	15	20	10	15	20	10	15	20	10	15	20
Keep Alive Anode Resistor	R_{KA}	Mohm	0.9	1.0	1.1	0.9	1.0	1.1	0.9	1.0	1.1	.95	1.0	1.05
Keep Alive Cathode Resistor	R_{KA}	Mohm	—	—	—	—	—	—	—	—	—	.95	1.0	1.05
Keep Alive Current	I_{KA}	μA	—	100	—	—	100	—	—	100	—	—	50	—
Display Anode Current Limiting Resistor	R_D	Kohm	19.0	20.0	21.0	34.2	36.0	37.8	22.8	24.0	25.2	22.8	24.0	25.2
Display Anode Current	I_D	mA	4.0	5.0	6.0	2.5	2.8	3.0	3.5	4.2	5.0	3.7	4.2	4.5
Display Anode Sustaining Voltage	V_D	VDC	—	150	—	—	150	—	—	150	—	—	150	—
Cathode Off Bias Voltage	E_{KO}	VDC	68	72	76	68	72	76	68	72	76	68	72	76
Display Anode Off Bias Voltage	E_{BO}	VDC	80	100	120	80	100	120	80	100	120	80	100	120
Refresh Rate	f_r	Hz	—	70	—	—	70	—	—	70	—	—	70	—
Cathode Scan Time	t_s	μS	120	140	180	70	70	90	60	70	90	70	70	90
Applied Reset Pulse Width	t_r	μS	120	140	180	140	140	180	70	140	180	140	140	180

OPTICAL CHARACTERISTICS

Color — Neon Orange

Display Uniformity — The light output of individual cathodes appears uniform to the unaided eye when viewed from a distance greater than 24 inches.

Light Output — The typical time-averaged luminous intensity per cathode operating at the recommended conditions is per the following table:

Device	Luminance (ft. L)
PBG-16101	60
PBG-12201	35
PBG-12205	70
PBG-12203	30

Viewing Angle — 120° included horizontal viewing angle (bar graph mounted vertically).

ENVIRONMENTAL CHARACTERISTICS

Ambient Operating Temperature — 0°C to 55°c

Storage Temperature — -40°C to 85°C

Altitude — 70,000 feet maximum

Vibration — .018 inch D.A., 10 to 50 Hz 2g, 50 to 2000 Hz

Shock — 50g, ½ sinewave, 11 ms duration

Humidity — 85 percent maximum (no condensation)

MECHANICAL CONFIGURATION

Dimensions for each bar graph model are shown in the following figures:

PBG-16101 — figure 2
PBG-12201 — figure 3
PBG-12205 — figure 4
PBG-12203 — figure 5

PIN CONNECTORS

Pin	Connection
1	Channel No. 1 Anode
2	Phase 1 Cathode
3	Phase 3 Cathode
4	Reset Cathode
5	Keep Alive Anode
6	Keep Alive Cathode
7	Phase 2 Cathode
8	Channel No. 2 Anode

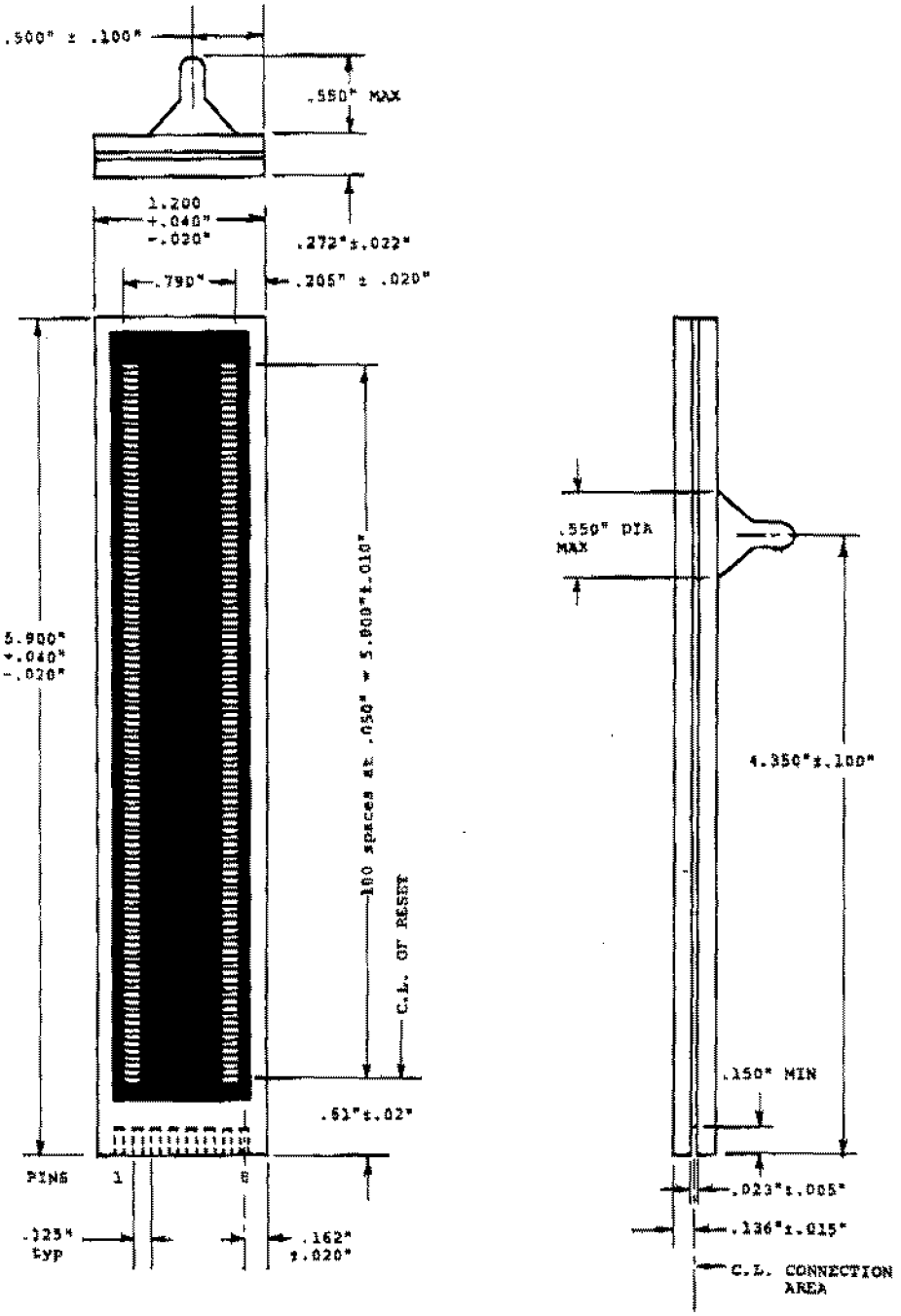

Figure 2: PBG-16101 OUTLINE DRAWING

PIN CONNECTORS

Pin	Connection
1	Channel No. 1 Anode
2	Phase 1 Cathode
3	Phase 3 Cathode
4	Reset Cathode
5	Keep Alive Anode
6	Keep Alive Cathode
7	Phase 2 Cathode
8	Channel No. 2 Anode

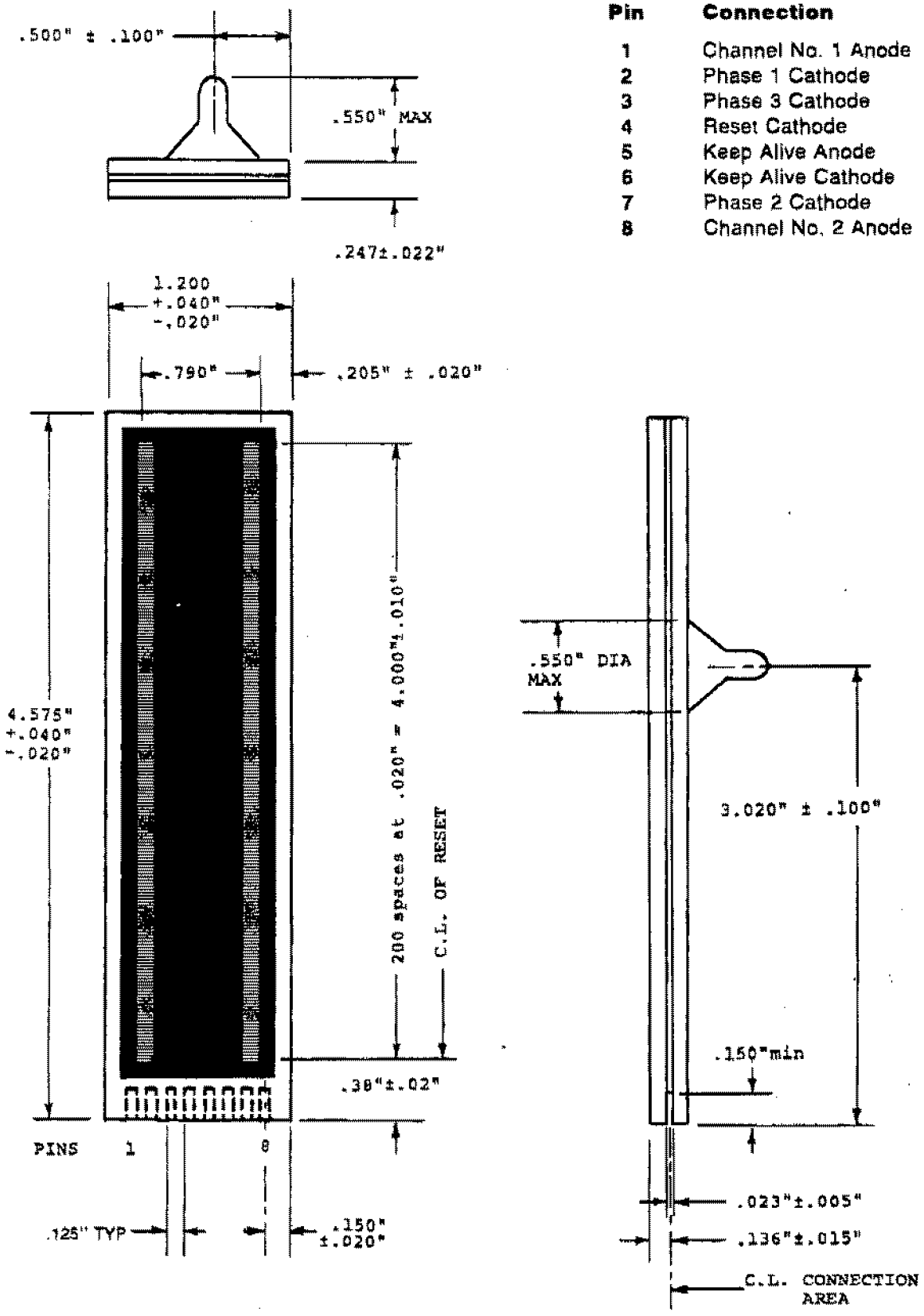

Figure 3: PBG-12201 OUTLINE DRAWING

PIN CONNECTORS

Pin	Connection
1	Channel No. 1 Anode
2	Phase 2 Cathode
3	Phase 1 Cathode
4	Reset Cathode
5	Keep Alive Anode
6	Keep Alive Cathode
7	Phase 4 Cathode
8	Phase 3 Cathode
9	Phase 5 Cathode
10	Channel No. 2 Anode

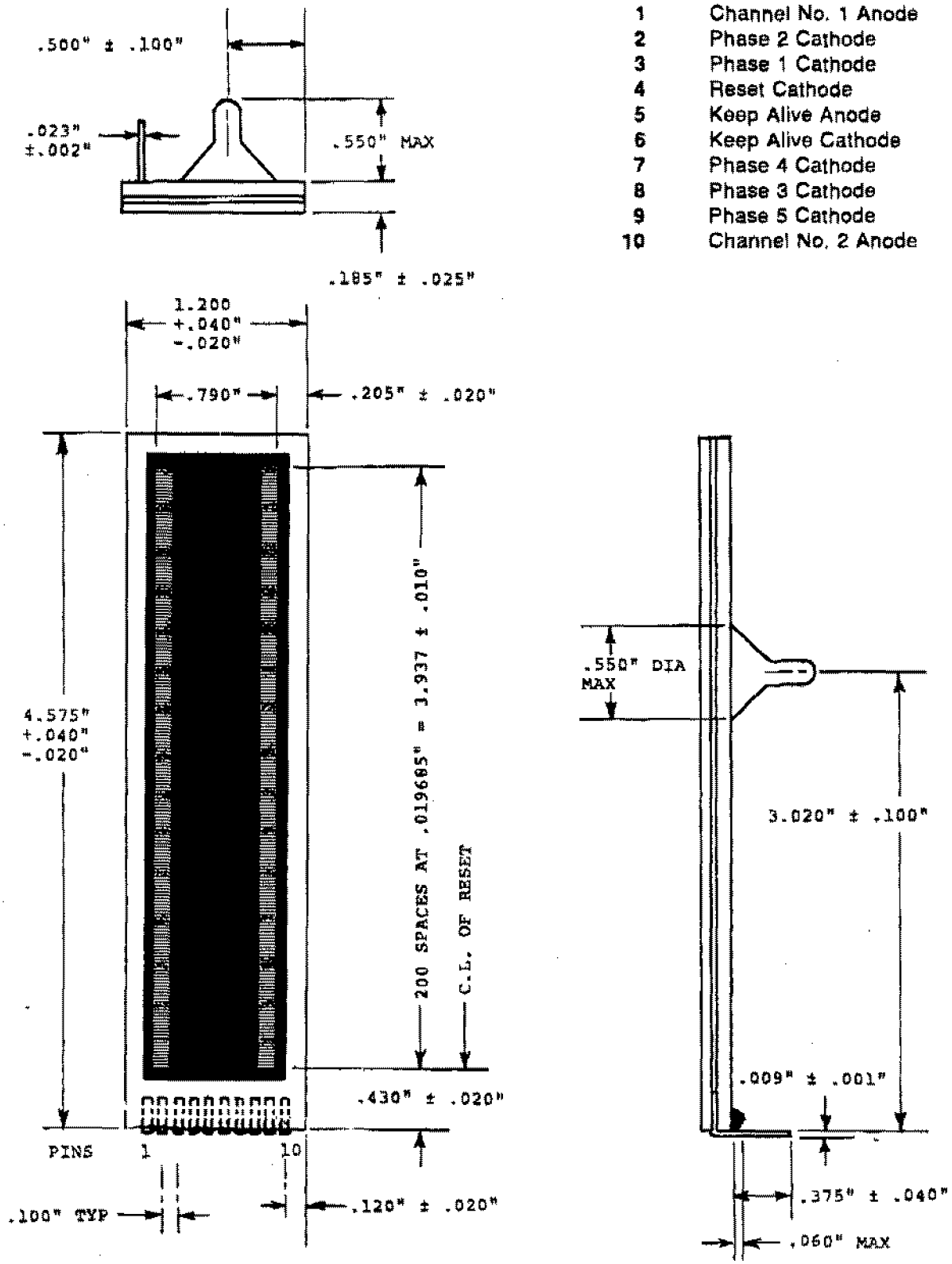

Figure 4: PBG-12205 OUTLINE DRAWING

PIN CONNECTORS

Channel No. 1		Channel No. 2	
Pin	**Connection**	**Pin**	**Connection**
1	Anode	9	Anode
2	Top Reset Cathode	10	Top Reset Cathode
3	Phase 1 Cathode	11	Phase 1 Cathode
4	Bottom Reset Cathode	12	Bottom Reset Cathode
5	Phase 2 Cathode	13	Phase 2 Cathode
6	Keep Alive Cathode	14	Keep Alive Cathode
7	Keep Alive Anode	15	Keep Alive Anode
8	Phase 3 Cathode	16	Phase 3 Cathode

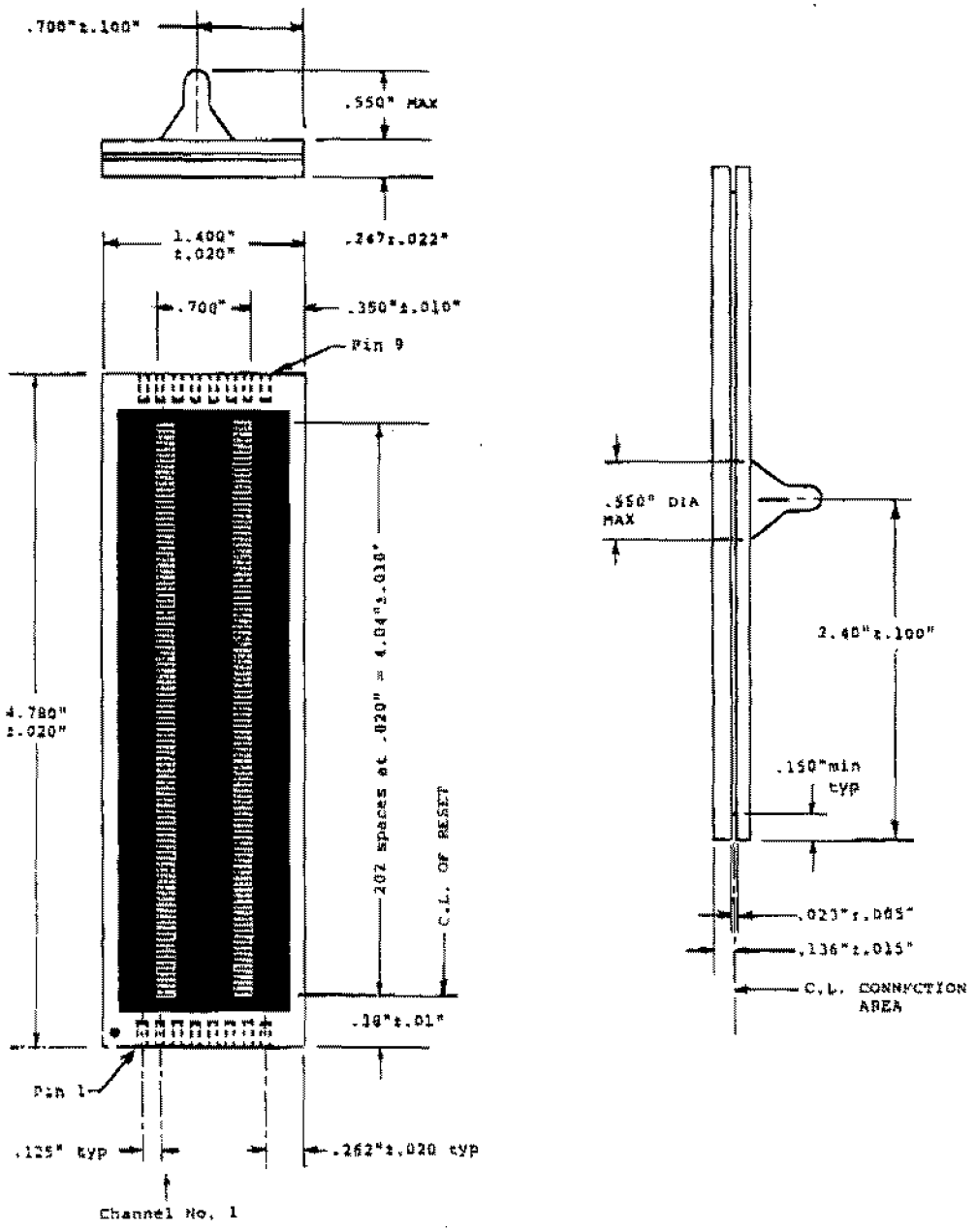

Figure 5: PBG-12203 OUTLINE DRAWING

MOUNTING

Dale bar graphs are designed for mounting behind a host system panel. The method of securing is left as a user option best suited to the particular application. Some viable methods are shown below:

1. Double sided foam adhesive tape (3M).
2. Small plastic mirror-support clips (as typically used to support hanging mirrors).
3. Housings shaped to mechanically grip the device.

The bar graph consists of two pieces of glass. During operation size changes are caused by thermal expansion and contraction. The mounting method used must allow for expansion and contraction of the units. A rigid fixing method, such as epoxy, must not be used. Such a fixing method will often result in either the cracking of the glass or the separation of the two pieces of glass.

INTERFACE OPERATION (All but PBG-12203)

1. Each device (except for PBG-12203) contains a common reset cathode which is energized for one cathode bar time per scan. The time taken for one scan of the device is equal to one more than the number of display elements (N + 1) times the cathode bar time.
2. The display anode for each channel must be turned on at reset time.
3. Following the reset time, each cathode phase is sequentially energized for one bar time. For example, in the PBG-16101 the sequence would be reset, phase 1, phase 2, phase 3, phase 1, phase 2, etc.
4. During this interval the bar graph will illuminate from the reset end up to the cathode currently being addressed.
5. When the desired display height in the bar graph is reached, the display anode for that channel is turned off (returned to display anode off-bias).
6. The remaining cathodes are scanned until the full bar count value is reached, indicating time for another reset.
7. This cycle is repeated at a rate of 60 times per second or more.

INTERFACE OPERATION (PBG-12203)

1. Operation is similar to that previously described except that the device contains a reset cathode at each end of the panel. This allows scanning to commence from either end of the panel or even from both ends simultaneously.
2. Each channel may display two independent columns of information as long as the combined total display for that channel does not exceed 201 bar counts.
3. A reset is applied to one end of the bar graph and the relevant channel display anode is turned on.
4. Scanning then commences from the end which was reset. Note that when the bottom reset is the starting point, scanning must proceed in the sequence phase 1, phase 2, phase 3, phase 1, etc.; but for the top reset, scanning sequences phase 3, phase 2, phase 1, phase 3, etc. The bottom of the bar graph is shown by the position of the dot adjacent to pad 1 (see figure 7).Scanning continues until the desired channel height is reached (Point A).
5. The display anode is left on and the opposite reset is then energized for one bar time.
6. The cathodes are now addressed but in the opposite phase sequence (i.e., instead of $\phi 1$, $\phi 2$, $\phi 3$ the sequence becomes $\phi 3$, $\phi 2$, $\phi 1$, $\phi 3$, $\phi 2$, $\phi 1$, etc.).
7. Bar is scanned until desired displayed value is reached, representing second displayed height (Point B). At this time the display anode is turned off.
8. Remaining cathodes are scanned through a total of 201 bar times.
9. The above sequence results in two illuminated areas: the first is from one end (first reset) to Point A, and the second is from the opposite end to Point B.
10. The total number of displayed bars must not exceed 201.

TYPICAL DRIVE CIRCUITS

The circuits described below allow an input of one or two analog voltages of between 0 and 30 volts to be displayed on the bar graphs as proportionally displayed displacements.

PBG-12201, PBG-16101 and PBG-12205

The circuit shown is designed to operate with the PBG-16101. Figures in parentheses allow use with the PBG-12201. For operation with the PBG-12205 an additional flip flop and transistor should be added to allow for 5-phase operation.

A typical circuit is shown in block diagram form and schematic form in figures 6 and 7 respectively. Operation is controlled by a free running clock circuit with a basic period of 140 μs (70 μs). This is applied to the reset and phase generator circuitry.

The reset generator is a divide-by-100 (200) counter with two outputs. One output is applied to the ramp generator; the other output is appllied to the reset anode of the display.

The ramp generator provides a linearly rising sawtooth voltage from 0 to + 1.01V (2.01V), commencing at 0V at reset pulse time and reaching maximum voltage in 14.2 ms.

This ramp signal is applied to one input to a dual input comparator circuit.

The analog voltage to be displayed is applied across scaling networks designed to limit the maximum input voltage to the circuit to 1.01V (2.01V). This scaled voltage is applied to the other input of the comparator. The comparator drives the front anode of the bar graph.

At the same time that the clock signal is supplied to the reset circuit, it is supplied to the 3-phase generator. This circuit operates as a ring counter and continually generates the three phases required to drive the cathode.

At each reset pulse, the anode circuit is enabled, and as long as the input voltage exceeds the level of the ramp voltage the comparator output is maintained, the anode voltage is retained and the scan is illuminated. When coincidence occurs between the input signal and the ramp the anode voltage drops and the scan ceases.

This action is repeated at a rate of approximately 70 times per second, allowing the bars to appear

TYPICAL DRIVE CIRCUITS

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A typical circuit is shown in block diagram form and schematic form in figures 6 and 7 respectively. Operation is controlled by a free running clock circuit with a basic period of 140 μs (70 μs). This is applied to the reset and phase generator circuitry.

The reset generator is a divide-by-100 (200) counter with two outputs. One output is applied to the ramp generator; the other output is appllied to the reset anode of the display.

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The analog voltage to be displayed is applied across scaling networks designed to limit the maximum input voltage to the circuit to 1.01V (2.01V). This scaled voltage is applied to the other input of the comparator. The comparator drives the front anode of the bar graph.

At the same time that the clock signal is supplied to the reset circuit, it is supplied to the 3-phase generator. This circuit operates as a ring counter and continually generates the three phases required to drive the cathode.

At each reset pulse, the anode circuit is enabled, and as long as the input voltage exceeds the level of the ramp voltage the comparator output is maintained, the anode voltage is retained and the scan is illuminated. When coincidence occurs between the input signal and the ramp the anode voltage drops and the scan ceases.

This action is repeated at a rate of approximately 70 times per second, allowing the bars to appear as a continuous flicker-free display.

Flip-flop A5 shown on the schematic is optional. When installed, the last bar in the column may cycle on and off at a slow rate if the input signal is between two steps. If not installed, the last bar will appear slightly dimmer if the input signal is between two steps. When A5 is not used, jumpers should be connected between pins 3 and 5, and 9 and 11 of A5.

ADJUSTMENTS

Prior to supplying an input signal, the circuit must be calibrated. Four potentiometers must be adjusted. Two of these control the scaling of the maximum input voltage to permit any analog signal with amplitude ranges up to + 30V to be applied to the circuit.

Adjustments must also be made to establish the ramp comparison voltage and reset pulse generation levels.

Input Scaling Adjustment:

1. Turn potentiometer R40 and R41 fully clockwise.
2. Connect DVM to pin 4 of A1.
3. Apply voltage equivalent to maximum analog signal to be displayed to V1 input.
4. Adjust R41 for + 1.01V (2.01V) at pin 4 of A1.
5. Connect DVM to pin 8 of A1.
6. Apply voltage equivalent to maximum analog signal to be displayed to V2 input.
7. Adjust R40 for + 1.01V (2.01V) at pin 8 of A1.

Reset Pulse Generator Adjustment:

1. Adjust R44 for mid-range setting.
2. Connect DVM to pin 6 of A1.
3. Turn system + 5V power on.
4. Adjust R44 for + 1.01V (2.01V) at pin 6 of A1.

Ramp Generator Adjustment:

1. Adjust R45 for mid-range setting.
2. Apply voltage equivalent to maximum analog signal to be displayed to V1 and V2 inputs.
3. Turn system + 5V and + 250V power on.
4. Adjust R45 slowly until all bars are lit.
5. Decrease input voltage and observe that the bar height decreases proportionally.

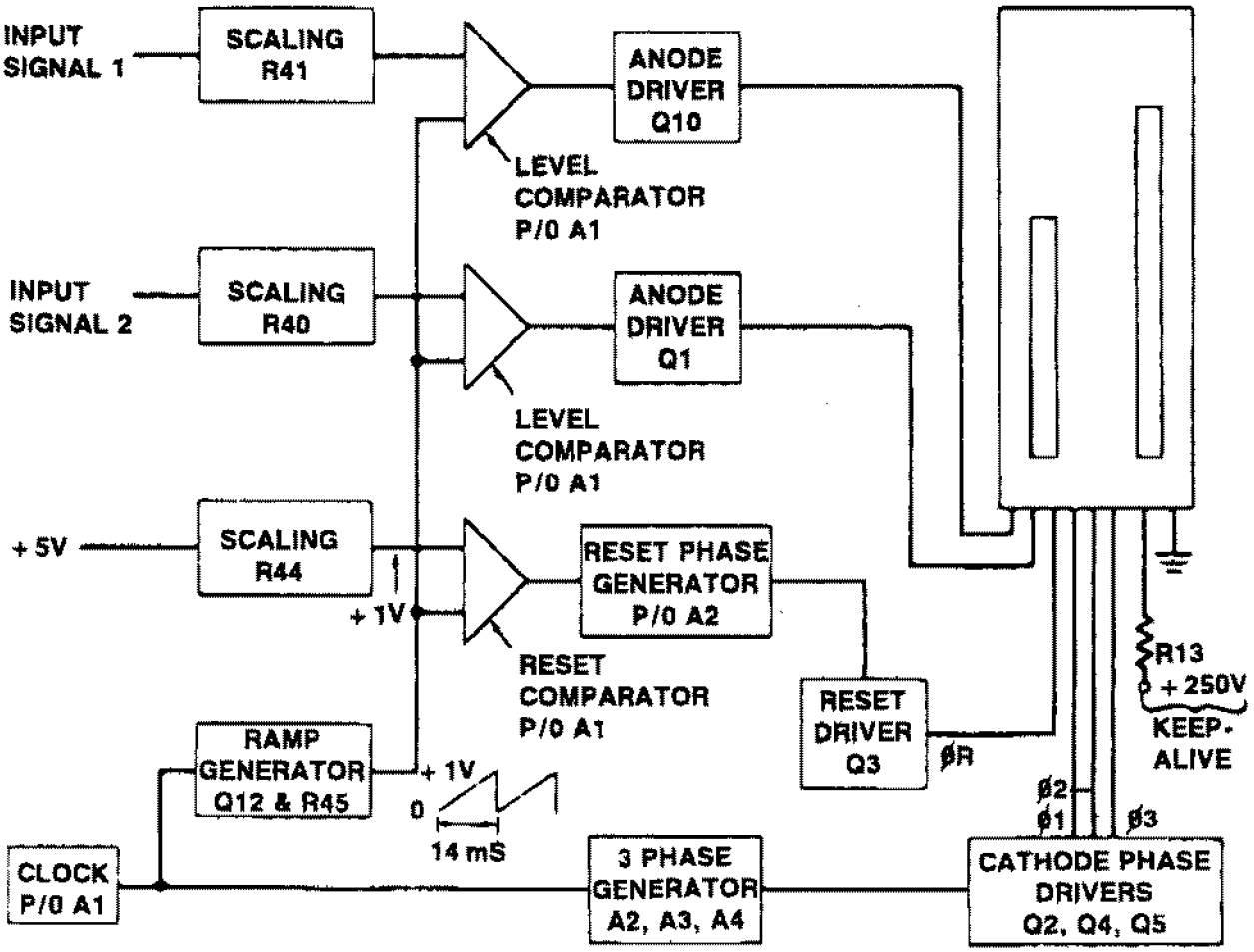

Figure 6: BLOCK DIAGRAM PBG-12201, PBG-16101 and PBG-12205

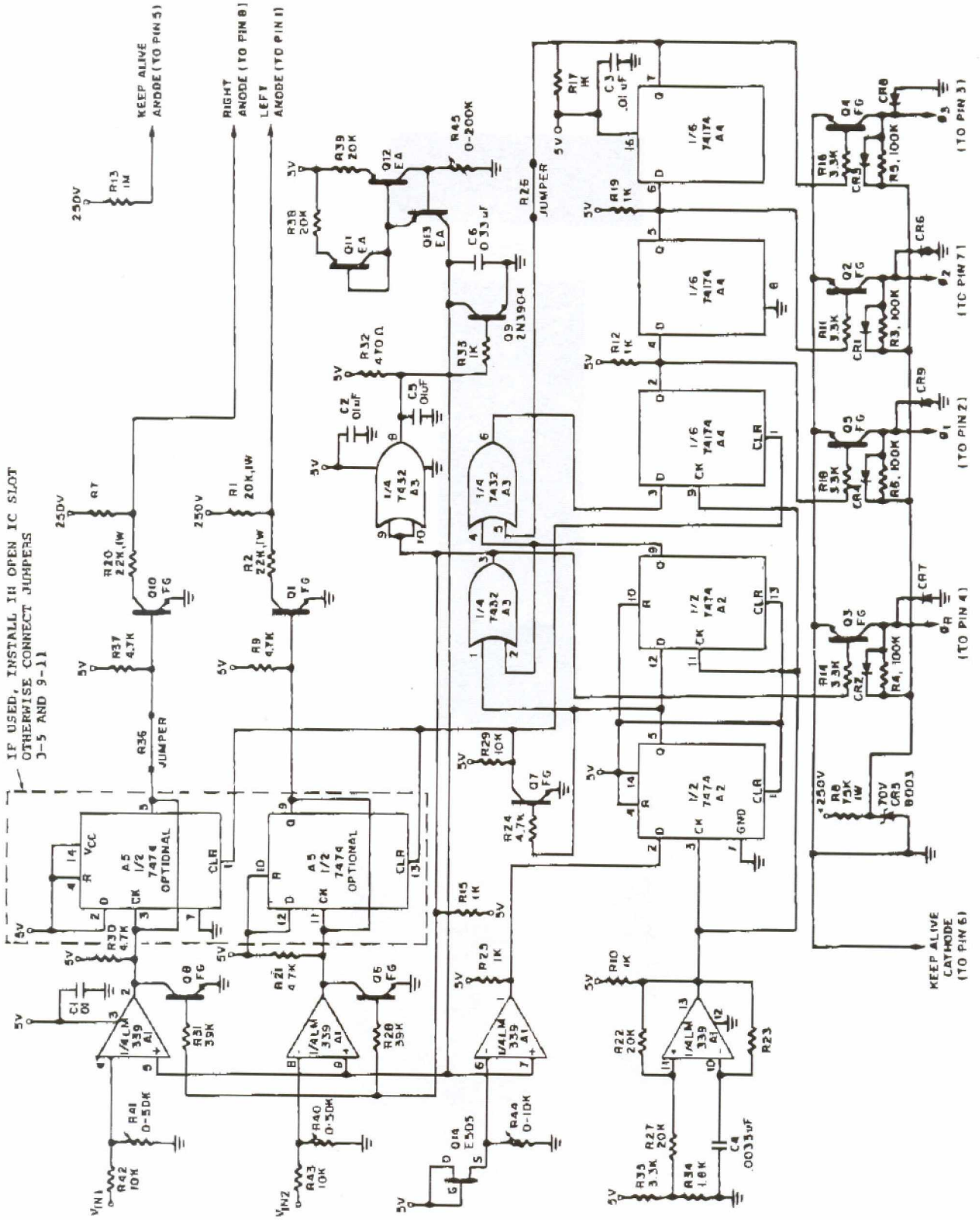

Figure 7: SCHEMATIC DIAGRAM PBG-12201, PBG-16101 and PBG-12205

PARTS LIST

Ref. Desig.	P/N or Value
A1	LM339 Comparator
A2	7474 Flip Flop
A3	7432 OR Gate
A4	74174 Flip Flop
C1	.01uF
C2	.01uF
C3	.01uF
C4	.0033uF
C5	.01uF
C6	.33uF
CR1	1N3070 or equiv.
CR2	1N3070 or equiv.
CR3	1N3070 or equiv.
CR4	1N3070 or equiv.
CR5	B003 Zener
CR6	1N3070 or equiv.
CR7	1N3070 or equiv.
CR8	1N3070 or equiv.
CR9	1N3070 or equiv.
Q1	2N7055
Q2	2N5550
Q3	2N5550
Q4	2N5550
Q5	2N5550
Q6	2N3643
Q7	2N3643
Q8	2N3643
Q9	2N3904
Q10	FG or PN7055
Q11	EA or 2N4209
Q12	EA or 2N4209
Q13	EA or 2N4209
Q14	E505 FET
R1	20K (33K) 1W
R2	22K 1W
R3	100K ¼W
R4	100K ¼W
R5	100K ¼W
R6	100K ¼W

Ref. Desig.	P/N or Value
R7	20K (33K) 1W
R8	75K 1W
R9	4.7K ¼W
R10	1K ¼W
R11	3.3K ¼W
R12	1K ¼W
R13	1M ¼W
R14	3.3K ¼W
R15	1K ¼W
R16	3.3K ¼W
R17	1K ¼W
R18	3.3K ¼W
R19	1K ¼W
R20	22K 1W
R21	4.7K ¼W
R22	20K ¼W
R23	15K (7.5K) ¼W
R24	4.7K ¼W
R25	1K ¼W
R26	Jumper
R27	20K ¼W
R28	39K ¼W
R29	10K ¼W
R30	4.7K ¼W
R31	39K ¼W
R32	470ohm ¼W
R33	1K ¼W
R34	1.8K ¼W
R35	3.3K ¼W
R36	Jumper
R37	4.7K ¼W
R38	20K ¼W
R39	20K ¼W
R40	0-50K Pot ¼W
R41	0-50K Pot ¼W
R42	10K ¼W
R43	10K ¼W
R44	0-10K Pot ¼W
R45	0-200K Pot ¼W

The unique feature of this type of display is that addressing and scanning are acheived by means of priming and transfer of the priming signal sequentially from the first position to the following ones. This is accomplished by establishing a glow in the gas at the bottom side of the panel. This glow then appears at the top side that contains the display anode and cathode, and is transferred along by the priming signal moving through small holes from the priming section to each of the other sections, sequentially. This transfer of ignition from the first section to the last section in a row is done without the need for electronic scanning or multiplexing signals, so that the electronics and connections are reduced by using this technique. It is most effective for bar graphs with up to 2 bars of 201 elements each, although the electronics is somewhat complex, requiring three phase circuitry as well as anode drivers. However, the resulting image can be impressive. (typical refresh rate of 70Hz)

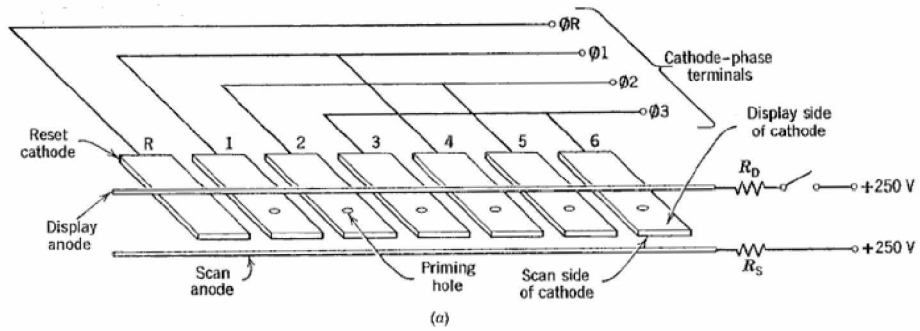

Figure 3.5 (*a*) Simplified diagram of cell electrodes for Self-Scan panel. After Cola [2], by permission of Academic Press.