IL2238 Laboratory Report

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I Objective

A closed loop feedback voltage operational amplifier using a two-stage topology was designed and simulated in Cadence Virtuoso suite, within the following specifications of interest –

- Open loop gain ≥ 50 dB
- Bandwidth (3-dB) = 2 MHz (after compensation)
- Phase margin ≥ 60°
- Power consumption ≤ 4 mW
- Input referred in-band (100 kHz - 2 MHz) integrated noise, $V_{n,in} \leq 40\mu V_{\text{rms}}$
- V_{DD} = 1.8 V, at 180 nm XFAB

II Design Strategies and Results

1. Transistor Selection and Operation Point

   According to the requirements, each transistor has a transit frequency f_T no less than $10f_u$, while

   $$f_u = A_v \cdot BW_{-3dB},\ A_v = 50dB \approx 316.23.$$

   We have

   $$f_T \geq 6.32\ \text{GHz},$$

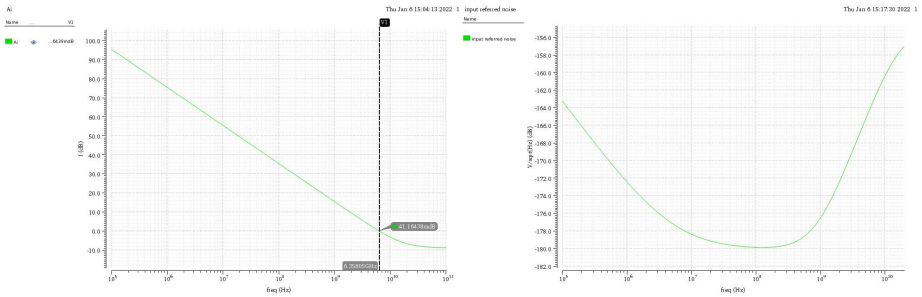
   But in actual design, we only need to consider f_T that satisfies the gain of a certain stage and a transistor belongs to if no more stability problems are caused.

   For the 1st stage differential amplifier, we need that:

   - The gain to be as high as possible with the bandwidth satisfied,
   - The noise should be well controlled,
   - The PVT sensitivity should be reduced to the lowest level,
   - Control the power consumption – static current constraint (this is ignored in the first version of design).

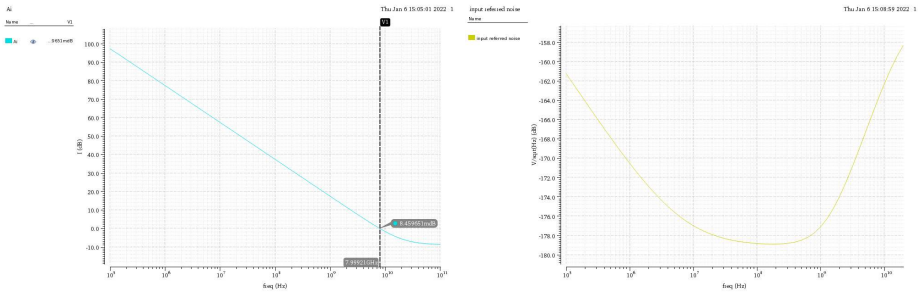
   In the first version of design, we mainly focus on the gain performance and noise reduction. Considering that transistors with larger area and lower output resistance has lower input referred noise level and that a higher $\frac{W}{L}$ yields a higher gain level at the same static current, we choose 150/0.3 NMOS ($f_T = 6.36$ GHz, $V_{n,in} = 4.018\mu$V, $g_m = 13.21$ mS, $\frac{g_m}{I_D} = 13.52$, $C_{GD} = 49.5$ fF, $C_{GS} = 248.4$ fF, $r_o = 7.831$ kOhm) and 100/0.3 PMOS ($f_T = 8.46$ GHz, $V_{n,in} = 4.342\mu$V, $g_m = 6.322$ mS, $\frac{g_m}{I_D} = 6.322$, $C_{GD} = 32.17$ fF, $C_{GS} = 179.2$ fF, $r_o = 3.855$ kOhm) for the first stage amplifier, while 100/0.3 NMOS ($f_T = 8.46$ GHz, $V_{n,in} = 5.026\mu$V, $g_m = 11.41$ mS, $\frac{g_m}{I_D} = 11.41$, $C_{GD} = 33$ fF, $C_{GS} = 172.3$ fF, $r_o =$

8.042 kOhm) and 100/0.3 PMOS for the second, 1mA bias current for all transistors.



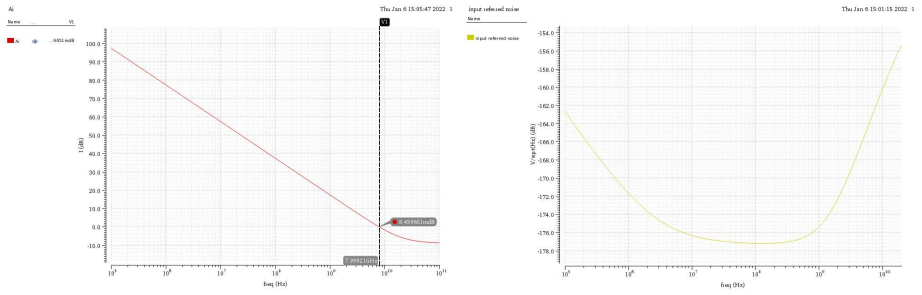
(a) (b)

Fig 1. NMOS performance in the differential pair, (a) frequency response, (b) input referred noise level, supposing $V_{DS} = 500$ mV



(a) (b)

Fig 2. NMOS performance in the common source stage, (a) frequency response, (b) input referred noise level, supposing $V_{DS} = 500$ mV



(a) (b)

Fig 3. PMOS performance in the differential pair and the common source stage, (a) frequency response, (b) input referred noise level, supposing $V_{DS} = 500$ mV

Since we noticed that the first version has a rather low power efficiency and there is much space for trade-off between noise performance and power consumption, we made the second decision that all transistors in the design are 50/0.3 in dimension (for $\frac{g_m}{I_D}$, NMOS 13.38, PMOS 8.02) and operating

with 350μA bias current. All transistors mentioned below are using the parameters in the first design and capacitive load is 1 pF unless otherwise stated. Two layouts of the circuit will cover both designs.

2. Differential Amplifier Design

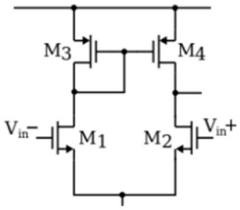


Fig. 4 Differential Pair

According to the data from measurement, we have$A_{v1,2} = -g_{m1,2} \cdot (r_{o3,4}//r_{o1,2}) = 13.21 \times (3.855//7.831)$ V/V = 30.59 V/V = 29.71 dB, which is a moderate gain. Below are the simulation results of gain, and we have $V_{n,in} = 8.146\ \mu$V.

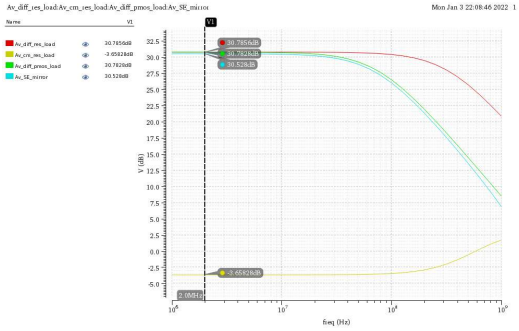


Fig. 5 Differential Pair Simulation

3. Common Source Amplifier Design

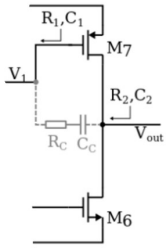


Fig. 6 CS amplifier

The common source stage uses a PMOS transistor as an amplifier tube and an NMOS as a current source load. We theoretically have

$$A_{v2} = -g_{m7} \cdot (r_{o6}//r_{o7}) = -6.322 \times (8.042//3.855)\ \text{V/V} = 16.47\ \text{V/V} = 24.33\ \text{dB}.$$

So, we can reach an overall gain

$$A_{v(dB)} = A_{v1(dB)} + A_{v2(dB)} = 29.71 + 24.33\ \text{dB} = 54\ \text{dB} > 50\text{dB}.$$

Below are simulation results, and we have $V_{n,in} = 8.146\ \mu V$.

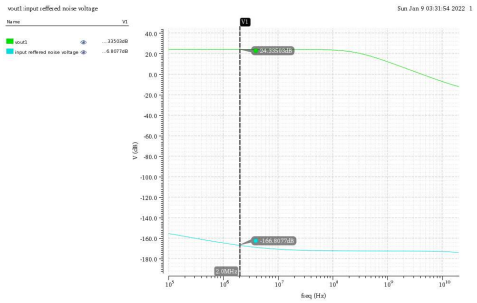


Fig. 7 CS stage amplifier performance

4. Ideal Simulation and Miller Compensation

After finishing the CS stage and differential pair design, we move onto simulation with ideally fixed V_{DS} simulation to roughly check the global performance of the amplifier. We still assume that all transistors have $V_{DS} = 500$ mV.

First, we test the pure differential pair in schematic file "OPAMP_START".

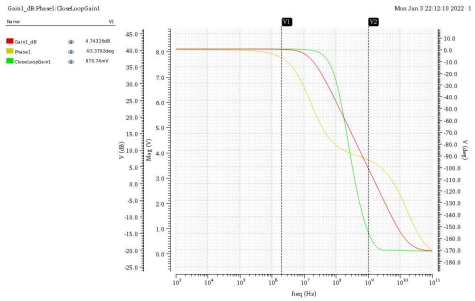


Fig. 8 OPAMP_START simulation

We observe that it has an open loop gain at 40 dB and a close loop gain voltage at 870mV, which is rather close to 900mV that we demand.

We can further boost the gain with the CS stage amplifier, as is simulated in schematic "OPAMP_0".

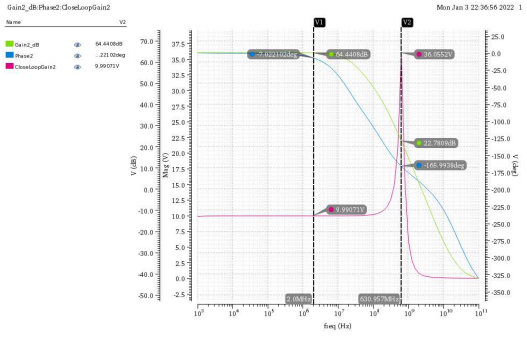


Fig.9 Ideal OPAMP simulation with only NMOS pair and PMOS CS stage amplifier, no compensation applied.

We can see that these two stages can yield a gain at most 64 dB and resonates at 630.957MHz, which needs Miller compensation to eliminate the instability. To estimate the Miller compensation capacitance, we analyze the circuit as below with only C_{GD} and C_{GS} considered.

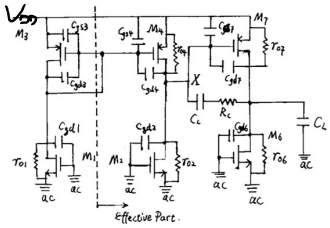


Fig. 10 Small signal analysis of OPAMP

We have

$$C_X \approx C_{gd7}(1+A_{v2}) + C_{gs} + C_{gd4}\left(1+\frac{1}{g_{m4}(r_{o2}||r_{o4})}\right) + C_{gd} + C_c(1+A_{v2}),$$

$$C_{out} \approx C_{gd}\left(1+\frac{1}{A_{v2}}\right) + C_L + C_c\left(1+\frac{1}{A_{v2}}\right) + C_{gd6}$$

Hence:

$$\omega_X = \frac{1}{C_X(r_{o2}||r_{o4})},$$

$$\omega_{out} = \frac{1}{C_{out}(r_{o7}||r_{o6})},$$

$$-\omega_Z = \omega_{out} = \frac{1}{C_c\left(R_c - \frac{1}{g_{m7}}\right)}.$$

From experiment, we observe that it is more easily to ensure a phase margin larger than $60°$ when

$$\omega_{p2} = 2\omega_{p1} \cdot A_{dc}$$

while typically $\omega_{p1} = \omega_X,\ \omega_{p2} = \omega_{out}$.

With measured value, we can get

$$C_c = 2.1\ \text{pF}, R_c = 275\ \text{Ohm}$$

While R_c may need to be tweaked due to its sensitivity in C_c, which is different between the one in fixed-V_{DS} simulation and that in actual schematic for

$$r_o \propto \lambda^{-1}, \lambda = \frac{1}{\frac{I_{bias}}{g_{ds}} - V_{DS}}.$$

With calculated C_c and R_c as a start point, we move onto the non-ideal simulation with schematic "OPAMP_nonideal". Results are demonstrated as below.

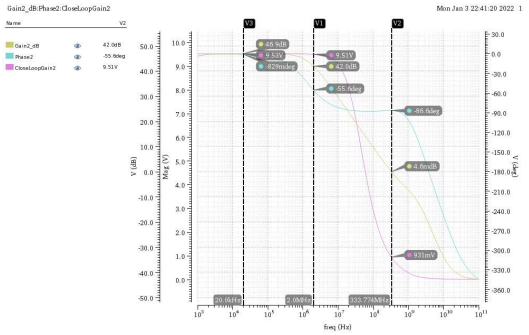


Fig. 11 Non-ideal OPAMP simulation with equal resistive load and miller compensation.

We can see that the DC gain is a little bit lower than desired, and the phase margin is slightly higher than best range of $[60°, 70°]$, which slows down the speed of the OPAMP. We temporarily accept this result and continue with a more complete architecture in schematic "OPAMP_1", and we have the results as below:

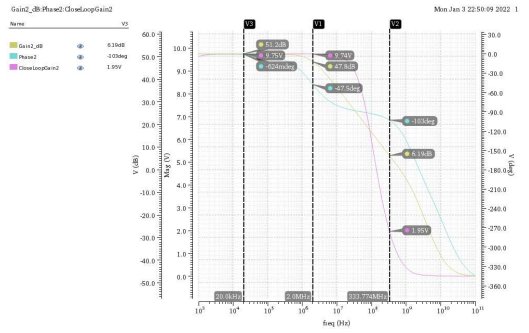


Fig. 12 OPAMP_1 simulation result

The characteristic of the OPAMP_1 is much closer to requirement.

5. Full Schematic Design

After taking these parameters into the final circuit in schematic "OPAMP_2" and slightly modifying the dimension of current mirrors in accordance with the current source load of common source amplifier, we have the schematic as below:

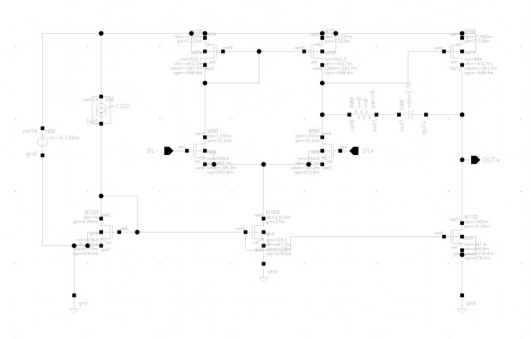
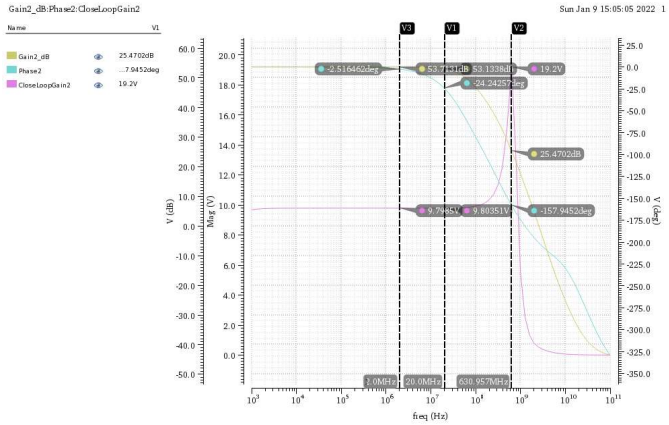


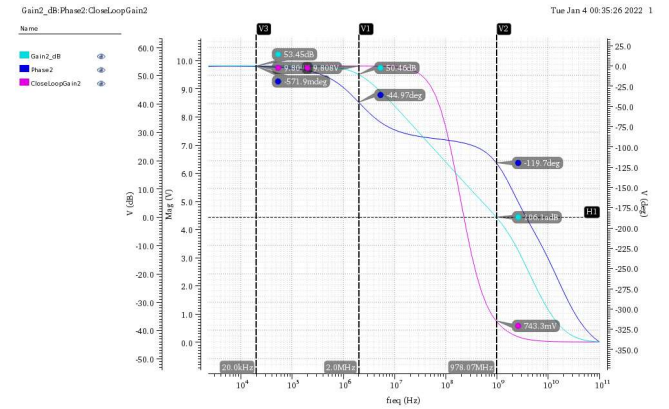
Fig. 13 Whole circuit design of OPAMP with $C_c = 2.7$ pF, $R_c = 220$ Ohm

To better reduce the influence of V_{DS}, which interferes with the accuracy of current mirrors, and shield the control voltage from output voltage variance, we use higher channel length to decrease λ and increase the output resistance of mirrors.

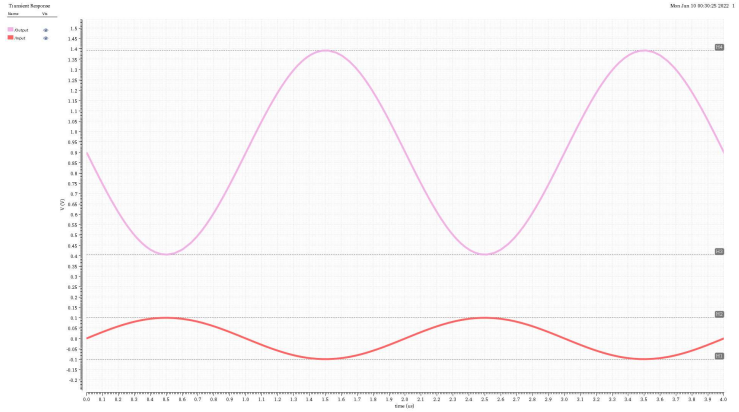
The simulation of OPAMP characteristic is demonstrated as below.



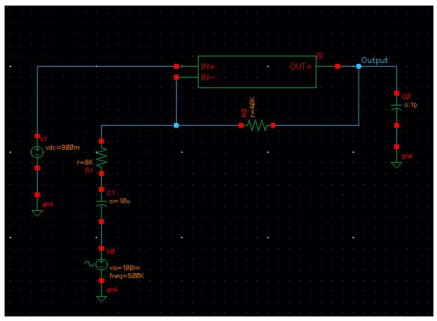
(a)



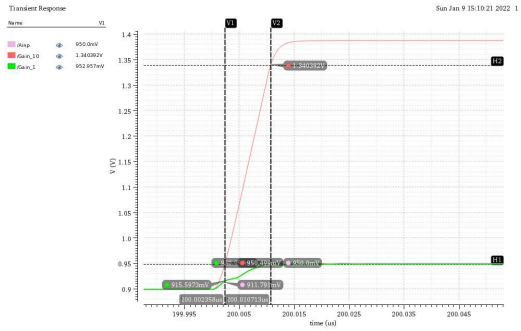
(b)



(c)



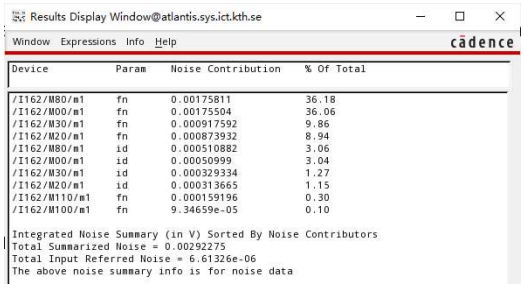
(d)



(e)

Fig. 14 Performance of OPAMP. (a) AC response of open or close loop before compensation. (b) AC response of open or close loop after compensation, phase margin 60.3°. (c) 500 kHz transient response output-input graph. (d) Transient testbench schematic. (e) Step response test.

Below is the result for noise simulation within 100 kHz to 2 MHz.



Device	Param	Noise Contribution	% Of Total
/I162/M80/m1	fn	0.00175811	36.18
/I162/M00/m1	fn	0.00175504	36.06
/I162/M30/m1	fn	0.000917592	9.86
/I162/M20/m1	fn	0.000873932	8.94
/I162/M80/m1	id	0.000510882	3.06
/I162/M00/m1	id	0.00050999	3.04
/I162/M30/m1	id	0.000329334	1.27
/I162/M20/m1	id	0.000313665	1.15
/I162/M110/m1	fn	0.000159196	0.30
/I162/M100/m1	fn	9.34659e-05	0.10

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00292275
Total Input Referred Noise = 6.61326e-06
The above noise summary info is for noise data

Fig. 15 Noise performance and contribution ranking.

According to the noise analysis done by Cadence, we observe that the most significant contributors, M80 and M00, are the amp transistors in differential pair, as the noise in front position will be amplified stage by stage.

Despite that this OPAMP yields a maximum gain at 53 dB, what is a little bit disappointing is that this amplifier costs 9.245 mW of power. We further designed an amplifier with all 50/0.3 transistors and have successfully satisfy the power requirement, and the introduction will be short.

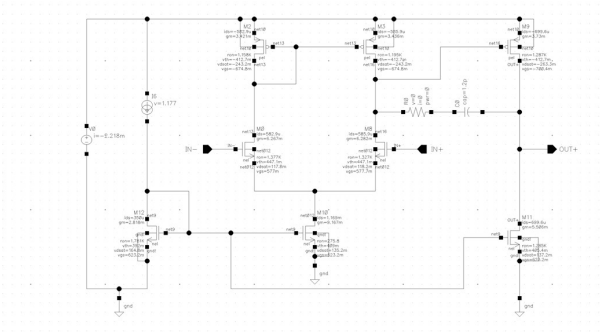


Fig. 16 Low-power design schematic with $C_c = 1.2$ pF, $R_c = 500$ Ohm.

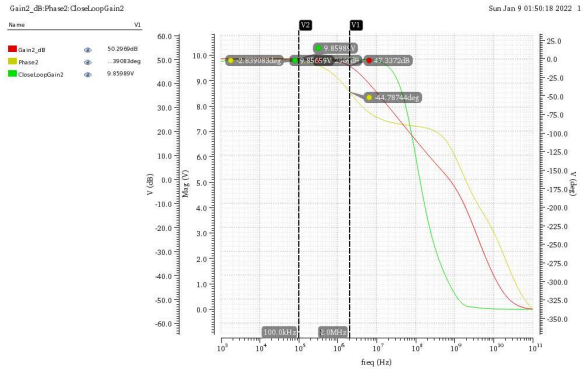


Fig. 17 Low-power design performance. Maximum DC gain at 50.3 dB and 2 MHz bandwidth. Phase margin 63.04°. Input referred noise $V_{n,in} = 12.66\ \mu$V. Total power consumption 3.993 mW.

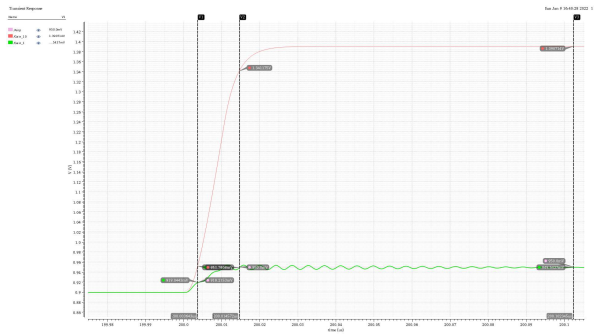


Fig. 18 Low-power design step response.

The ringing effect of low-power design is more significant than that of the high-power, indicating possible high frequency instability.

III Layout

To cut down on cost, we only used three layers of metal to connect PMOS and common centroid style NMOS pair. Due to a critical demand for pairing, all the layout is planned to be as symmetric as possible. Since overlapping of wires will cause extra capacitances which poses a threat to bandwidth, all wires are designed to reach as low crossing area as possible. However, it is hard to conceal the fact that the spacing of MOSFET is not that proper as their distances between each other are slightly far, which may introduce

mismatch issues.

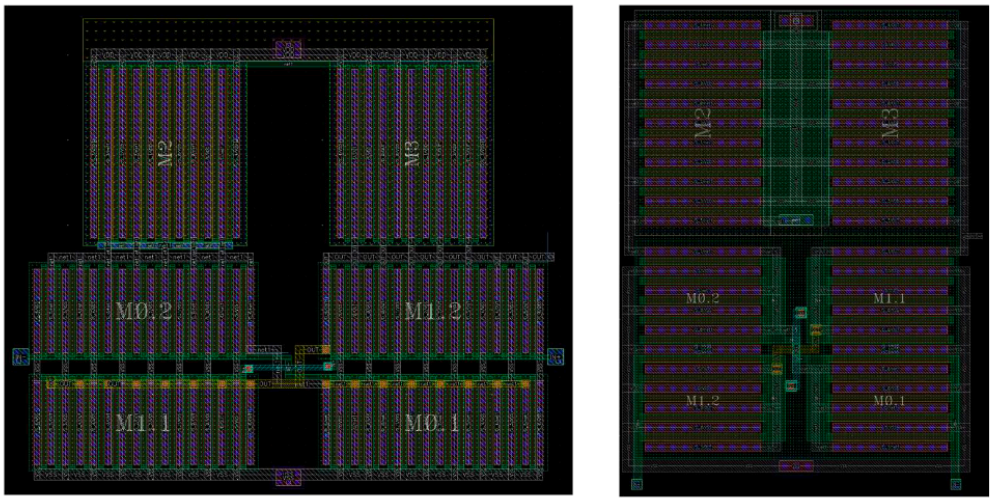
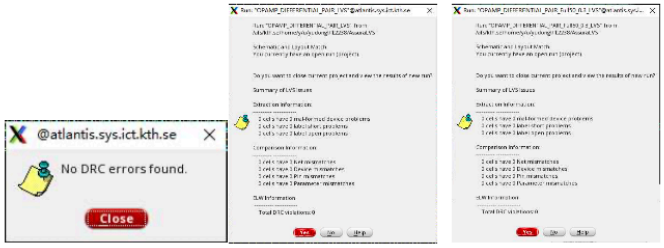


Fig. 19 Differential pair layout. The left is high-power version, the right is low-power version.



(a) (b) (c)

Fig. 20 DRC report and LVS report

The post-layout simulation results are as below. The noise performance is degraded due to the introduction of wire resistance with an input referred noise level $V_{n,in} = 8.146\,\mu V$ of high-power version and $13.22\,\mu V$ of low-power version. Due to smaller scale, the low-power version matches much better than the high-power.

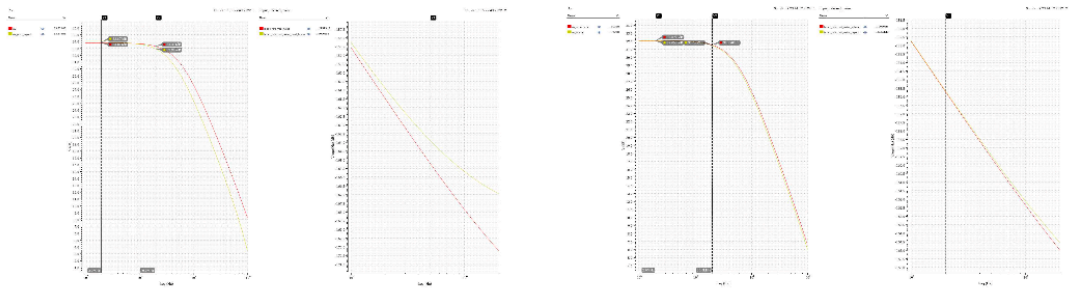


Fig. 21 Post-layout differential pair performance. The left is high-power version, the right is low-power version.

IV Conclusion

All necessary requirements of the desired OPAMP are met, while considering the power efficiency, transistors of 50/0.3 in dimension and operating with $350\mu A$ bias current are better.