In [1]:
```
#%%capture
!pip freeze > requirements.txt
!pip freeze | grep -v -f requirements.txt - | grep -v '^#' | grep -v '^-e ' | xargs pip uninstall -y
```

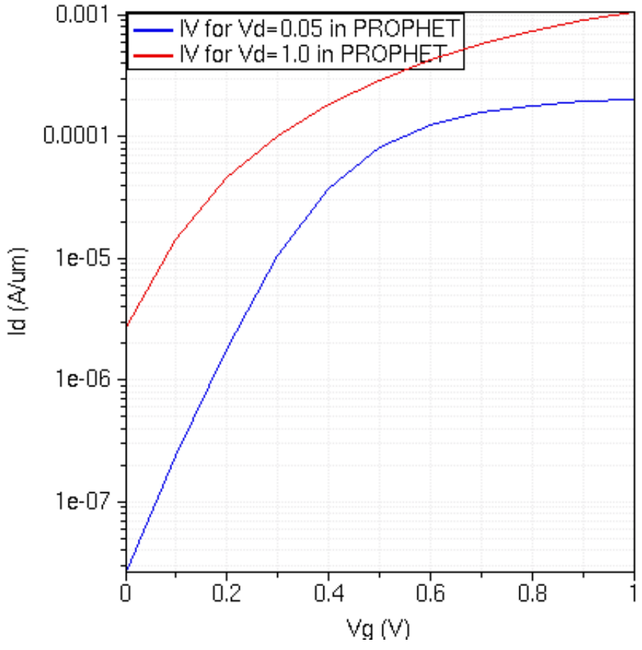
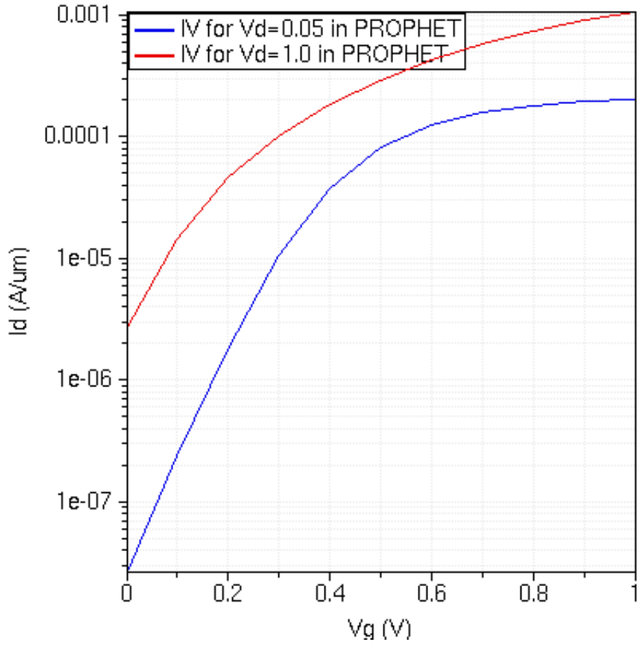
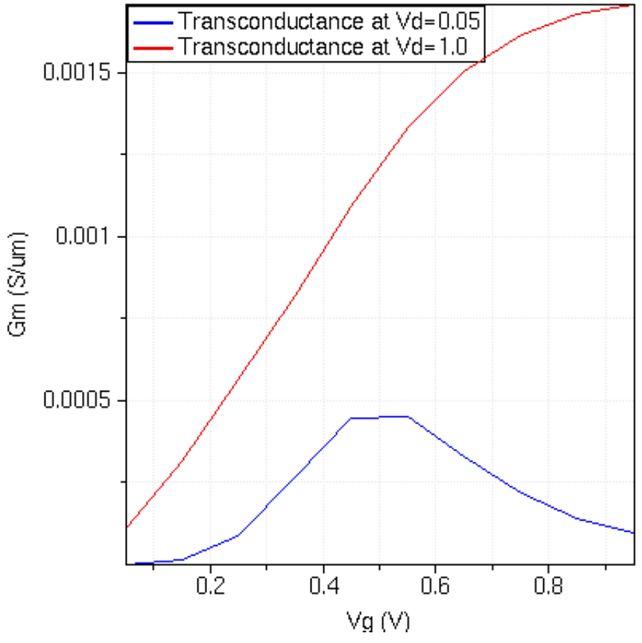
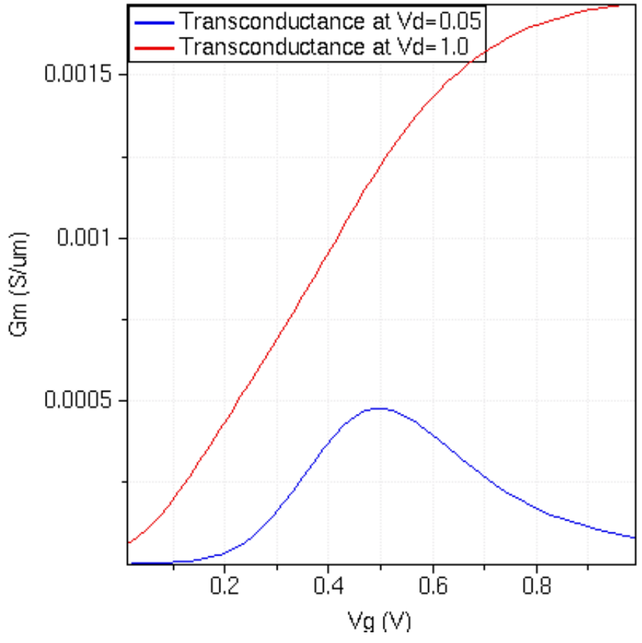
Abstract

This PROPHET TCAD MOSFET simulation work pertains to a FinFET structure with two gates (in 2D) and a simplified ultra-thin body SOI transistor at 300K, using nanoHUB's '**MuGFET**' tool.

Table of Contents

Part I: 30nm width FinFET IV (and higher derivative) sweeps

Transfer IV and transconductance simulations with 11 (default) vs 51 (optimum) gate bias steps

	@11 **gate bias steps**	@51 **gate bias steps**
Transfer IV		
G_m-V_g		

Summary

1. Transfer IV sweeps $(\log I_d - V_g \forall V_d)$ of 30nm width FinFET transistor indicate the linear subthreshold region leading up to the first curvature transition point (V_T). This linear region can be represented by the following equation:

$$I_d = 100 \cdot \frac{W}{L} \cdot 10^{\frac{q(V_g - V_T)}{\eta kT}} = 100 \cdot \frac{W}{L} \cdot 10^{\frac{(V_g - V_T)}{S}} \tag{1}$$

2. First derivative IV sweeps $(G_m - V_g \forall V_d)$ of 30nm width FinFET transistor can be seen to reach a maximum at the the first curvature transition point V_T (upon reaching FinFET saturation) and then decrease (due to the channel length modulation effect - $1/\lambda$). The maximum G_m value can be derived from the generic MOSFET IV trend in saturation - $I_d = \frac{W}{L} \cdot C_{oxe} \cdot \mu \cdot (V_g - V_T)^2$; to be:

$$G_{m,\,\max} = \frac{2 \cdot I_d}{V_g - V_T} \tag{2}$$

3. With 51 gate bias steps, the PROPHET simulator in MuGFET seems to produce smoothest Transfer IV and transconductance sweeps than with 11 (default) gate bias steps. Beyond 51 gate bias steps, the PROPHET simulator does not produce Transfer IV / Transconductance sweeps, henceforth 51 gate bias steps are chosen to be optimum for further simulations.

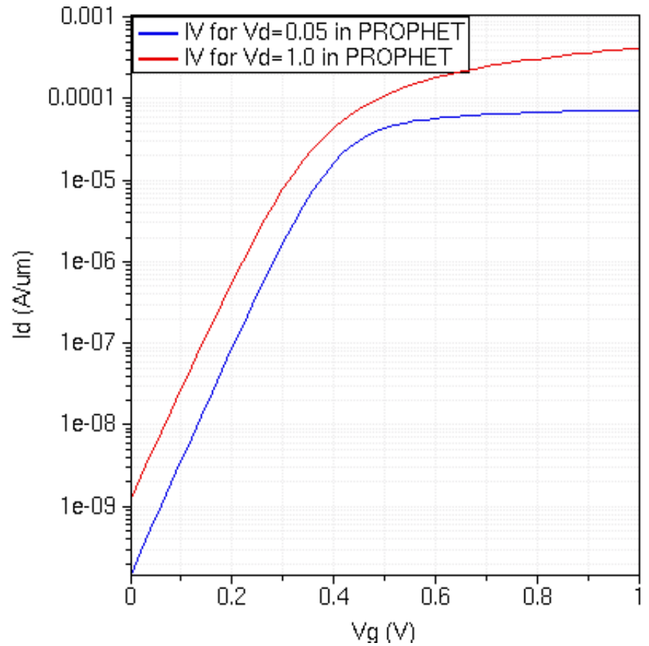
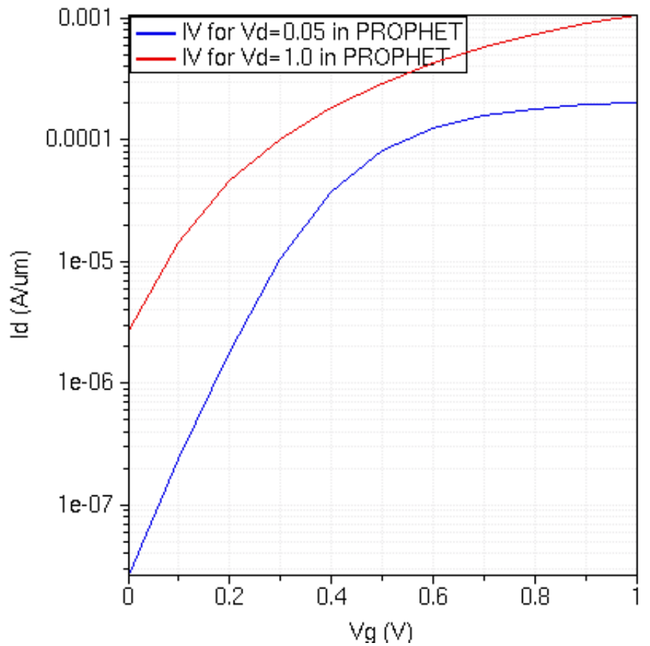
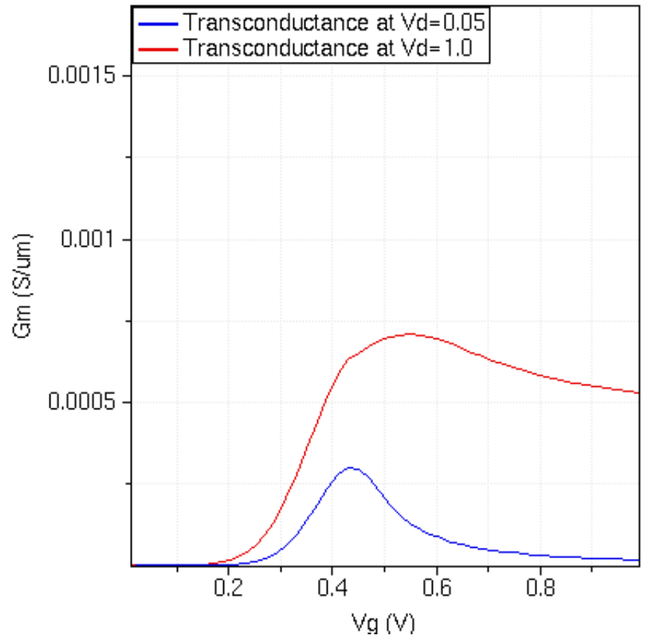
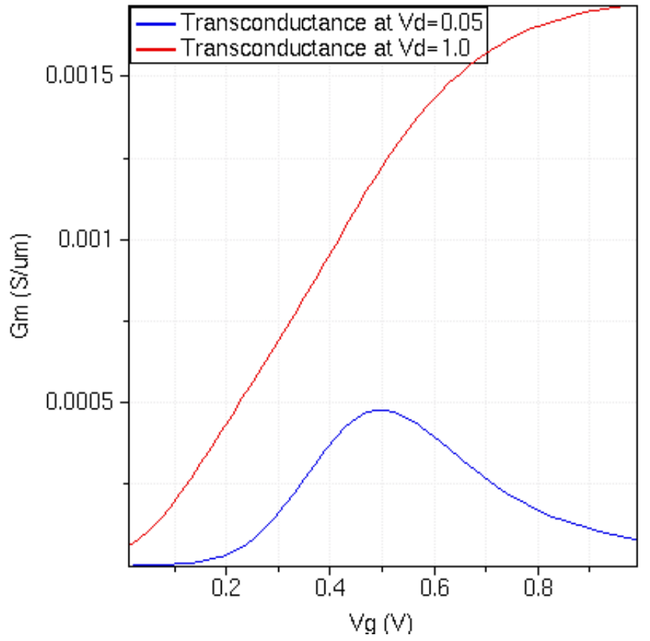
Part II: MuGFET Output Log Comprehension of 30nm width FinFET IV simulation with 51 (optimum) gate bias steps

Summary

1. Tensor mesh: `3 x 149 = 447` nodes.
2. Total simulation time: `304.12` seconds.
3. Average time for convergence at each bias point: ~ `3` seconds.
4. Numerical issues reported for 51 gate bias steps (while `Solving 'silicon_dd' with bias voltage(s): drain=1, gate=0`): `Newton failed (update too large)... cpu = 1.17 sec bias: backing off bias step` . However no meaningful Transfer IV / Transconductance sweeps were observed for PROPHET simulations beyond 51 gate bias steps.
5. Solution variables:
   - `silicon_poisson - psi` (as noted in page 47 of **[1] Prophet User Reference Guide**)
   - `silicon_dd - psi` , `electrons` , `holes` (as noted in page 48 of **[1] Prophet User Reference Guide**)
6. Derived quantities:
   - `residual norm`
   - `reduction`

Part III: Effect of gaussian doping profile on 30nm width FinFET IV (and higher derivative) sweeps

Transfer IV and transconductance simulations with 51 (optimum) gate bias steps

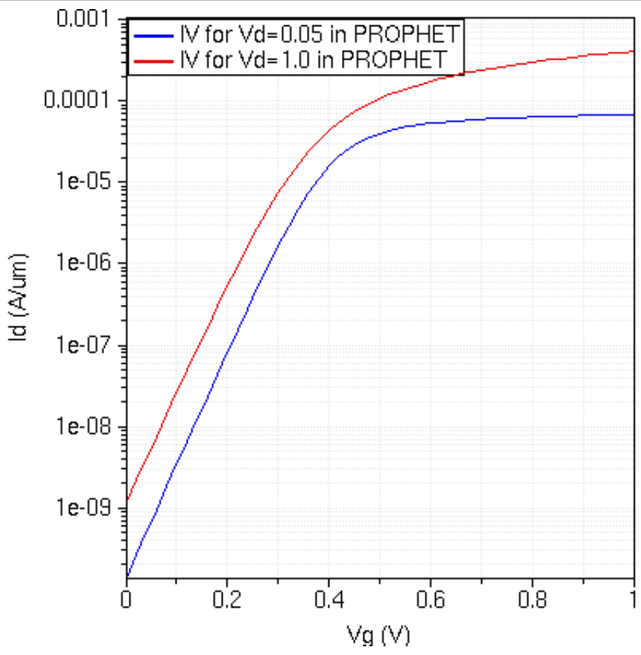
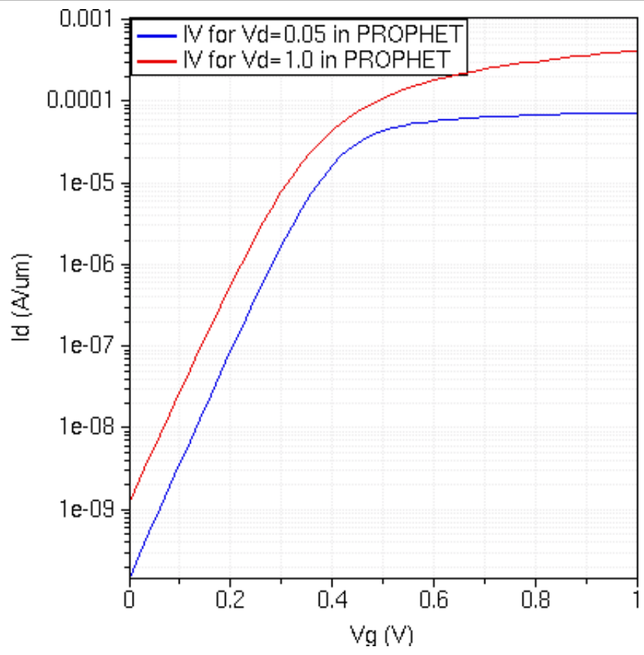
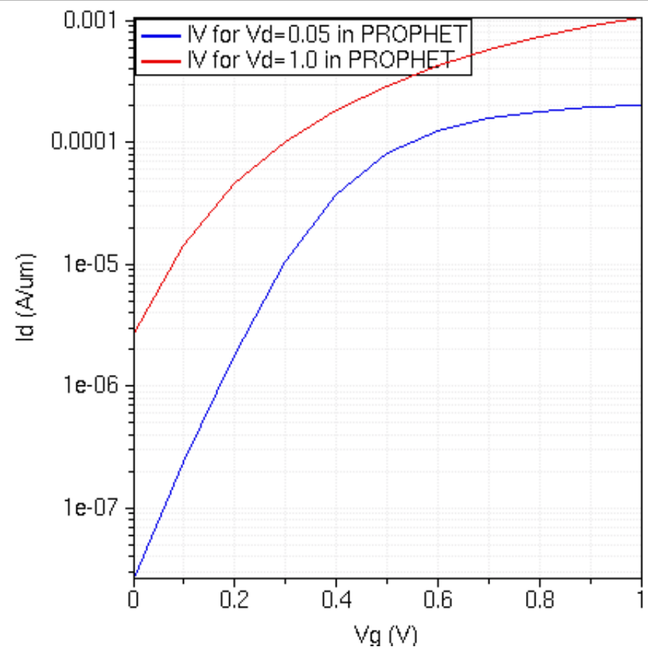
	With gaussian doping profile (characteristic length for source/ drain: 20nm, penetration into oxide: 0.05nm, @51 gate bias steps)	Without gaussian doping profile (@51 gate bias steps)
Transfer IV		
G_m-V_g		

Summary

1. The effect of a gaussian doped channel in 30nm width FinFET can be observed to decrease V_T and decrease $I_d \; \forall V_d$, which is due to increased carrier depletion due to gaussian doping profile in the channel.

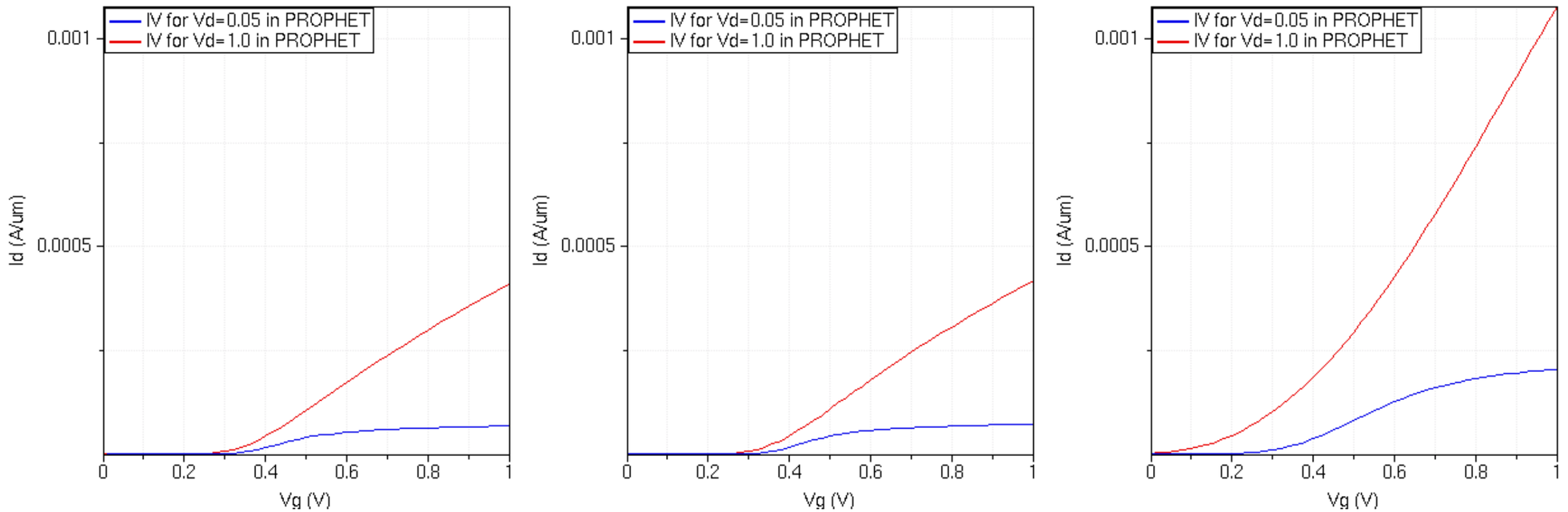
Part IV: Physics of short gate length MOSFETs: via Lombardi's mobility model on 30nm width FinFET

Transfer IV and transconductance simulations with 51 (optimum) gate bias steps

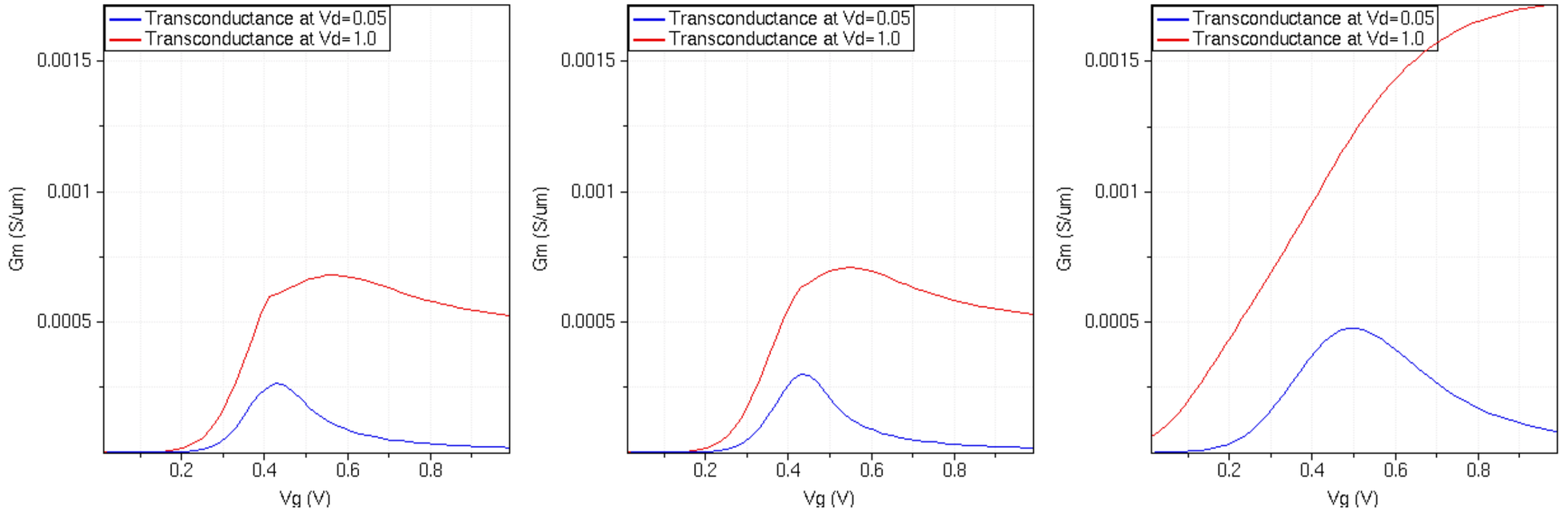
	With Lombardi's mobility model and gaussian doping profile (characteristic length for source/drain: 20nm, penetration into oxide: 0.05nm, @51 gate bias steps)	With only gaussian doping profile (characteristic length for source/drain: 20nm, penetration into oxide: 0.05nm, @51 gate bias steps)	Without gaussian doping profile (@51 gate bias steps)
Transfer IV			

I_d-V_g

(linear y-scale)



G_m-V_g



Summary

1. The effect of Lombardi's transverse (and low) field mobility model in a gaussian doped channel in 30nm width (short gate) FinFET can be observed to decrease V_T and decrease $I_d \ \forall V_d$. This is due to the added contribution of surface acoustic phonon (μ_{ac}) and surface roughness scattering (μ_{sr}), to the bulk mobility of the channel (μ_b) using a Matthiesen-like rule:

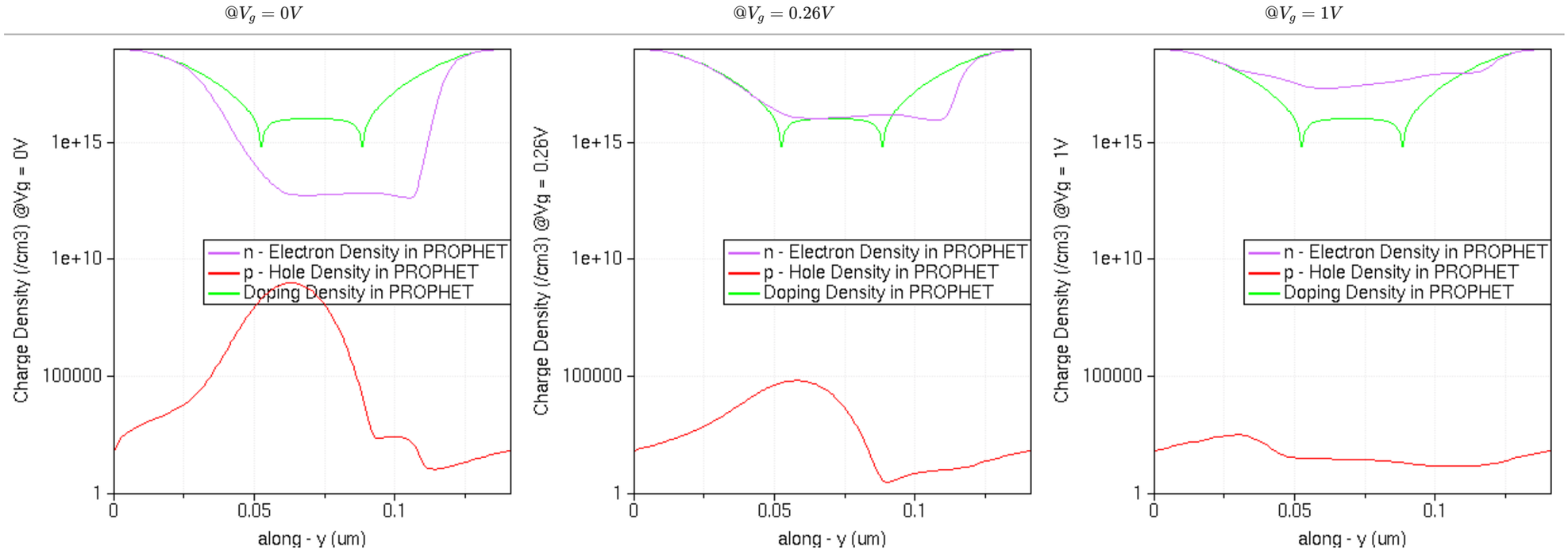
$$\frac{1}{\mu_{lomb}} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_b} \tag{3}$$

Part V: Channel inversion illustration along with MOSFET threshold voltage

Doping, electron density \& hole density simulations at $V_d = 1V$ with 51 (optimum) gate bias steps

With Lombardi's mobility model and gaussian doping profile (characteristic length for source/drain: 20nm, penetration into oxide: 0.05nm, $@51$ gate bias steps)

$@V_g = 0V$ $@V_g = 0.26V$ $@V_g = 1V$



Summary

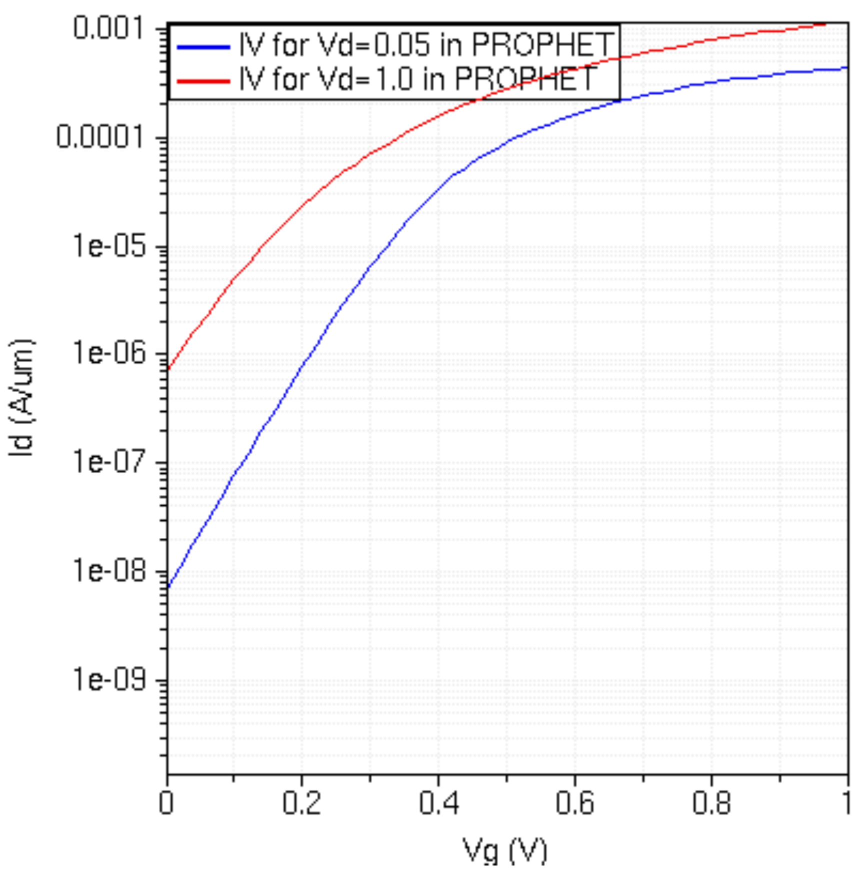
1. The slight askew of electron and hole density near the drain end of the channel in all plots, is indicative of $V_d = 1V$.
2. $@V_g = 0V$, electron density in the channel is lower than doping density, which indicates that very few acceptor dopants in the channel are ionised $(\phi_s < 2 \cdot \phi_b)$.
3. $@V_g = 0.26V$, electron density in the middle of the channel is the same as doping density, which means nearly all acceptor dopants in the channel are ionised $(\phi_s \approx 2 \cdot \phi_b)$. This marks the threshold of charge inversion at the gate-oxide interface in the channel, hence $V_g = 0.26V$ is the threshold voltage.
4. $@V_g = 1V$, electron density in the channel is higher than doping density, which indicates that now an inversion electron layer exists in the channel along the gate-oxide interface $(\phi_s = 2 \cdot \phi_b)$. The very low hole density near the drain end end of the channel also indicates a full saturation of I_d (strong inversion).

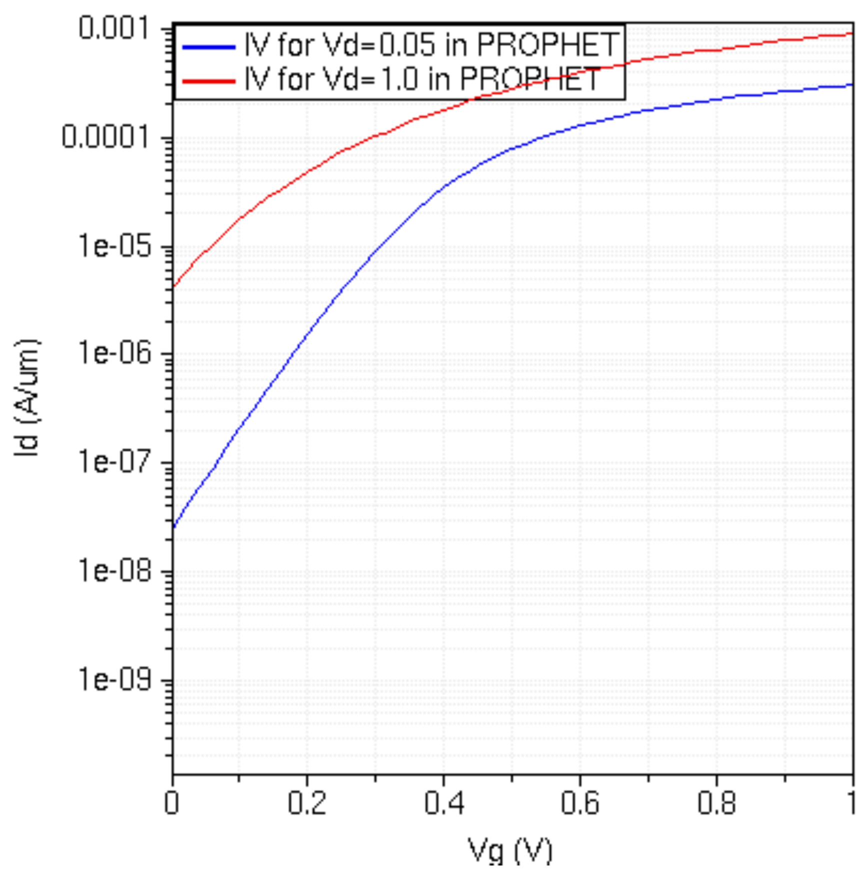
Part VI: Comparison of 30nm width FinFET IV Characteristics vs that of an ultra-thin-body SOI MOSFET

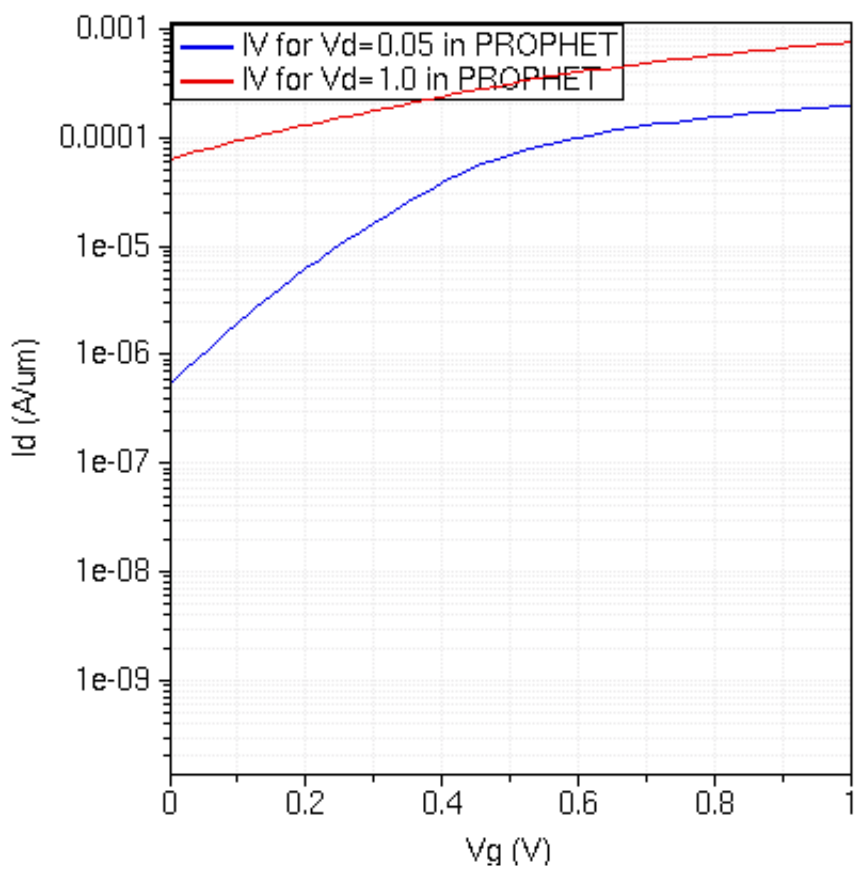
Transfer IV, I_d-V_g and transconductance simulations with 51 (optimum) gate bias steps

	30nm width FinFET (source/drain extension length: 5nm, back gate oxide thickness: 2.5nm) with Lombardi's mobility model \& gaussian doping profile (characteristic length for source/drain: 2nm, penetration into oxide: 0.05nm, @51 gate bias steps)	Ultra-thin-body SOI MOSFET (or 30nm width FinFET with source/drain extension length: 5nm, back gate oxide thickness: 5nm) with Lombardi's mobility model \& gaussian doping profile (characteristic length for source/drain: 2nm, penetration into oxide: 0.05nm, @51 gate bias steps)	Ultra-thin-body SOI (or 30nm width FinFET with source/drain extensio length: 5nm, back gate oxide thickness: 20nm) with Lombardi's mobility model \& gaussian doping profile (characteristic length for source/drain: 2nm, penetration into oxide: 0.05nm, @51 gate bias steps)

Transfer IV

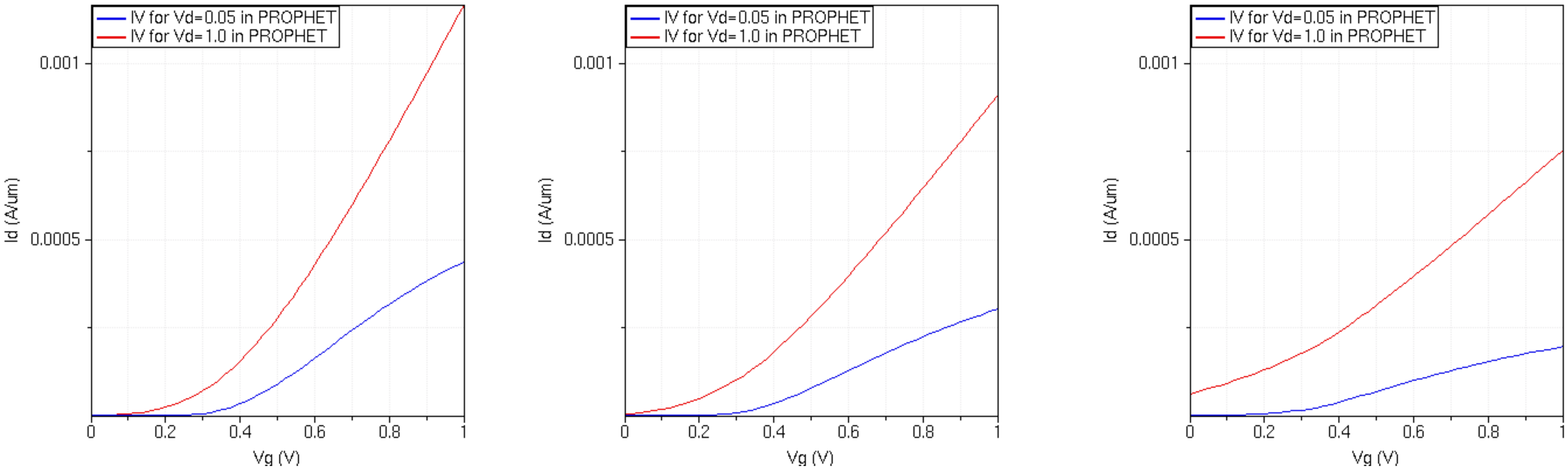




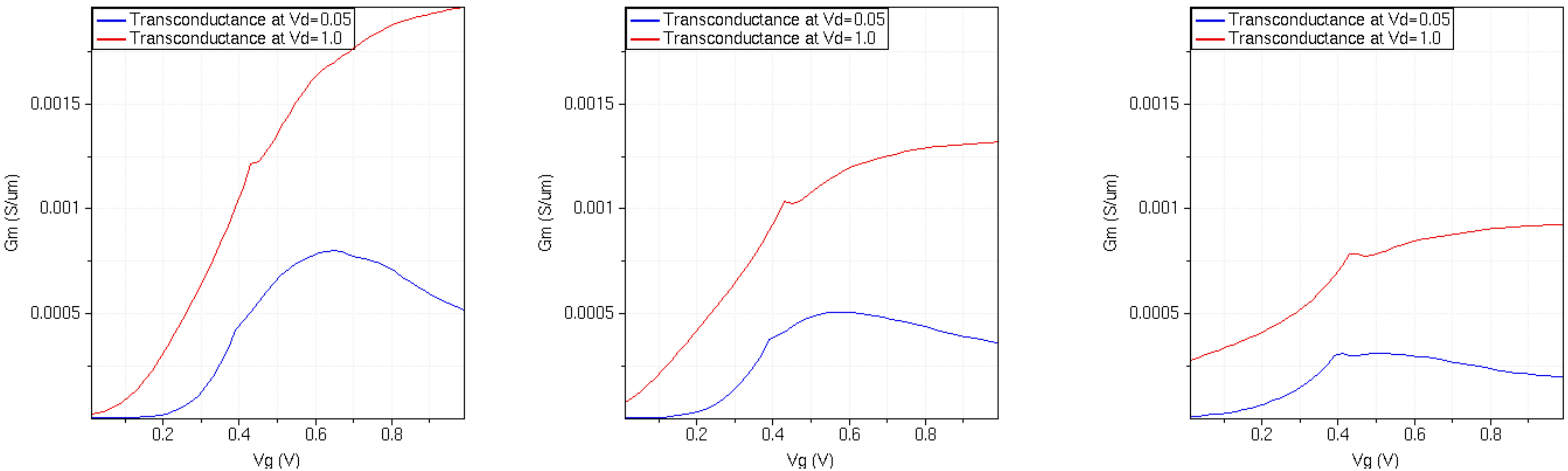


I_d-V_g

(linear y-scale)



G_m-V_g



Summary

1. Effect of increasing back gate oxide thickness (from 2.5nm in FinFET to 20nm in ultra-thin-body SOI MOSFET) can be observed to decrease V_T and decrease $I_d \forall V_d$. This is due to decreasing drain-to-channel capacitance (resulting from increasing body depletion) with increasing back gate oxide thickness.

References

- [1] **Prophet User Reference Guide**

Additional information

Created by: Rochish Manda, MSc KTH

IH2653 Examiner: Dr. Gunnar Malm, Professor KTH

Data and config file at: **Github**