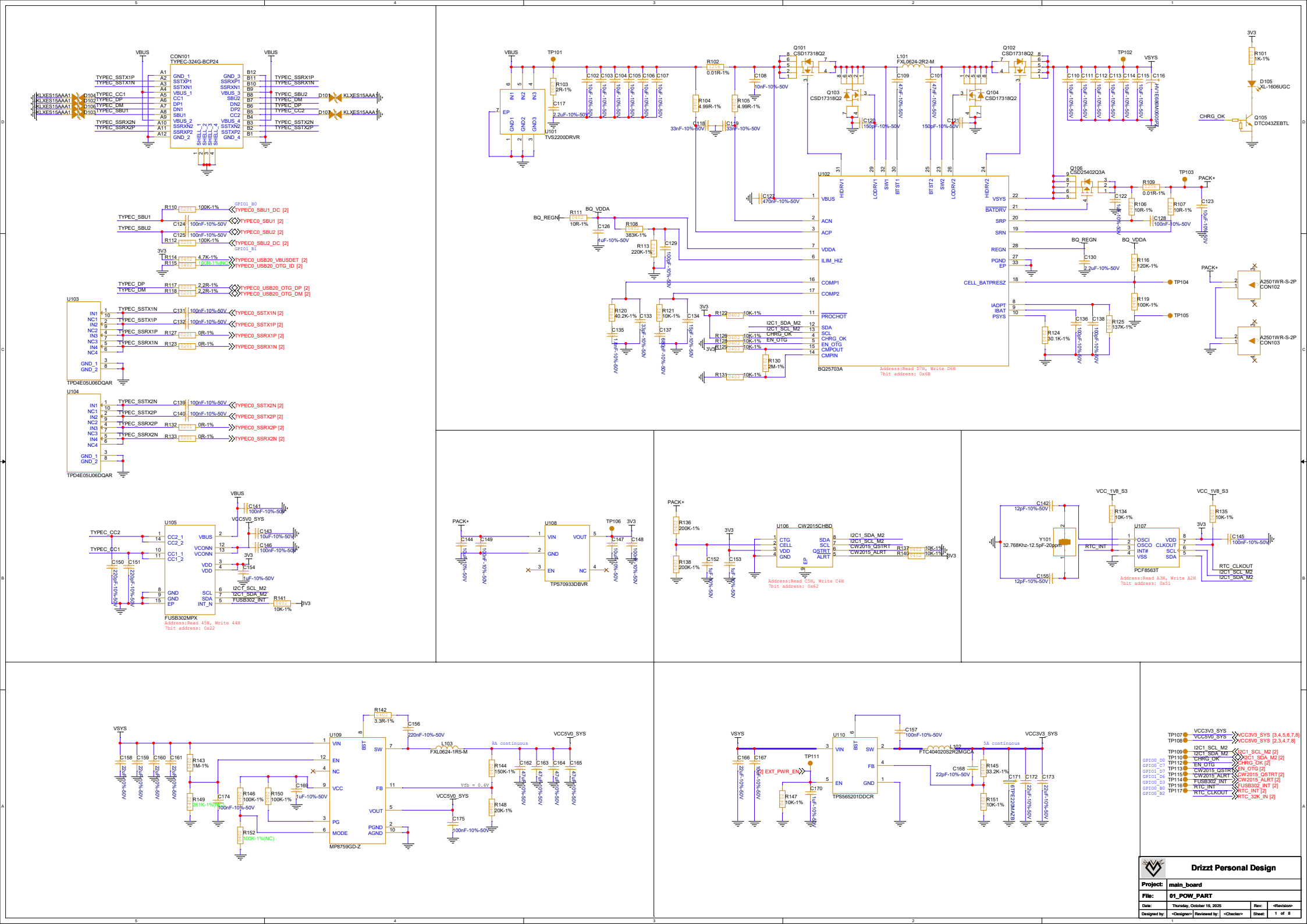
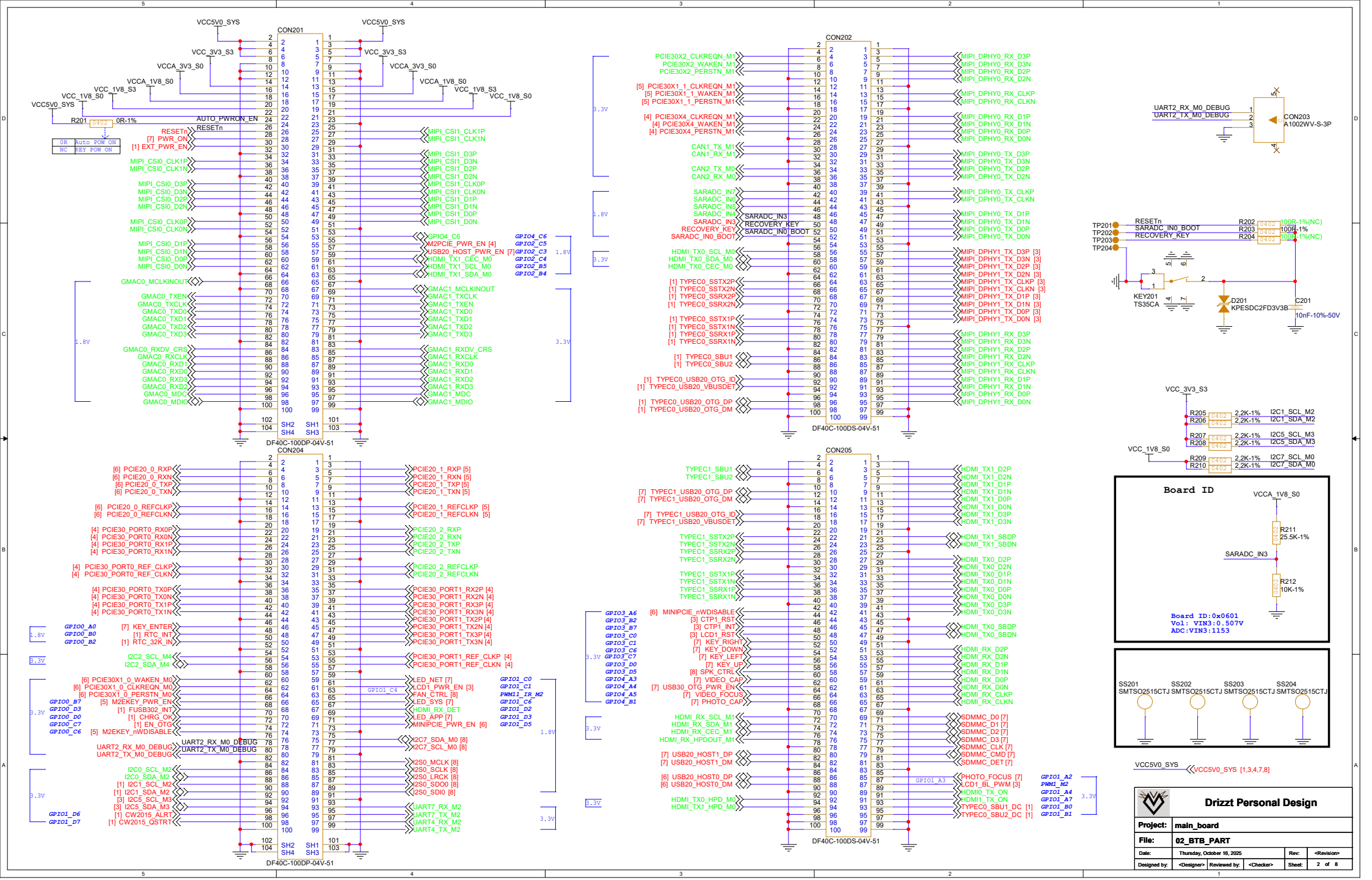
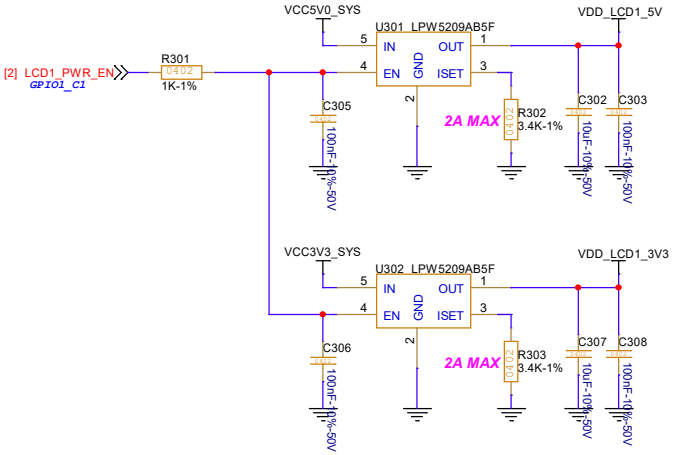
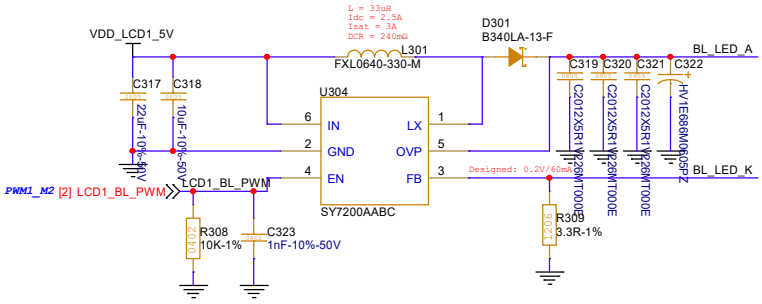
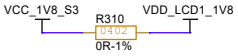
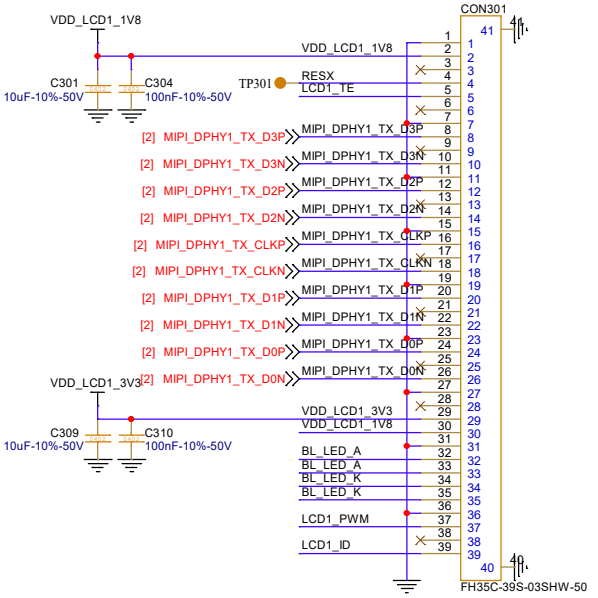

CON101
TYPEC-324G-BCP24
TVS2200DRVR
FXL0624-2R2-M
CSD17318Q2
CSD25402Q3A
BQ25703A
TPS565201DDCR
MP8759GD-Z
TPS70933DBVR
FUSB302MPX
TPD4E05U06DQAR
PCF8563T
CW2015CHBD
A2501WR-S-2P
XL-1606UGC
DTC043ZEBTL
Drizzt Personal Design
Project: main_board
File: 01_POW_PART
Date: Thursday, October 16, 2025
Designed by: <Designer>
Reviewed by: <Checker>
Rev: <Revision>
Sheet: 1 of 8

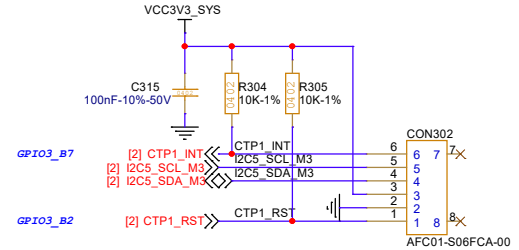

CON201
CON202
CON203
CON204
CON205
DF40C-100DP-04V-51
DF40C-100DS-04V-51
A1002WV-S-3P
VCC5V0_SYS
VCC_3V3_S3
VCCA_3V3_S0
VCCA_1V8_S0
VCC_1V8_S3
VCC_1V8_S0
R201 0402 0R-1%
AUTO_PWRON_EN
RESETn
[7] PWR_ON
[1] EXT_PWR_EN
0R Auto POW ON
NC KEY POW ON
MIPI_CSI0_CLK1P
MIPI_CSI0_CLK1N
MIPI_CSI0_D3P
MIPI_CSI0_D3N
MIPI_CSI0_D2P
MIPI_CSI0_D2N
MIPI_CSI0_CLK0P
MIPI_CSI0_CLK0N
MIPI_CSI0_D1P
MIPI_CSI0_D1N
MIPI_CSI0_D0P
MIPI_CSI0_D0N
GMAC0_MCLKINOUT
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
GMAC0_RXD1
GMAC0_RXD0
GMAC0_RXD3
GMAC0_RXD2
GMAC0_MDC
GMAC0_MDIO
MIPI_CSI1_CLK1P
MIPI_CSI1_CLK1N
MIPI_CSI1_D3P
MIPI_CSI1_D3N
MIPI_CSI1_D2P
MIPI_CSI1_D2N
MIPI_CSI1_CLK0P
MIPI_CSI1_CLK0N
MIPI_CSI1_D1P
MIPI_CSI1_D1N
MIPI_CSI1_D0P
MIPI_CSI1_D0N
GPIO4_C6
M2PCIE_PWR_EN [4]
USB20_HOST_PWR_EN [7]
HDMI_TX1_CEC_M0
HDMI_TX1_SCL_M0
HDMI_TX1_SDA_M0
GMAC1_MCLKINOUT
GMAC1_TXCLK
GMAC1_TXEN
GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_RXDV_CRS
GMAC1_RXCLK
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_MDC
GMAC1_MDIO
PCIE30X2_CLKREQN_M1
PCIE30X2_WAKEN_M1
PCIE30X2_PERSTN_M1
[5] PCIE30X1_1_CLKREQN_M1
[5] PCIE30X1_1_WAKEN_M1
[5] PCIE30X1_1_PERSTN_M1
[4] PCIE30X4_CLKREQN_M1
[4] PCIE30X4_WAKEN_M1
[4] PCIE30X4_PERSTN_M1
CAN1_TX_M1
CAN1_RX_M1
CAN2_TX_M0
CAN2_RX_M0
SARADC_IN7
SARADC_IN6
SARADC_IN5
SARADC_IN4
SARADC_IN3
RECOVERY_KEY
SARADC_IN0_BOOT
HDMI_TX0_SCL_M0
HDMI_TX0_SDA_M0
HDMI_TX0_CEC_M0
[1] TYPEC0_SSTX2P
[1] TYPEC0_SSTX2N
[1] TYPEC0_SSRX2P
[1] TYPEC0_SSRX2N
[1] TYPEC0_SSTX1P
[1] TYPEC0_SSTX1N
[1] TYPEC0_SSRX1P
[1] TYPEC0_SSRX1N
[1] TYPEC0_SBU1
[1] TYPEC0_SBU2
[1] TYPEC0_USB20_OTG_ID
[1] TYPEC0_USB20_VBUSDET
[1] TYPEC0_USB20_OTG_DP
[1] TYPEC0_USB20_OTG_DM
MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N
MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N
MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N
MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N
MIPI_DPHY1_TX_D3P [3]
MIPI_DPHY1_TX_D3N [3]
MIPI_DPHY1_TX_D2P [3]
MIPI_DPHY1_TX_D2N [3]
MIPI_DPHY1_TX_CLKP [3]
MIPI_DPHY1_TX_CLKN [3]
MIPI_DPHY1_TX_D1P [3]
MIPI_DPHY1_TX_D1N [3]
MIPI_DPHY1_TX_D0P [3]
MIPI_DPHY1_TX_D0N [3]
MIPI_DPHY1_RX_D3P
MIPI_DPHY1_RX_D3N
MIPI_DPHY1_RX_D2P
MIPI_DPHY1_RX_D2N
MIPI_DPHY1_RX_CLKP
MIPI_DPHY1_RX_CLKN
MIPI_DPHY1_RX_D1P
MIPI_DPHY1_RX_D1N
MIPI_DPHY1_RX_D0P
MIPI_DPHY1_RX_D0N
UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG
TP201
TP202
TP203
TP204
RESETn
SARADC_IN0_BOOT
RECOVERY_KEY
R202 0402 100R-1%(NC)
R203 0402 100R-1%
R204 0402 100R-1%(NC)
KEY201
TS35CA
D201
KPESDC2FD3V3B
C201
10nF-10%-50V
R205 0402 2.2K-1% I2C1_SCL_M2
R206 0402 2.2K-1% I2C1_SDA_M2
R207 0402 2.2K-1% I2C5_SCL_M3
R208 0402 2.2K-1% I2C5_SDA_M3
R209 0402 2.2K-1% I2C7_SCL_M0
R210 0402 2.2K-1% I2C7_SDA_M0
Board ID
R211 25.5K-1%
R212 10K-1%
Board ID:0x0601
Vol: VIN3:0.507V
ADC:VIN3:1153
SS201 SMTSO2515CTJ
SS202 SMTSO2515CTJ
SS203 SMTSO2515CTJ
SS204 SMTSO2515CTJ
[6] PCIE20_0_RXP
[6] PCIE20_0_RXN
[6] PCIE20_0_TXP
[6] PCIE20_0_TXN
[6] PCIE20_0_REFCLKP
[6] PCIE20_0_REFCLKN
[4] PCIE30_PORT0_RX0P
[4] PCIE30_PORT0_RX0N
[4] PCIE30_PORT0_RX1P
[4] PCIE30_PORT0_RX1N
[4] PCIE30_PORT0_REF_CLKP
[4] PCIE30_PORT0_REF_CLKN
[4] PCIE30_PORT0_TX0P
[4] PCIE30_PORT0_TX0N
[4] PCIE30_PORT0_TX1P
[4] PCIE30_PORT0_TX1N
[7] KEY_ENTER
[1] RTC_INT
[1] RTC_32K_IN
I2C2_SCL_M4
I2C2_SDA_M4
[6] PCIE30X1_0_WAKEN_M0
[6] PCIE30X1_0_CLKREQN_M0
[6] PCIE30X1_0_PERSTN_M0
[5] M2EKEY_PWR_EN
[1] FUSB302_INT
[1] CHRG_OK
[1] EN_OTG
[5] M2EKEY_nWDISABLE
UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG
I2C0_SCL_M2
I2C0_SDA_M2
[1] I2C1_SCL_M2
[1] I2C1_SDA_M2
[3] I2C5_SCL_M3
[3] I2C5_SDA_M3
[1] CW2015_ALRT
[1] CW2015_QSTRT
PCIE20_1_RXP [5]
PCIE20_1_RXN [5]
PCIE20_1_TXP [5]
PCIE20_1_TXN [5]
PCIE20_1_REFCLKP [5]
PCIE20_1_REFCLKN [5]
PCIE20_2_RXP
PCIE20_2_RXN
PCIE20_2_TXP
PCIE20_2_TXN
PCIE20_2_REFCLKP
PCIE20_2_REFCLKN
PCIE30_PORT1_RX2P [4]
PCIE30_PORT1_RX2N [4]
PCIE30_PORT1_RX3P [4]
PCIE30_PORT1_RX3N [4]
PCIE30_PORT1_TX2P [4]
PCIE30_PORT1_TX2N [4]
PCIE30_PORT1_TX3P [4]
PCIE30_PORT1_TX3N [4]
PCIE30_PORT1_REF_CLKP [4]
PCIE30_PORT1_REF_CLKN [4]
LED_NET [7]
LCD1_PWR_EN [3]
FAN_CTRL [8]
LED_SYS [7]
HDMI_RX_DET
LED_APP [7]
MINIPCIE_PWR_EN [6]
I2C7_SDA_M0 [8]
I2C7_SCL_M0 [8]
I2S0_MCLK [8]
I2S0_SCLK [8]
I2S0_LRCK [8]
I2S0_SDO0 [8]
I2S0_SDI0 [8]
UART7_RX_M2
UART7_TX_M2
UART4_RX_M2
UART4_TX_M2
TYPEC1_SBU1
TYPEC1_SBU2
[7] TYPEC1_USB20_OTG_DP
[7] TYPEC1_USB20_OTG_DM
[7] TYPEC1_USB20_OTG_ID
[7] TYPEC1_USB20_VBUSDET
TYPEC1_SSTX2P
TYPEC1_SSTX2N
TYPEC1_SSRX2P
TYPEC1_SSRX2N
TYPEC1_SSTX1P
TYPEC1_SSTX1N
TYPEC1_SSRX1P
TYPEC1_SSRX1N
[6] MINIPCIE_nWDISABLE
[3] CTP1_RST
[3] CTP1_INT
[3] LCD1_RST
[7] KEY_RIGHT
[7] KEY_DOWN
[7] KEY_LEFT
[7] KEY_UP
[8] SPK_CTRL
[7] VIDEO_CAP
[7] USB30_OTG_PWR_EN
[7] VIDEO_FOCUS
[7] PHOTO_CAP
HDMI_RX_SCL_M1
HDMI_RX_SDA_M1
HDMI_RX_CEC_M1
HDMI_RX_HPDOUT_M1
[7] USB20_HOST1_DP
[7] USB20_HOST1_DM
[6] USB20_HOST0_DP
[6] USB20_HOST0_DM
HDMI_TX0_HPD_M0
HDMI_TX1_HPD_M0
HDMI_TX1_D2P
HDMI_TX1_D2N
HDMI_TX1_D1P
HDMI_TX1_D1N
HDMI_TX1_D0P
HDMI_TX1_D0N
HDMI_TX1_D3P
HDMI_TX1_D3N
HDMI_TX1_SBDP
HDMI_TX1_SBDN
HDMI_TX0_D2P
HDMI_TX0_D2N
HDMI_TX0_D1P
HDMI_TX0_D1N
HDMI_TX0_D0P
HDMI_TX0_D0N
HDMI_TX0_D3P
HDMI_TX0_D3N
HDMI_TX0_SBDP
HDMI_TX0_SBDN
HDMI_RX_D2P
HDMI_RX_D2N
HDMI_RX_D1P
HDMI_RX_D1N
HDMI_RX_D0P
HDMI_RX_D0N
HDMI_RX_CLKP
HDMI_RX_CLKN
SDMMC_D0 [7]
SDMMC_D1 [7]
SDMMC_D2 [7]
SDMMC_D3 [7]
SDMMC_CLK [7]
SDMMC_CMD [7]
SDMMC_DET [7]
PHOTO_FOCUS [7]
LCD1_BL_PWM [3]
HDMI0_TX_ON
HDMI1_TX_ON
TYPEC0_SBU1_DC [1]
TYPEC0_SBU2_DC [1]
VCC5V0_SYS [1,3,4,7,8]
Drizzt Personal Design
Project: main_board
File: 02_BTB_PART
Date: Thursday, October 16, 2025
Rev: <Revision>
Designed by: <Designer>
Reviewed by: <Checker>
Sheet: 2 of 8

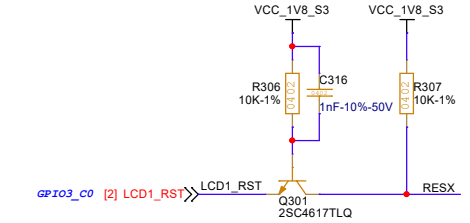






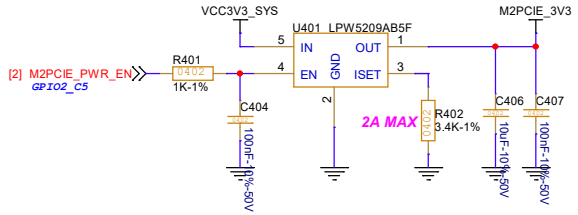


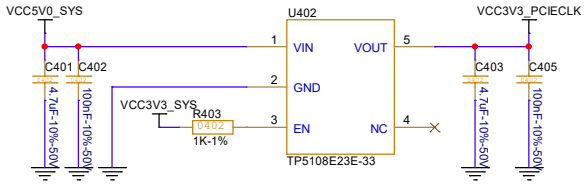


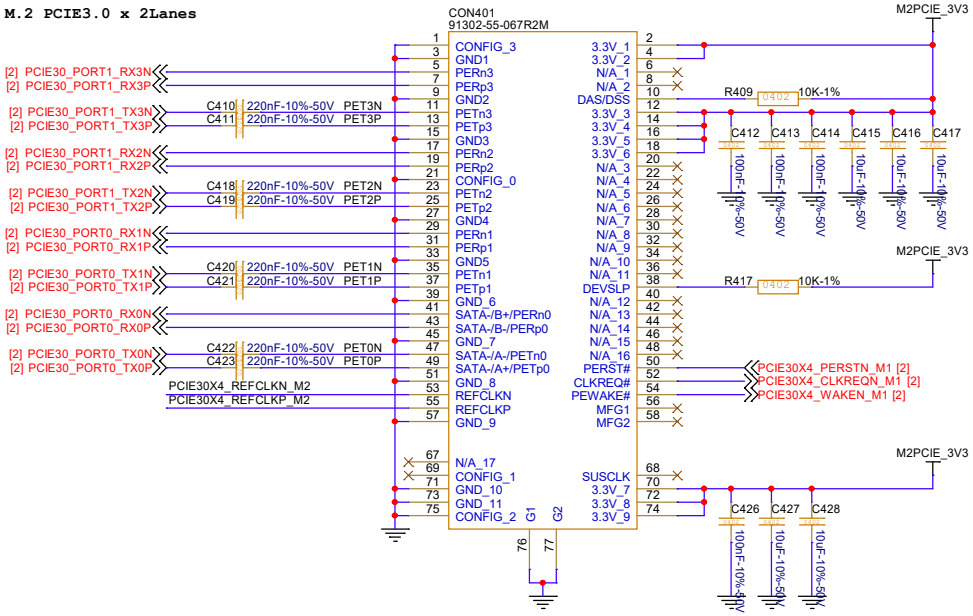


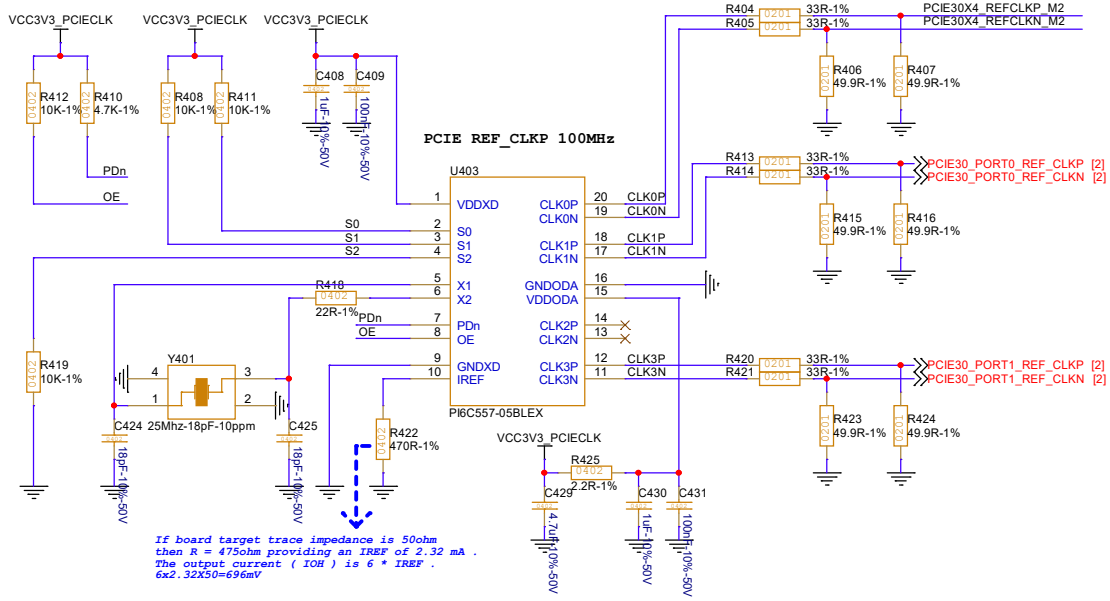
VCC3V3_SYS
VCC5V0_SYS
VCC3V3_SYS [1,4,5,6,7,8]
VCC5V0_SYS [1,2,4,7,8]

Drizzt Personal Design					
Project:	**main_board**				
File:	**03_DSI_PART**				
Date:	Friday, September 26, 2025			Rev:	<Revision>
Designed by:	<Designer>	Reviewed by:	<Checker>	Sheet:	3 of 8





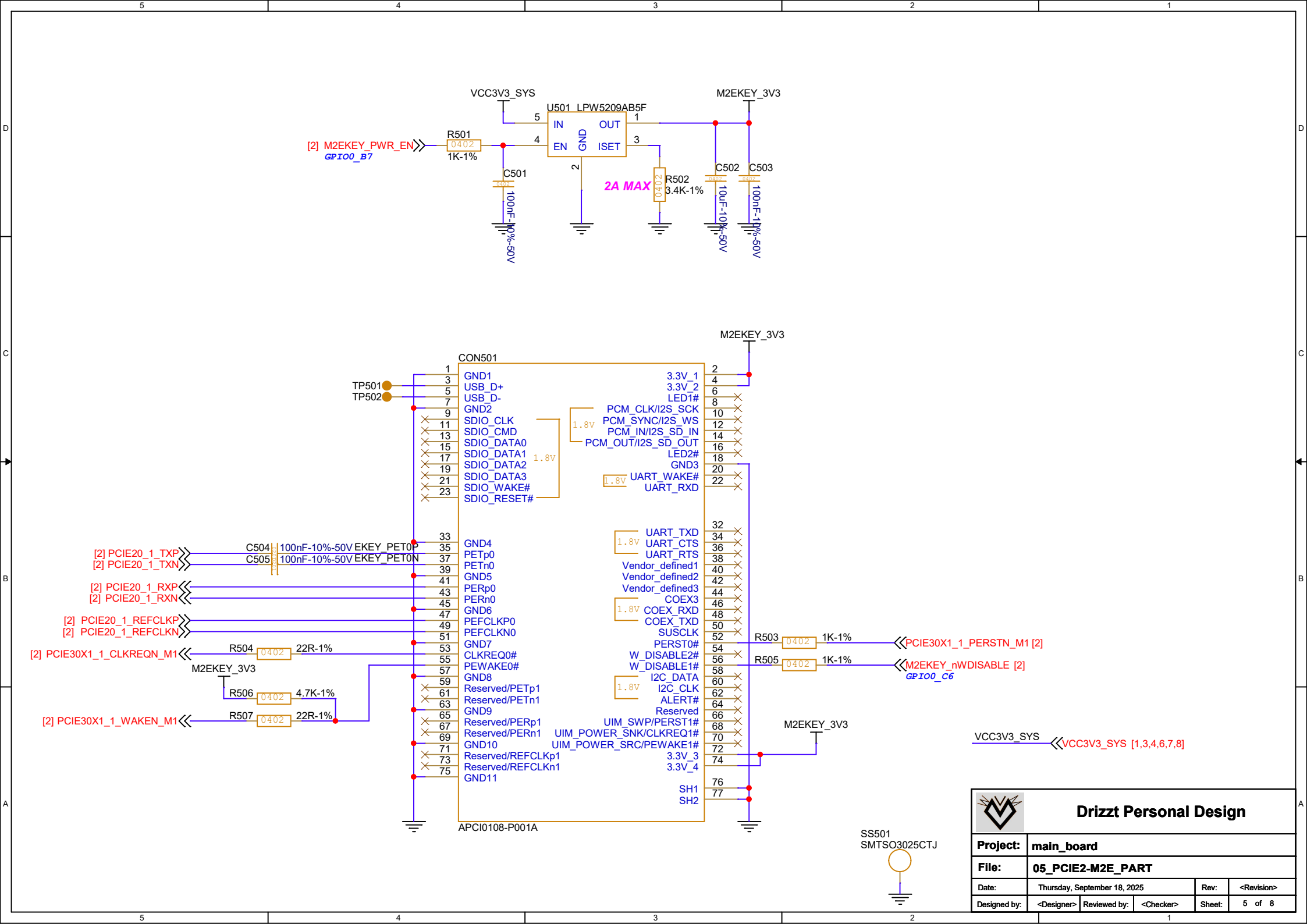


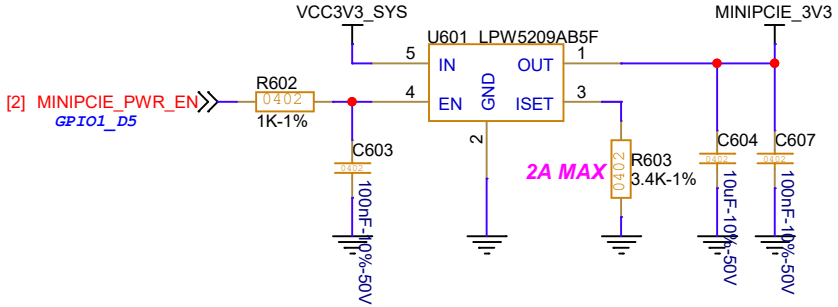


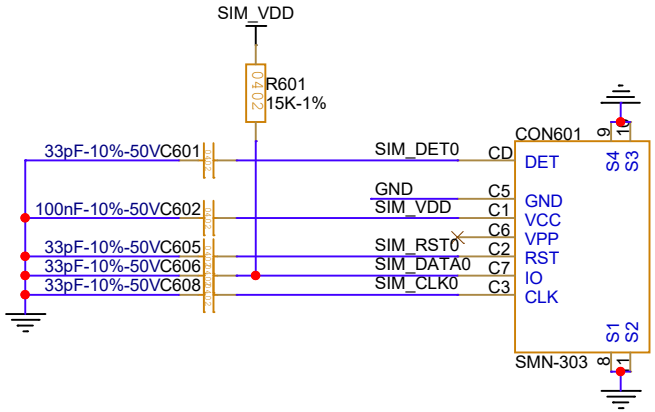
VCC3V3_SYS
VCC5V0_SYS
VCC3V3_SYS [1,3,5,6,7,8]
VCC5V0_SYS [1,2,3,7,8]

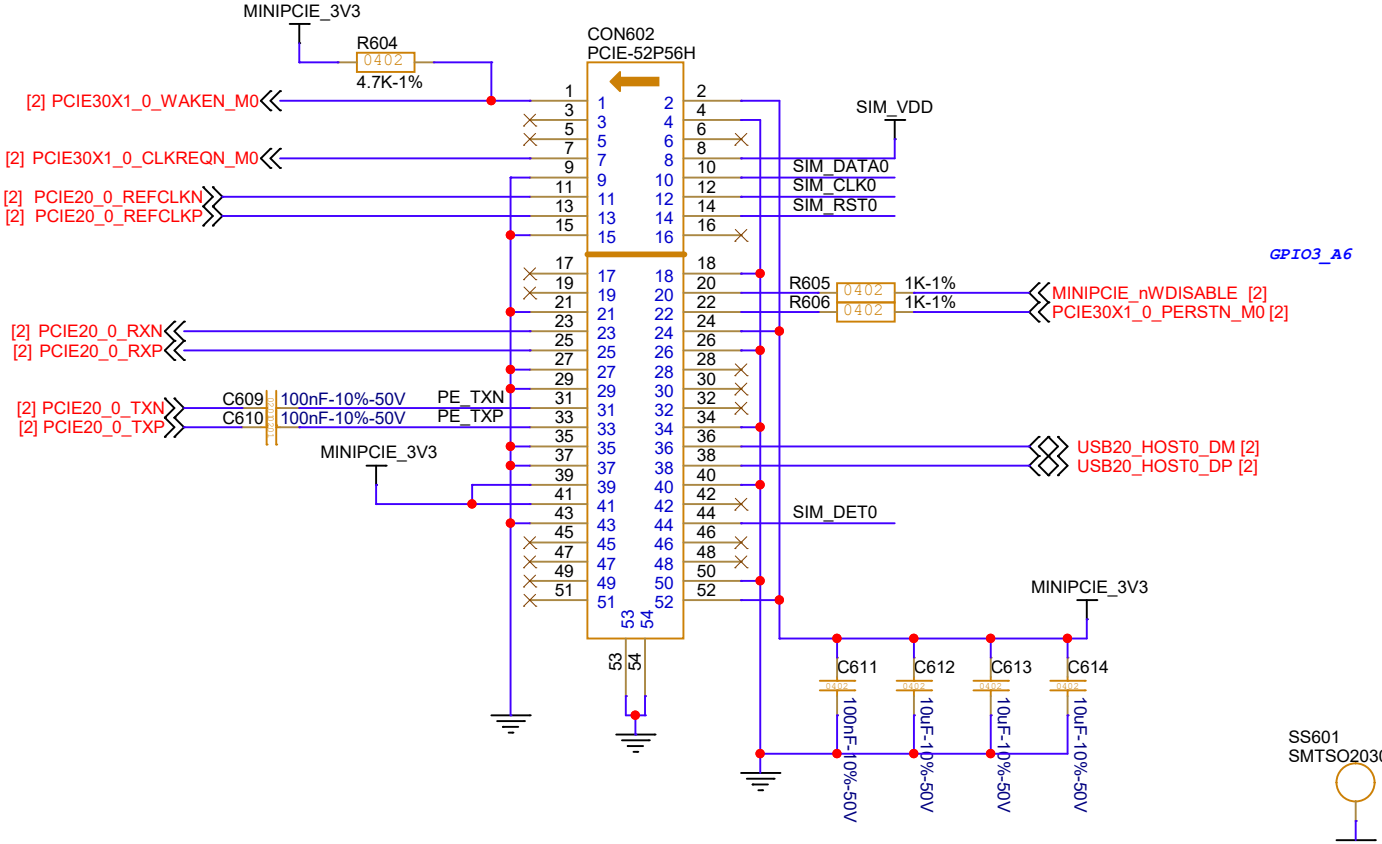
SS401
SMTSO3035CTJ

Drizzt Personal Design					
Project:	main_board				
File:	04_PCIE3-M2M_PART				
Date:	Thursday, September 18, 2025			Rev:	<Revision>
Designed by:	<Designer>	Reviewed by:	<Checker>	Sheet:	4 of 8


VCC3V3_SYS
M2EKEY_3V3
U501 LPW5209AB5F
IN
OUT
EN
GND
ISET
[2] M2EKEY_PWR_EN
GPIO0_B7
R501
1K-1%
C501
100nF-10%-50V
2A MAX
R502
3.4K-1%
C502
10uF-10%-50V
C503
100nF-10%-50V
CON501
TP501
TP502
GND1
USB_D+
USB_D-
GND2
SDIO_CLK
SDIO_CMD
SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SDIO_DATA3
SDIO_WAKE#
SDIO_RESET#
3.3V_1
3.3V_2
LED1#
PCM_CLK/I2S_SCK
PCM_SYNC/I2S_WS
PCM_IN/I2S_SD_IN
PCM_OUT/I2S_SD_OUT
LED2#
GND3
UART_WAKE#
UART_RXD
UART_TXD
UART_CTS
UART_RTS
Vendor_defined1
Vendor_defined2
Vendor_defined3
COEX3
COEX_RXD
COEX_TXD
SUSCLK
PERST0#
W_DISABLE2#
W_DISABLE1#
I2C_DATA
I2C_CLK
ALERT#
Reserved
UIM_SWP/PERST1#
UIM_POWER_SNK/CLKREQ1#
UIM_POWER_SRC/PEWAKE1#
3.3V_3
3.3V_4
SH1
SH2
GND4
PETp0
PETn0
GND5
PERp0
PERn0
GND6
PEFCLKP0
PEFCLKN0
GND7
CLKREQ0#
PEWAKE0#
GND8
Reserved/PETp1
Reserved/PETn1
GND9
Reserved/PERp1
Reserved/PERn1
GND10
Reserved/REFCLKp1
Reserved/REFCLKn1
GND11
APCI0108-P001A
C504
C505
100nF-10%-50V
EKEY_PET0P
EKEY_PET0N
[2] PCIE20_1_TXP
[2] PCIE20_1_TXN
[2] PCIE20_1_RXP
[2] PCIE20_1_RXN
[2] PCIE20_1_REFCLKP
[2] PCIE20_1_REFCLKN
[2] PCIE30X1_1_CLKREQN_M1
R504
22R-1%
M2EKEY_3V3
R506
4.7K-1%
[2] PCIE30X1_1_WAKEN_M1
R507
22R-1%
R503
1K-1%
PCIE30X1_1_PERSTN_M1 [2]
R505
1K-1%
M2EKEY_nWDISABLE [2]
GPIO0_C6
M2EKEY_3V3
VCC3V3_SYS
VCC3V3_SYS [1,3,4,6,7,8]
SS501
SMTSO3025CTJ
Drizzt Personal Design
Project: main_board
File: 05_PCIE2-M2E_PART
Date: Thursday, September 18, 2025
Rev: <Revision>
Designed by: <Designer>
Reviewed by: <Checker>
Sheet: 5 of 8





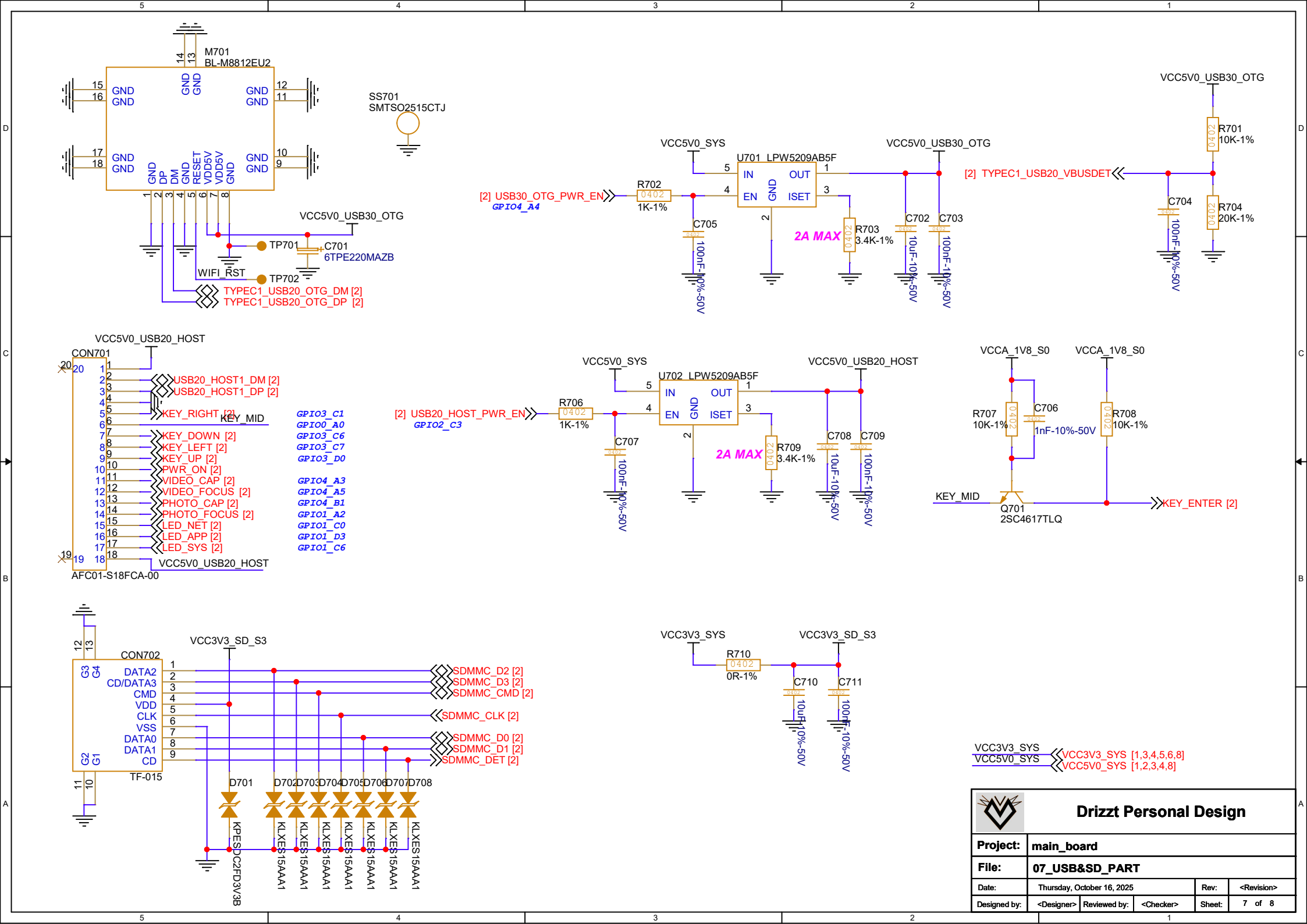


VCC3V3_SYS
VCC3V3_SYS [1,3,4,5,7,8]

SS601 SMTSO2030CTJ

SS602 SMTSO2030CTJ

Drizzt Personal Design					
Project:	**main_board**				
File:	**06_MINI-PCIE_PART**				
Date:	Friday, September 26, 2025			Rev:	<Revision>
Designed by:	<Designer>	Reviewed by:	<Checker>	Sheet:	6 of 8


M701
BL-M8812EU2
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
GND
DP
DM
RESET
VDD5V
VDD5V
SS701
SMTSO2515CTJ
VCC5V0_USB30_OTG
TP701
C701
6TPE220MAZB
WIFI_RST
TP702
TYPEC1_USB20_OTG_DM [2]
TYPEC1_USB20_OTG_DP [2]
VCC5V0_SYS
U701 LPW5209AB5F
IN
OUT
EN
GND
ISET
[2] USB30_OTG_PWR_EN
GPIO4_A4
R702
1K-1%
C705
100nF-10%-50V
2A MAX
R703
3.4K-1%
C702
10uF-10%-50V
C703
100nF-10%-50V
VCC5V0_USB30_OTG
R701
10K-1%
[2] TYPEC1_USB20_VBUSDET
C704
100nF-10%-50V
R704
20K-1%
VCC5V0_USB20_HOST
CON701
AFC01-S18FCA-00
USB20_HOST1_DM [2]
USB20_HOST1_DP [2]
KEY_RIGHT [2]
KEY_MID
KEY_DOWN [2]
KEY_LEFT [2]
KEY_UP [2]
PWR_ON [2]
VIDEO_CAP [2]
VIDEO_FOCUS [2]
PHOTO_CAP [2]
PHOTO_FOCUS [2]
LED_NET [2]
LED_APP [2]
LED_SYS [2]
VCC5V0_USB20_HOST
GPIO3_C1
GPIO0_A0
GPIO3_C6
GPIO3_C7
GPIO3_D0
GPIO4_A3
GPIO4_A5
GPIO4_B1
GPIO1_A2
GPIO1_C0
GPIO1_D3
GPIO1_C6
VCC5V0_SYS
U702 LPW5209AB5F
IN
OUT
EN
GND
ISET
[2] USB20_HOST_PWR_EN
GPIO2_C3
R706
1K-1%
C707
100nF-10%-50V
2A MAX
R709
3.4K-1%
C708
10uF-10%-50V
C709
100nF-10%-50V
VCC5V0_USB20_HOST
VCCA_1V8_S0
VCCA_1V8_S0
R707
10K-1%
C706
1nF-10%-50V
R708
10K-1%
KEY_MID
Q701
2SC4617TLQ
KEY_ENTER [2]
CON702
TF-015
VCC3V3_SD_S3
DATA2
CD/DATA3
CMD
VDD
CLK
VSS
DATA0
DATA1
CD
SDMMC_D2 [2]
SDMMC_D3 [2]
SDMMC_CMD [2]
SDMMC_CLK [2]
SDMMC_D0 [2]
SDMMC_D1 [2]
SDMMC_DET [2]
D701
D702
D703
D704
D705
D706
D707
D708
KPESDC2FD3V3B
KLXES15AAA1
VCC3V3_SYS
VCC3V3_SD_S3
R710
0R-1%
C710
10uF-10%-50V
C711
100nF-10%-50V
VCC3V3_SYS
VCC5V0_SYS
VCC3V3_SYS [1,3,4,5,6,8]
VCC5V0_SYS [1,2,3,4,8]
Drizzt Personal Design
Project: main_board
File: 07_USB&SD_PART
Date: Thursday, October 16, 2025
Rev: <Revision>
Designed by: <Designer>
Reviewed by: <Checker>
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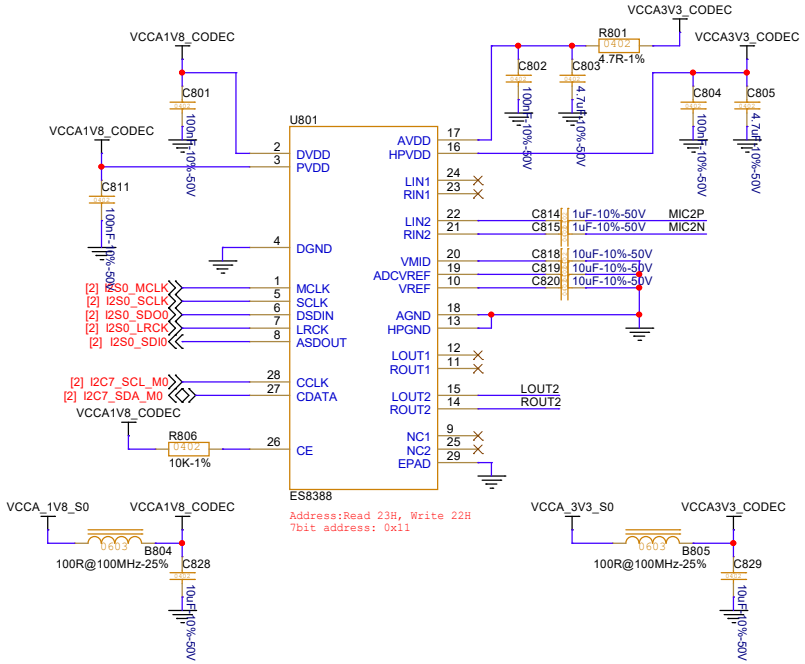

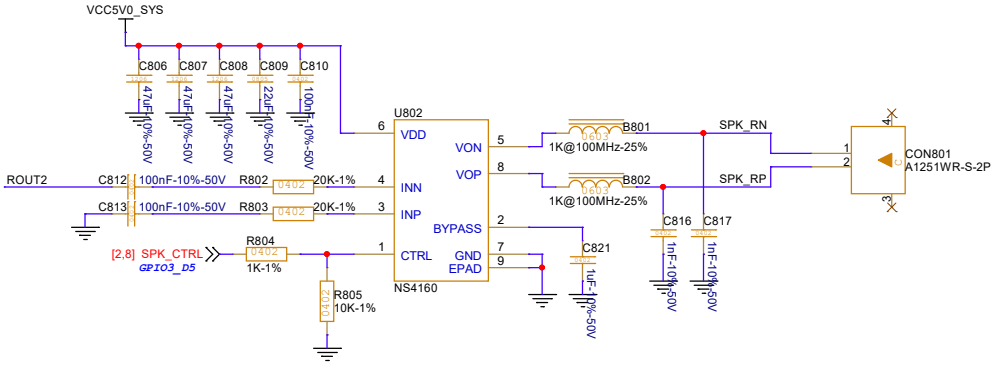

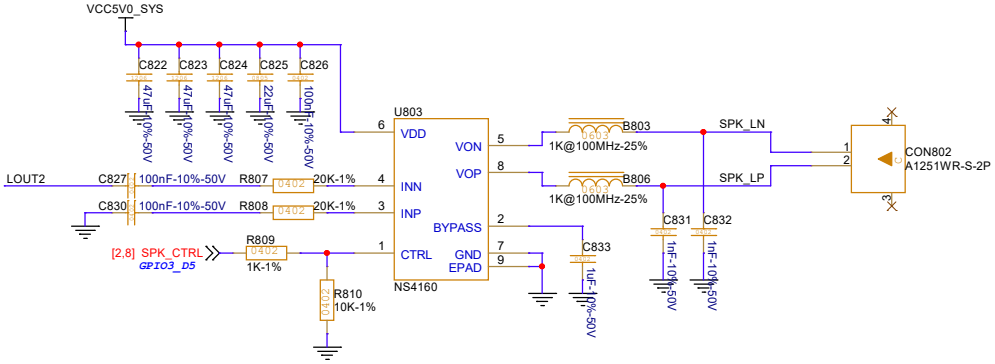

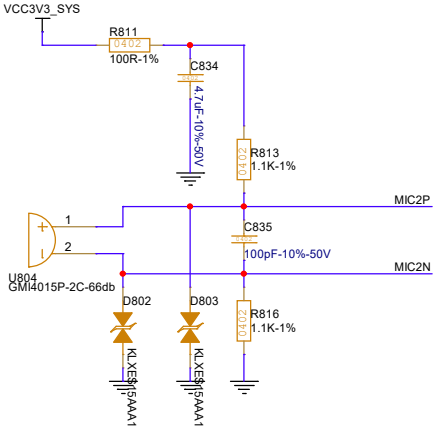

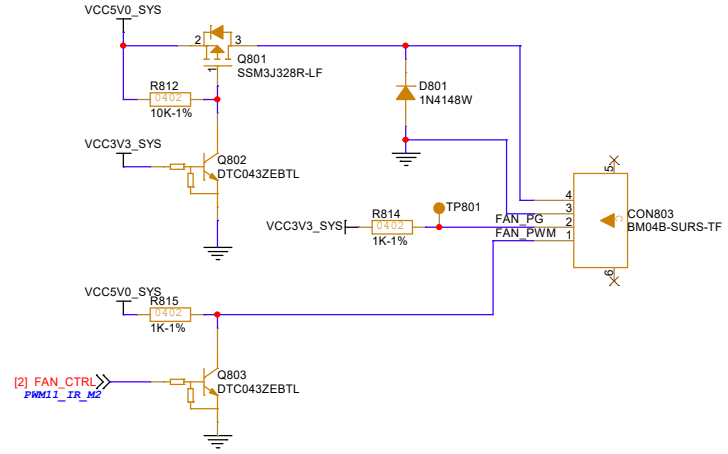

VCC3V3_SYS
VCC5V0_SYS

VCC3V3_SYS [1,3,4,5,6,7]
VCC5V0_SYS [1,2,3,4,7]

Drizzt Personal Design					
Project:	**main_board**				
File:	**08_AUDIO&FAN_PART**				
Date:	Wednesday, September 24, 2025			Rev:	<Revision>
Designed by:	<Designer>	Reviewed by:	<Checker>	Sheet:	8 of 8