Washington State University School of Electrical Engineering and Computer Science

EE 352 Electrical Engineering Laboratory

Lab # 3

Operational Amplifier Applications

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Lab Overview

To purpose of this lab was to use operational amplifiers to design, analyze and implement a few variations of simple and practical circuits. The first circuit is a first-order active high pass filter, the second one is an operational amplifier with high gain, high input resistance and low output resistance.

Experiment #1 First Order High Pass Active Filter

1.1 Purpose

Using LTSPICE, the purpose of this lab was to create a first order high pass active filter and analyze its components. These components included the step response, frequency response, and the sinusoidal response.

1.2 Theoretical Background

Operational amplifiers (Op-amps) are most used to implement filtering operations. Like the passive filter in Lab 1, the active first order high pass filter generates a frequency response and a step response for the circuit. Unlike the passive filter, there is a maximum pass band frequency which is limited to the bandwidth of the op-amp being used. This makes them appear as if they are band pass filters with a high frequency cut-off that would be determined by the selection of op-amp and the gain of the op-amp. To demonstrate this, Fig.1 below shows the first order high pass filter used in experiment 1.

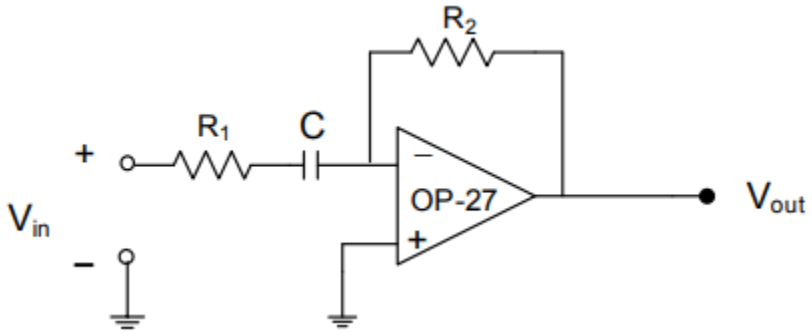

Figure 1: First order op-amp high pass filter.

To successfully conduct this experiment, the differential equation for the output voltage of the circuit shown in Fig. 1 assuming an ideal circuit, and there is no initial charge on the capacitor at t=0- was calculated along with finding the initial conditions. To find this, equation (1) was used to calculate the gain (G) with $\omega = 0, and\ \omega = \infty$ and the high frequency gain (k).

$$G = \frac{k\frac{j\omega}{\omega_0}}{1+\frac{j\omega}{\omega_0}} \qquad (1)$$

When $\omega = 0$, G=$\infty dB\ or\ 0\frac{V}{V}$. When $\omega = \infty$, G=k. Then equation (2) was used to find the initial conditions $j\omega_0, and\ \frac{dV_0}{dt}$. The resistor and capacitor variables in equation (2) are the ones represented in Fig. 1.

$$G(j\omega) = \frac{V_0}{V_I}(j\omega) = \left(-\frac{R_2}{R_1}\right)\frac{j\omega CR_1}{1+j\omega CR_1} \qquad (2)$$

Which let to equation (3)

$$G(j\omega) = \left(-\frac{R_2}{R_1}\right)\frac{k\frac{j\omega}{\omega_0}}{1+\frac{j\omega}{\omega_0}}\ where\ j\omega_0 = \frac{1}{CR_1} \qquad (3)$$

To then find $\frac{dV_0}{dt}$, it is known for the circuit that $I_c = I_1 = I_2$, $I_2 = \frac{CdV_c}{dt}$, and $V_c = V_I - I_1R_1$. Using this, equation (4) is the final derivation.

$$\frac{dV_0}{dt} = -(\frac{R_2}{R_1}\frac{dV_I}{dt} + \frac{V_0(t)}{R_1C}) \qquad (4)$$

To then find the analytical expression for the step response and the time constant τ, The same conditions as well as the results were used as above. Since τ is found in $\omega = \frac{1}{\tau}$=$\frac{1}{CR_1}$; this means τ= CR_1. Since the charge on the capacitor is 0 when t=0-, it is stated in equation (5) as follows:

$$V_I(t) = \begin{cases} 1 & t > 0 \\ 0 & t < 0 \end{cases} \qquad (5)$$

This including that all initial conditions are equal to 0 including V(0-)=V(0+)=0. Therefore the concluded analytical expression is shown in equation (6).

$$V_0(t) = [V_0(0+) - V(\infty)]e^{-t/R_1C} + V_0(\infty) \qquad (6)$$

Where $V_0(0+) = -\frac{R_2}{R_1}(1)$ and $V_0(\infty) = 0V$. To determine the analytical expression for the amplitude response of the circuit, assuming an ideal op-amp for checking both high and low frequency inputs; equation (2) was the result. This was the result from equation (7) below.

$$G = -\frac{z_2}{z_1} \qquad (7)$$

Where z_1 is the impedance of C and R_1 in Fig. 1 and z_2 is the impedance of R_2. Equation (2) is also the form of the gain at high frequency. At low frequency the gain is 0 as shown above. Considering the equation is derived from the circuit, the predicted responses form the analytical expressions above make sense.

Like $\omega = \frac{1}{\tau}$, since the cutoff frequency is also an ω represented as ω_c; it also equals $\frac{1}{\tau}$. Thus, τ is the inverse of ω_c.

Now, when Fig.1 has an $R_1 = 10k\Omega$, G=6dB, and a $-3dB$ (cutoff) frequency of 300Hz; realistic resistor and capacitor values need to be chosen. G=6dB stems from 20log(-2), meaning k=2. So

$R_2 = 20k\Omega$. The $-3dB$ (cutoff) frequency (f_0) of 300Hz means that ω_0= 600rad/s which leads to C=53nF and $\tau = 530$ us.

To find the step response graphically when V_0 vs. time is graphed is shown in equation (8).

$$V_0\,(\text{peak}) * (1 - 63\%) = V_\tau => \ \tau = \text{x coordinate of } V_\tau \quad (8)$$

1.3 Procedure

Lab Procedure:

1. LTSPICE was used to construct the circuit shown in Fig. 1 using OP-27, DC voltages VCC=12V and VEE = -12V, R1, R2 and C that were obtained in the prelab part (e), gain of 6 dB, and a –3 dB (cutoff) frequency of approximately 300 Hz and input resistance $R_1 = 10k\Omega$
2. The step response was found by applying a rectangular pulse, where the ON time is ≈5ms, a pulse signal that jumps from 0 to 1V in 1ns for 5ms then falls from1V to 0 in 1ns and then stays at 0 for another 5ms. The transient simulation was set at a stop time of 20ms. This to then plot the input voltage and the output voltage to find τ and compare to prelab.
3. The frequency response was found by applying a Vin = 1V AC small signal analysis and using AC analysis with sweep size as Decade, with 1000 points per decade. The frequency was set to be from 10Hz to 10 Meg and then Vout/Vin of the circuit was plotted to find the 3dB cutoff frequency.
4. The sinusoidal response was found by using the same circuit from part 3 but adjusting the frequency and max step and stop time 10 times and comparing them to their determined gains. To determine each gain the peak Vout value was found on each LTSPICE graph for each frequency then G=20log(Vout/Vin) was used to find gain. Finally, all 10 frequency and corresponding gain values were plotted on the log scale in Excel and compared to the graph in part 3.

1.4 Results & Analysis

When applying all the parameters of step 1 and step 2 of the procedure above, Fig. 2 is the resulting circuit. While Fig. 3 is the resulting graph exhibiting the correct V_0 value used to find the step response for step 2 of the procedure. V_0 was found to be 1.98V, then in using equation (8), the resulting $\tau = 527.8$us. This was just a .41% error from the prelab calculation which is due to human measuring error.

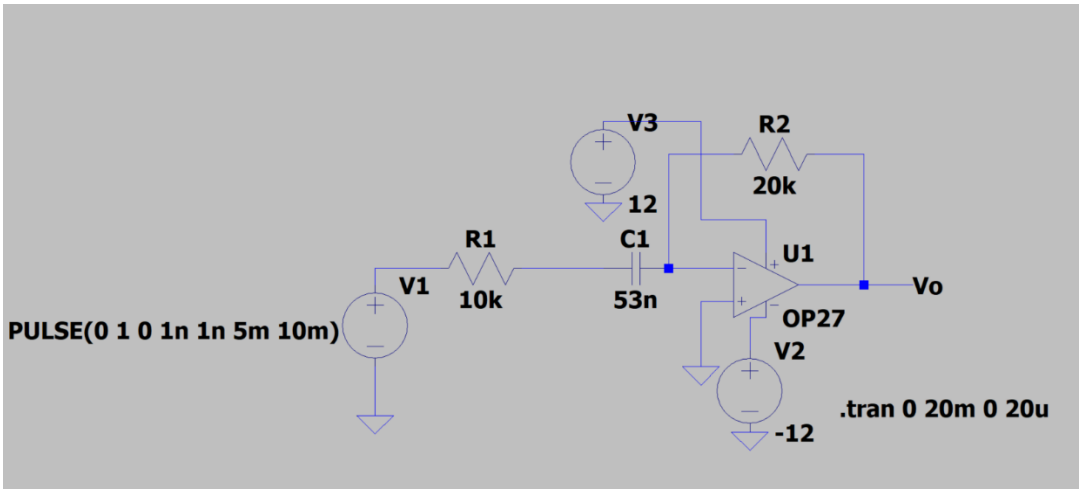

Figure 2: Pulse Circuit for Step 1 and 2 of Procedure

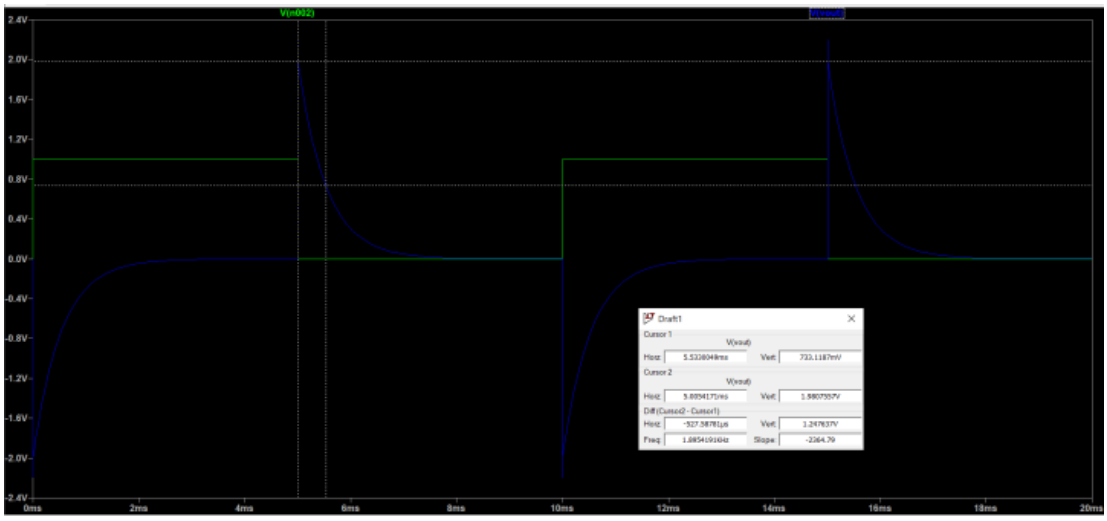

Figure 3: Vo Graph for Step Response

Using the parameters in step 3 to find the frequency response, Fig. 4 was the resulting circuit. When graphing [Vout/Vin] of Fig. 4, the product was the graph shown in Fig. 5. When measuring to point when it is most flat at the max of the curve, the -3dB cutoff frequency gain was shown to be 2.996 dB. Since the high frequency gain is 6 dB, the difference is estimated to be 3 dB for the 3 dB cutoff frequency. The cause of the high frequency response is that it is related to the bandwidth gain product of the op-amp. This puts a limit on the gain at high frequencies which causes gain to drop off when frequency hits 2MHz.

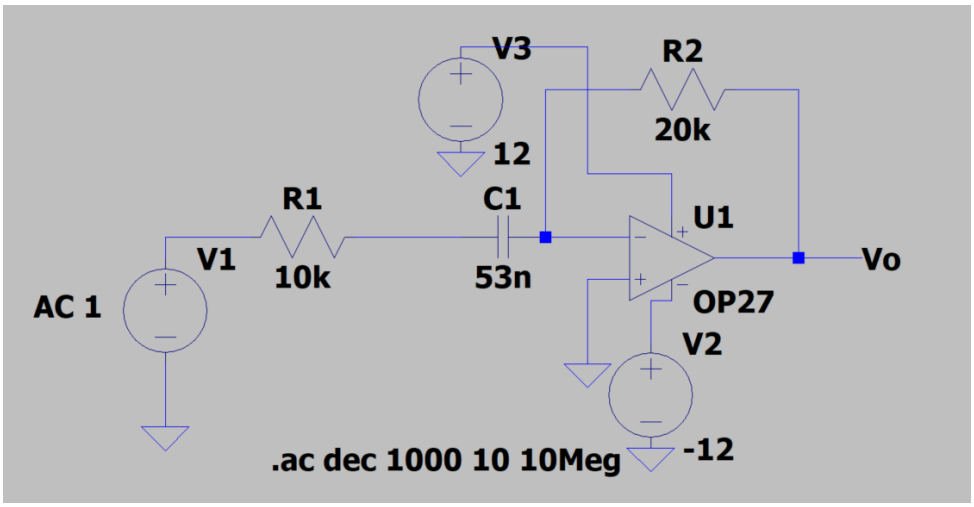

Figure 4: AC Circuit for Step 3 to Find Frequency Response.

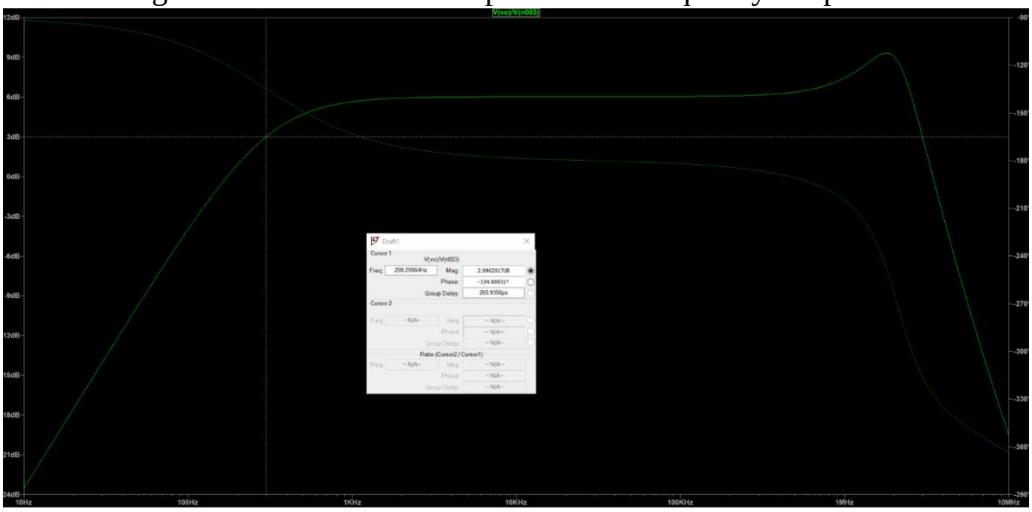

Figure 5: Graph of AC Circuit showing [Vout/Vin].

When completing step 4 of the procedure, the AC circuit shown in Fig. 4 was used with changing the frequency (f_0), the stop time and the max timestep. Each time these values were changed, the circuit was plotted in LTSPICE to find the resulting Vi and Vo peak values. Table 1 shows the results of how the variables stated were changed and the resulting Vi and Vo values. The last column was calculated in Excel using 20log[Vout/Vin]. Once the logscale gain was calculated for all 10 frequency values, using Excel, Logscale Gain vs. f_0 was graphed shown in Fig. 6.

Table 1- Input frequency, transient analysis stop time and timestep, plotted peaks for Vi and Vo, Logscale

frequency (f_0)	frequency (Hz)	stop time	max timestep	Vi peak (V)	Vo peak (V)	Logscale Gain (dB)
0.01 f_0	3	.1 s	.1 ms	2	0.039957	-33.9887
0.1 f_0	30	.05 s	.05 ms	2	0.39761	-14.0315
0.2 f_0	60	.02 s	.02 ms	2	0.78368	-8.13782
.5f_0	150	.01 s	.01 ms	2	1.787	-0.97811
f_0	300	5 ms	5 us	2	2.826	3.002843
2 f_0	600	2 ms	2 us	2	3.585	5.069183
5 f_0	1500	1 ms	1 us	2	4.01	6.042288
10 f_0	3000	.5 ms	.5 us	2	4.113	6.262574
20 f_0	6000	.2 ms	.2 us	2	4.11	6.256237
100 f_0	30000	.1 ms	.1 us	2	4.035	6.096271

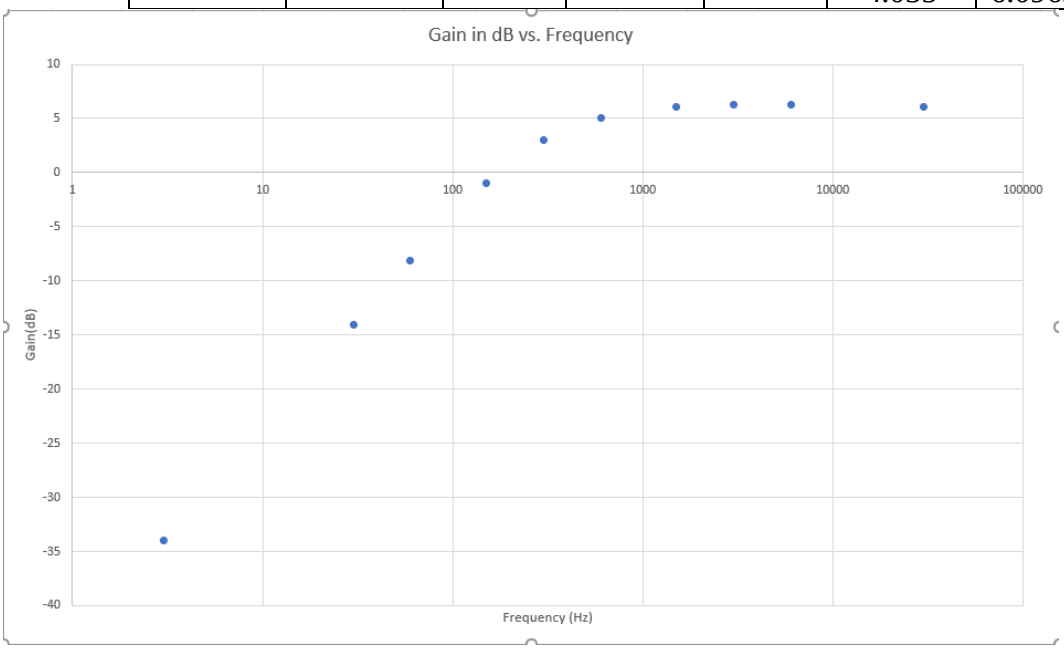

Figure 6: Gain (dB) vs. Frequency (Hz) using Excel.

When comparing the plot in Fig. 6 to the plot in Fig. 5, they exhibit the same values when using both Excel and LTSPICE. Also, from looking at both figures, the high frequency response and the cutoff frequency both conform to the design specifications. With that said though, the key difference is that the Excel graph displays no drop off, while LTSPICE exhibits a drop off due to the bandwidth gain.

1.5 Conclusion

To conclude this experiment, to resulting step response exhibited a .41% error between the experimental value and theoretical value. When comparing the graphed values of the 10 frequency values based on f_0=300 Hz to the LTSPICE [Vout/Vin] graph was shown to produce the same values. These graphs also showed that both the cutoff frequency and high frequency gain conform to the design specifications.

Experiment #2 High Gain Amplifier

2.1 Purpose

The purpose of experiment 2 was to design and implement a high-gain amplifier with a high input resistance and then with a low output resistance.

2.2 Theoretical Background

The background of this experiment is like that of experiment 1 because the topic is still operational amplifiers. The difference is that the specific category of op-amps that is being tested is high gain operational amplifiers. This means, noise will be a dominant factor in measuring the output voltage of the op-amp circuit. Noise is defined as a random voltage generated at the output even when there is no applied input voltage. This can be due to various factors including but not limited to thermal noise or flicker noise of the devices.

While there was no prelab for this experiment, there was a list of design specifications and a circuit design procedure. The parameters for the design specifications were to have an input sine wave signal of 10kHz with an amplitude of between 6 to 20 mv peak-to-peak. The overall gain was required to be 1000±2%, with the output signal being at 10 kHz and 1000 times amplitude than the input amplitude, with minimum phase shift with respect to input. The input resistance was required to be 1MΩ and the output resistance less than or equal to 10 Ω. The op-amp specs were to be the same as the op-amps used in experiment 1. The required circuit that meets these design specification is shown in Fig. 7. Fig. 8 shows the added input resistance (R_{in}) that would be applied between V1 and the first op-amp of Fig.7 that meets the specification for the input resistance. To determine if Fig. 7 meets the specification for the output resistance (R_0) is by using equation (9) where V_o is the output voltage with the 470 Ω resistor (R_L), and V_{oc} is the output voltage without R_L.

$$V_o = \frac{R_L}{R_L + R_0} V_{oc} \qquad (9)$$

To verify the gain experimentally, equation (10) is applied.

$$G = \frac{V_o}{V_{in}} \qquad (10)$$

The theoretical gain (G) using the resistors in Fig. 7 was calculated to be 978 V/V which is just outside of the 1000±2% requirement. Then to verify R_{in}, equation (11) was used.

$$R_{in} = \frac{V}{I} (* \; across \; the \; resistor) \qquad (11)$$

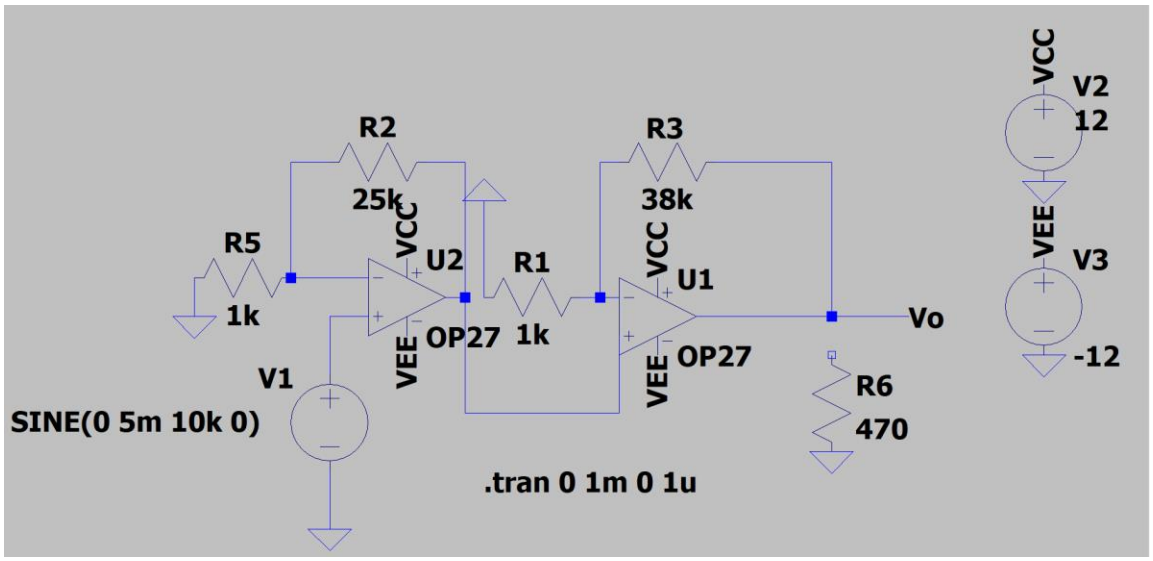

Figure 7: Sinewave Op-amp Circuit to meet Design Specification.

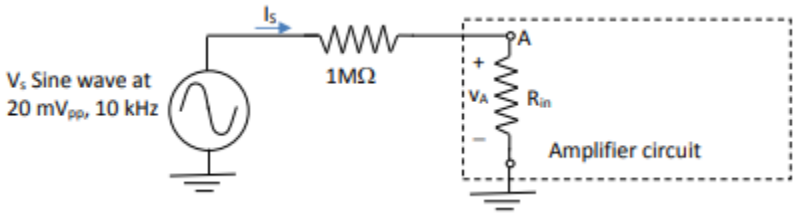

Figure 8: Fig. 7 Circuit with additional Rin=1MΩ.

2.3 Procedure

Circuit Design Procedure:

1. Created a circuit between two and five op-amp stages.

2. Calculated theoretical values for the expected gain, and the expected input and output resistances, given the design specifications.

3. Calculated the expected gain, and expected input and output resistances for each stage.

4. Use two to five OP-27 op-amps to maintain the design requirements for a gain of at least 1000 and the frequency of 10 kHz.

Lab Procedure:

1. Using LTSPICE, the circuit to meet the design specifications and circuit procedure was built. Then a transient analysis with proper settings was applied and the overall gain was verified by plotting Vout and using equation (10).

2. The input resistance of 1MΩ was applied to the circuit as shown in Fig. 8 and the voltage across the 1MΩ (VS- VA), the current (I) through 1MΩ and VA were plotted to estimate R_{in} using equation (11).

3. The output resistance was calculated by removing R_{in}, applying a sinewave input with a 10 mV peak to peak and 10 kHz then plotting the open circuit to find V_{oc}. Then to find V_o, R_L was applied and the circuit was again plotted. Then using equation (9), R_0 was determined.

2.4 Results & Analysis

Most of this experiment was to design a high gain amplifier circuit that met both the design specifications and the circuit design procedure described in the theoretical background and the first part of the procedure. In conducting the experiment, due to the random voltages generated by the noise in the op-amp, the resistors picked for the circuit in Fig. 7 could not satisfy the gain requirement both theoretically and experimentally. The resistor values pick did however get close to the gain requirement in the theoretical calculation and actually satisfy the requirement experimentally. As shown in Fig. 7 above, Rin (R5)= 1 kΩ, Rout(R2)= 25 kΩ, Rin(R1)=1 kΩ, and Rout (R3)=38 kΩ. Fig. 9 is the graph showing the Vin and the Vout of the circuit in Fig. 7. The peak values of both voltages were then applied to equation (10) to result in a G of 1010.8 V/V for the experimental gain. This ended up being a 3.35% error from the theoretical value due to the noise of the op-amp.

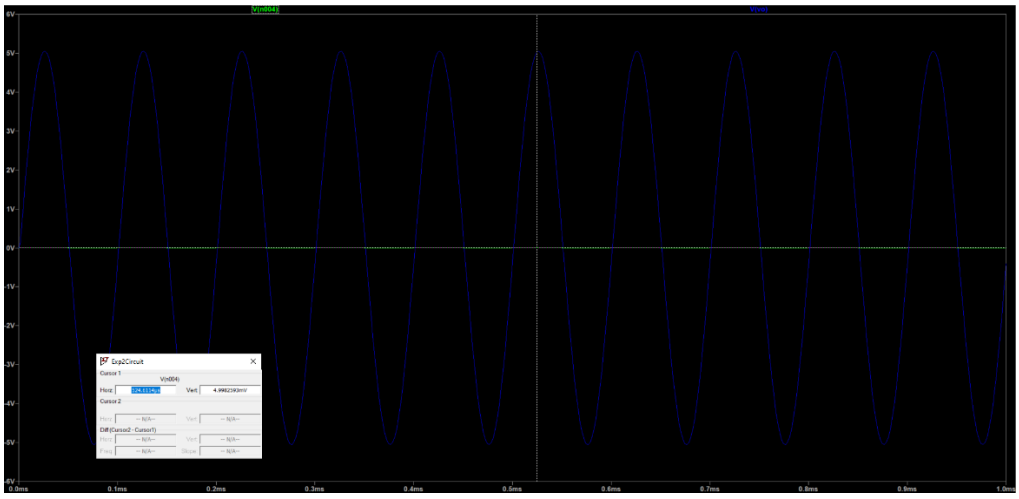

Figure 9: Vin and Vout of Fig. 7 Circuit.

To then find the variables around R_{in}, Fig. 10 shows the circuit created that combines Fig. 7 and Fig. 8 together. This circuit was used to then graph the variables stated in step 2 of the lab procedure. After finding these variables from the graph shown in Fig. 11, equation (11) was used to calculate R_{in}=5.6 MΩ.

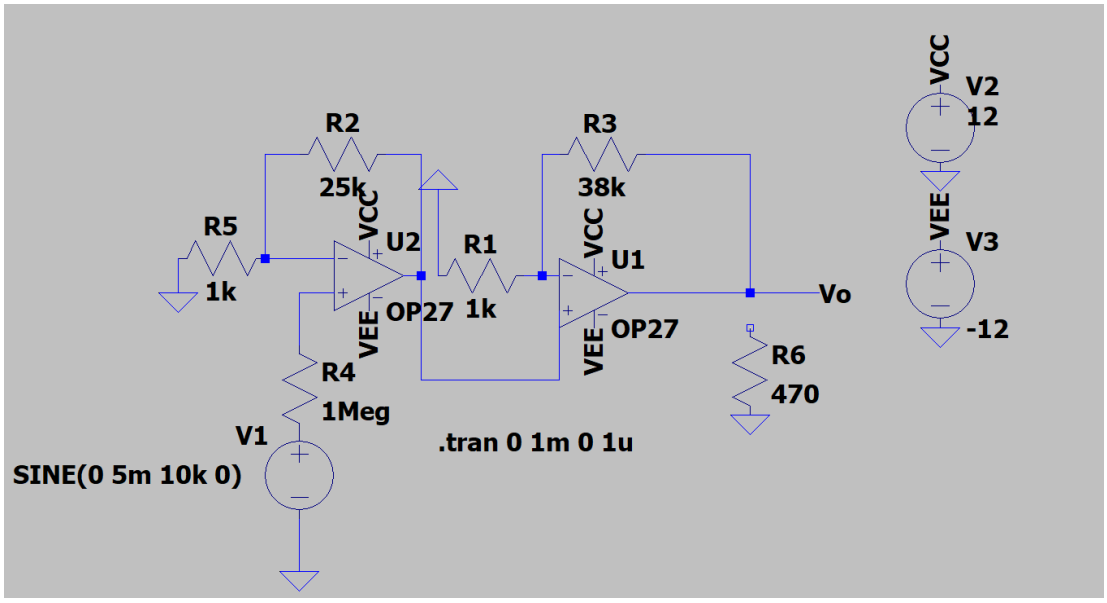

Figure 10: Fig.7 Circuit with R_{in} applied to the Circuit.

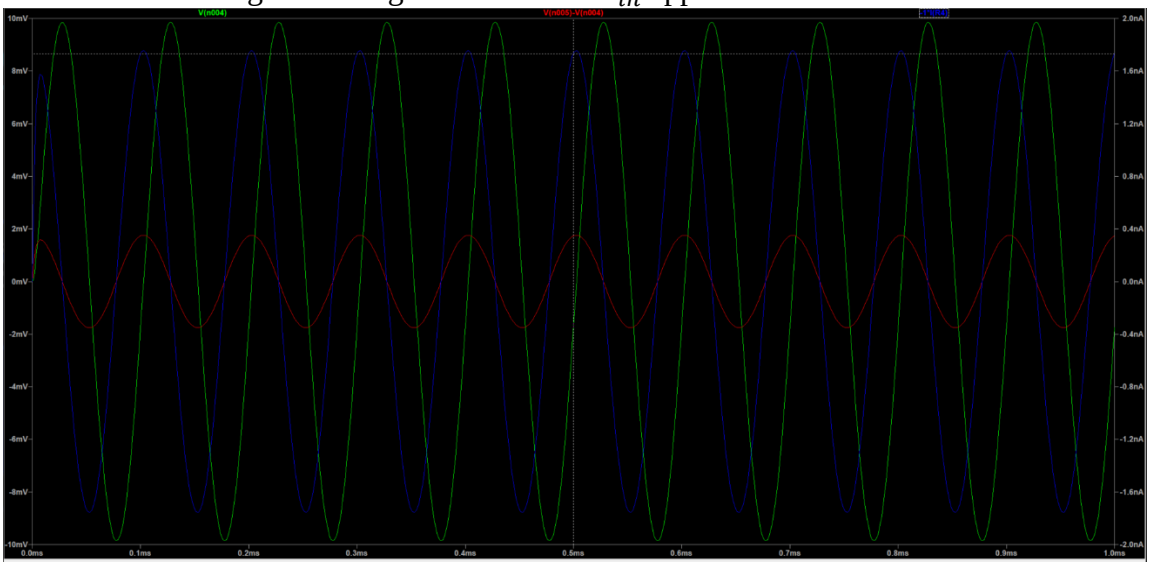

Figure 11: Graph showing I of R_{in}, Vs-Va across R_{in}, and Va above R_{in} in Fig.10.

Once removing R_{in} and adding R_L, the circuit provided in Fig. 12 was generated to be plotted as shown in Fig. 13 to calculate R_o using equation (9). R_o was then found to be .27 Ω. This made sense since VL > (470/480) × Voc => 5.056V >(470/480)*5.059=4.953 V determined that $R_o$would be less than 10 Ω as stated in the handout.

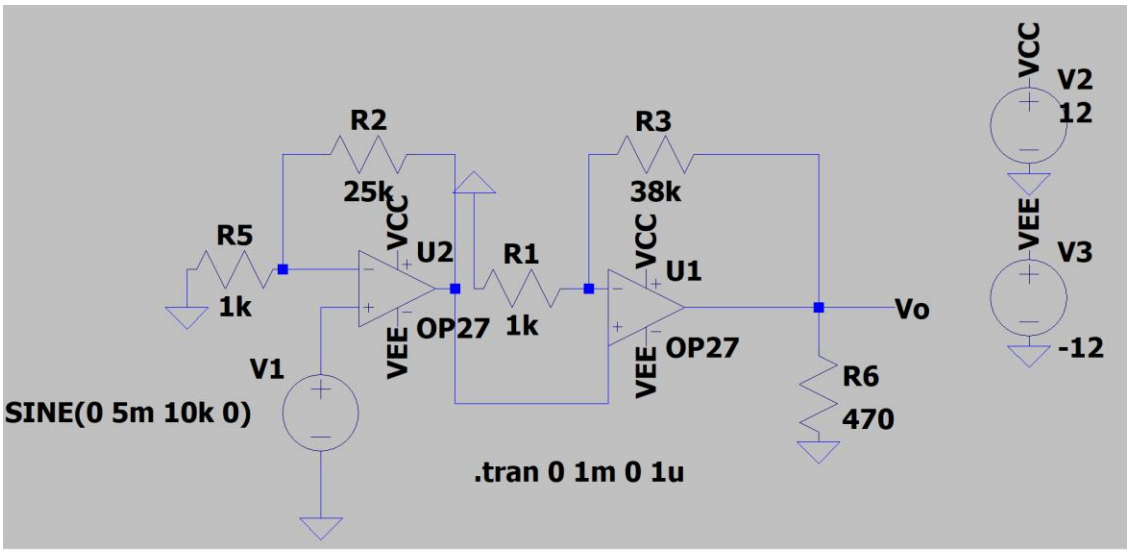

Figure 12: Fig. 7 Circuit with R_L applied.

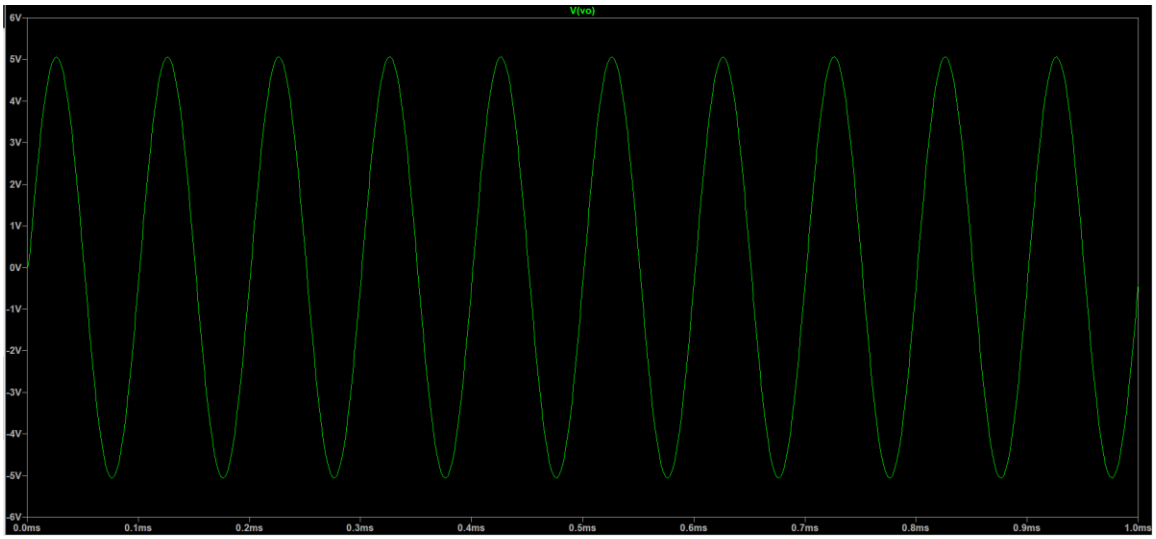

Figure 13: Graph of V_o from Fig. 12.

2.5 Conclusion

To conclude this experiment, noise was proved to create a significant disturbance in the output voltage which effected the overall gain of the circuit. This meaning, the Rin changed from 1M Ω to 5.6 M Ω and the Rout went from 10 Ω to .27 Ω . The .27 Ω was validated because the two output voltages verified that the Rout was to be less than 10 Ω .

Appendix

Appendix A

Lab 3 Checklist

Name:_____

Lab title and introduction

- Lab title, your name, date, and lab partner.

I. First Order High Pass Active Filter (50 pts total)

1. Differential equation relating v_{out} and v_{in} for circuit of Figure 1.
2. Selected values for R_1, R_2, and C to meet design specifications.
3. **DEMO**: Have a teaching assistant mark your Demo on Blackboard, indicating that they have observed your circuit's simulation.
   - Circuit sinusoidal operation is observed for at least one value of input frequency
   - Show TA analysis from pre-lab providing design approach.
   - Discuss with TA whether circuit's frequency response is consistent with expectations from pre-lab analysis.
   - Discuss with TA whether circuit's step response is consistent with expectations from pre-lab analysis simulations.
   - Plot your experimental frequency response data using Microsoft Excel.
   - Also provide either a sketch or a picture of your step response.
4. Compare your experimental data discuss any discrepancies. Does your circuit's response meet the design specifications?

II. High Gain Amplifier (50 pts total)

(a) Circuit Design

1. Sketch of amplifier circuit. Include desired values for circuit components (e.g. resistor values).
2. Expected gain, input and output resistances for your overall amplifier circuit, and for each stage within your amplifier circuit.

(b) Circuit Implementation and testing

1. Measured values of the circuit's gain, input resistance, and output resistance. Does the circuit meet specifications?
2. **DEMO**: Have a TA initial Blackboard indicating that he/she has observed (i) your circuits' operation on LTSPICE; (ii) your measurements verifying that the circuit meets the design specifications, and (iii) your calculations of gain and input and output resistance for the overall circuit and for each stage within the circuit.
4. Comparison of measured and expected gain, input and output resistances for your circuit and discussion of any discrepancies between measurements and expectations.

