Washington State University

School of Electrical Engineering and Computer Science

EE 352 Electrical Engineering Laboratory

Lab # 5

Diode Characterization and Applications

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Lab Overview

In this lab, various types of diodes were studied for their characteristics in both forward and reversed biased modes. These diodes included general purpose switching, rectifier, and Zener diodes. These diodes are commonly used for circuit applications such as voltage regulator, voltage clipper, peak detector, and voltage doubler. To demonstrate these applications, the diode current and voltage were graphed in LTSPICE to obtain the characteristics for forward and reverse biased. The saturation current and n were estimated from the datasheet provided. Then using a Zener diode, a voltage regulator was designed to regulate the dc voltage across the load. Also using a Zener diode, a voltage limiting circuit was designed to clip the output voltage, then a voltage doubler was designed to study the ripple and output voltage.

Experiment #1 Diode Forward and Reversed Bias Characteristics

1.1 Purpose

The purpose of this experiment was to obtain the characteristic curves for forward biased diodes (1N914) and calculate the critical diode parameters such as the saturation current and n.

1.2 Theoretical Background

To address the background of this experiment, it is important to first address the significance of a PN junction diode. A PN junction diode is formed when a p-type semiconductor is fused to an n-type semiconductor creating a potential barrier voltage across the diode junction. When fusion happens, this results in a depletion layer where there occurs free electrons which produces a asymmetrical conducting two terminal device which is the PN junction diode. The characteristics of this is that there is a current that flows through in one direction, and it does not behave linearly with respect to the applied voltage.

When a diode is connected to a forward bias condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. When the external voltage is greater than the value of the potential barrier, the potential barriers oppositions will be overcome and current will begin to flow. This is due to the negative voltage repelling electrons toward the junction causing them to cross over and combine with the holes being pushed by the positive voltage. This results in a characteristics curve of zero current flowing up to the voltage point called the “knee” on the static curves and then a high current flow through the diode with little increase in the external voltage.

When a diode is connected in the reverse bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage attracts electrons toward the N-type material and away from the junction. While the holes are attracted toward the P-type material, also away from the junction. The net result causes the depletion layer to grow wider due to lack of electrons and holes and presents a high impedance path preventing current from flowing.

When conducting this experiment and the prelab, Fig. 1 below and equations (1) and (2) were used to calculate n and I_s.

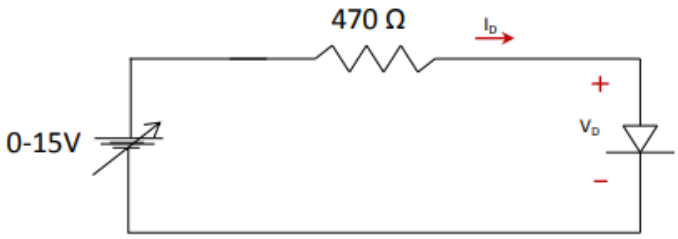

Figure 1: Diode voltage and current measurement

$$I_D = I_s(e^{\frac{V_D}{nV_T}} - 1) \qquad (1)$$

$$\ln(I_D) = \ln(I_s) + \frac{V_D}{nV_T} \quad (2)$$

For equations (1) and (2), I_D is the diode current, I_s is the saturation current, V_D is the diode voltage and V_T is the thermal voltage which is typically valued at 26mV in room temperature. The 1 in equation (1) is usually very small in comparison so it can typically be ignored. By rearranging equation (2) to solve for n, the product is in equation (3), where the change in V_D and the change in I_D is found by analyzing two points on the graph and V_T is a constant.

$$n = \frac{\Delta V_D}{V_T \ln\left(\frac{I_{D2}}{I_{D1}}\right)} \quad (3)$$

To calculate I_s, equation (1) was rearranged and used. Then for the second part of the prelab, equation (4) was used to calculate r_D where the change in voltage and the change in current are the same values indicated in equation (3). Here r_D is the dynamic diode resistance as a function of diode voltage.

$$r_D = \frac{\Delta V_D}{\Delta I_D} \quad (4)$$

Here the theoretical r_D value is 4.78 Ω.

1.3 Procedure

1. Fig. 1 was built using LTSPICE with the diode 1N914 available in the Diodes library.
2. A DC Analysis was applied with a varied linear voltage from 0 to 15 V with a 1 mV step size.
3. Then I_DVs. V_D was plotted. Using two points to measure I_s and n and the r_D was found using I_D=10 mA with a 1 mA separation and equation (4). This was then compared to the prelab value.
4. Then the reversed biased characteristics were studied with a DC Analysis with varied linear input voltage from -10V to zero with a step size of 1 mV. Then I_DVs. V_D was plotted to then comment on the amplitude of the diode current.
5. Lastly, Matlab was used to estimate the values for n and I_s, and plot I_DVs. V_D. To which then the similarities and the dissimilarities between the two graphs were commented on.

1.4 Results & Analysis

Fig. 2 below represents the LTSPICE model of Fig. 1 with the specified parameter in step 2 of the procedure.

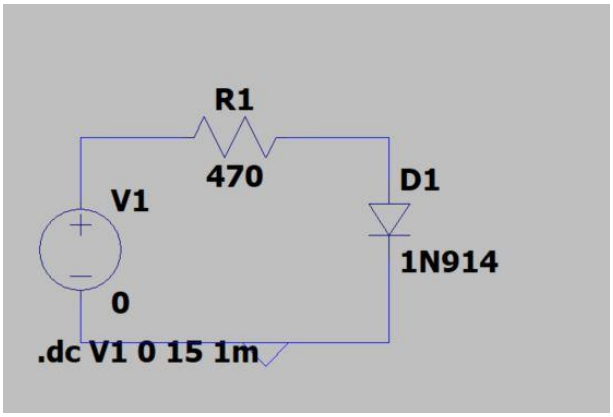

Figure 2: LTSPICE circuit of Fig. 1 with a 0 to 15 linear input voltage

Fig. 4 below shows I_DVs. V_D of Fig. 2 with the selected points to find r_D. These points were (640.7665 mV, 3.343 mA) and (690.94 mV, 9.379 mA). These points corresponded as (V_{D1}, I_{D1}) and (V_{D2}, I_{D2}). Using these points, a $V_T = .026V$, and equation (3); n was found to be 1.87. Using these points, n,V_T, and equation (1) rearranged to solve for I_s; I_s was found to be 6.3 nA. Finally using the points and equation (4), r_D was found to be 5.4 Ω. This is only a 12.98% error from the theoretical value of r_D due to measuring errors and the internal software variance.

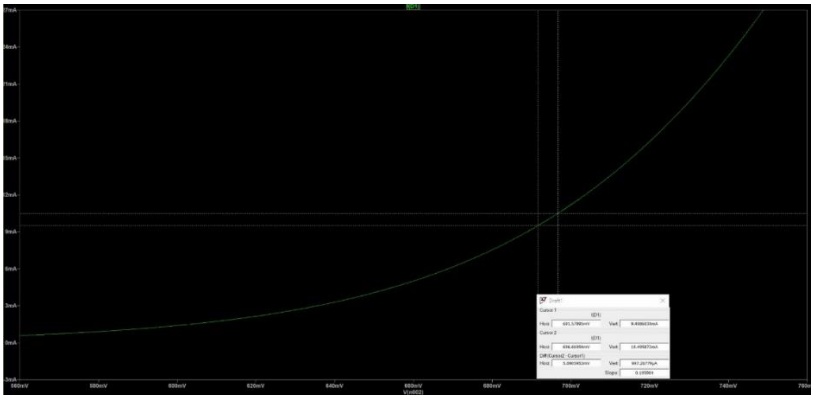

Figure 3: Plot of Fig. 2 showing I_DVs. V_D to find r_D.

Fig. 4 below shows the circuit of Fig.1, this time representing it as a reverse bias with the specified parameters from step 4 of the procedure.

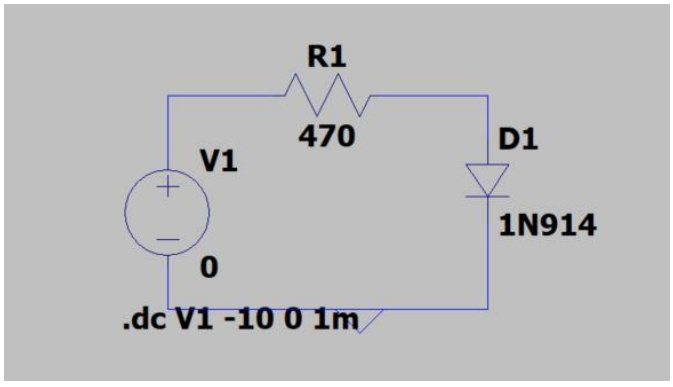

Figure 4: Circuit of Fig. 1 with a -10 to 0 linear input voltage

Fig. 5 below is the plot of Fig. 4 showing I_DVs. V_D. The amplitude of this graph is 0 until its close to 0 V because the circuit specifies the point of voltage to be a 0V, where then current is no longer limited. The reason it spikes at 0 V is because while the current is building between -10 and 0 V, it is being prevented from crossing the depletion layer due to the diode until it hits the specified point voltage of 0 V where that limiting is no longer so that build up current can cross.

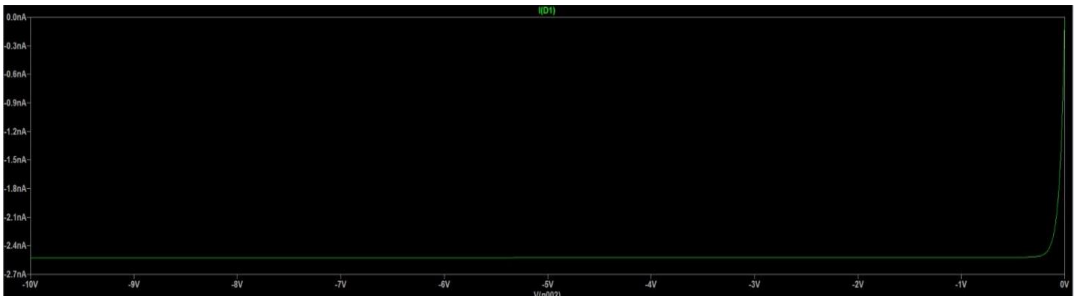

Figure 5: Plot of Fig.4 showing I_DVs. V_D.

Fig. 6 shows the Matlab plot from the code found in Appendix B. This is a graph of I_DVs. V_D with the estimated values of I_s and n. The pattern of the Matlab plot versus the LTSPICE plot is the same while the Matlab plot is a little off simply due to how each software's internal parameters are different.

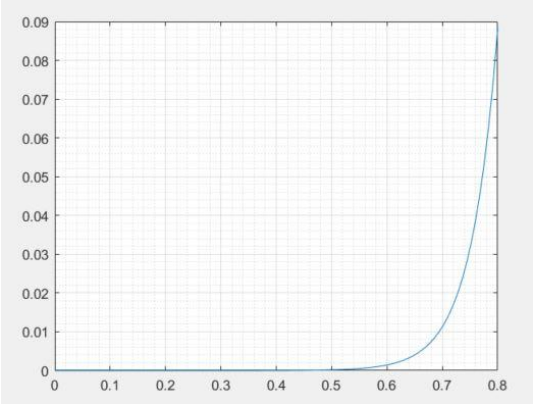

Figure 6: Matlab graph with linear varying voltage between 0 and .8 V.

1.5 Conclusion

To conclude this experiment, the r_D between the theoretical and experimental was found to be a 12.98% error due to internal software parameters and measurement errors. Matlab reflected basically the same graph as LTSPICE only a little skewed because of differences in internal software parameters.

Experiment #2 Zener Diode Characteristics

2.1 Purpose

The purpose of this experiment was to study the voltage-current characteristics of a Zener diode for both the forward region and the reverse bias.

2.2 Theoretical Background

Here, the same concepts with the forward and reverse bias are also applied like in experiment 1. The key addition for this experiment is the application of the Zener diode. In the forward region, the Zener diode acts like a regular diode as described in the theoretical background of experiment 1. In the reverse bias, the Zener diode has a very small reversed current until it reaches the breakdown voltage ("knee"), then the Zener voltage varies linearly with the current.

From the Datasheet of 1N750, the I_Z, V_Z, and r_z are 20mA, 4.7V, and 19 Ω respectively. Then using equation (5) below, the estimated $V_{Z0} \approx V_{Zk}$ is 4.32V using the datasheet values.

$$V_{Z0} = V_Z - I_Z r_z \qquad (5)$$

Fig. 7 below shows the circuit to which the experiment was conducted.

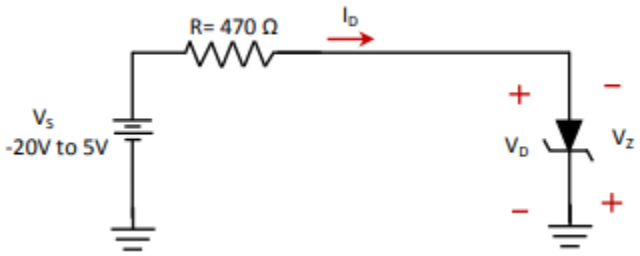

Figure 7: Experimental set up to measure Zener diode characteristics

2.3 Procedure

1. Fig. 7 was constructed using LTSPICE with the Zener diode 1N750.
2. A DC Analysis was then applied with a linear varied input voltage from -20 V to +5 V with a step size of 1 mV.
3. Then I_DVs. V_D was plotted of the Zener diode to estimate the minimum current ($I_{Z,min}$) in the breakdown region shown in Fig. 10. Then using two cursors the incremental resistance was estimated with one point at 20 mA.
4. Lastly, using equation (5) and the points found in step 3, V_{Z0} was calculated.

2.4 Results & Analysis

Fig. 8 below shows the circuit in Fig.7 with the specified parameters given in step 2 of the procedure.

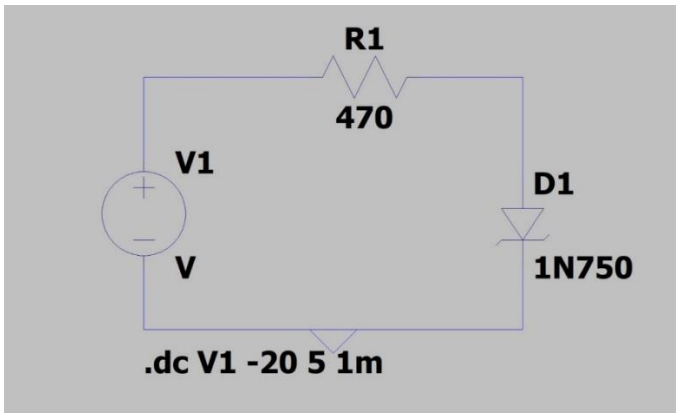

Figure 8: LTSPICE Model of Fig. 7 with varying input voltage of -20 to 5 V.

Fig. 9 is the plot of Fig. 8 showing I_DVs. V_D to find $I_{Z,min}$. To do this, first to points (-4.7 V, 20 mA) and (-4.712 V, 25 mA) were selected to be the corresponding (V_{D1}, I_{D1}) and (V_{D2}, I_{D2}). Using these points and equation (4), r_D was found to be 2.4 Ω. This is an 87.3% error from the theoretical value of r_Z due to measuring errors and the internal software variance and because the datasheet value is based on an average of 1000 diode circuits. Then using equation (5) to find V_{Z0} with $V_Z = -4.7\ V$, $I_Z = 20\ mA$, and $r_Z = 2.4\ \Omega$; V_{Z0} was found to be 4.652 V. This is a 7.69% error due to the r_Z value differing. Then from the plot in Fig. 9, the minimum current that enters the linear region is 6 mA.

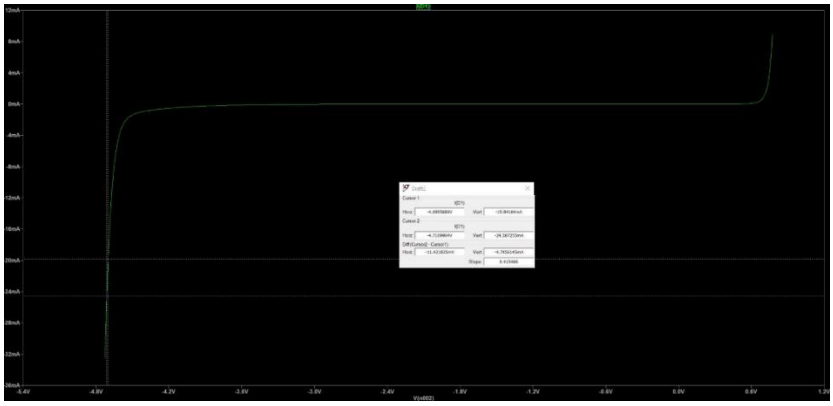

Figure 9: Plot of Fig. 8 showing I_DVs. V_D.

2.5 Conclusion

To conclude this experiment, the r_Z differed significantly with a 87.3% error due to measurement error, software parameters, and the theoretical value being based on the average of 1000 different diode circuits. This variation than led to V_{Z0} having a 7.69% error because of the differing r_Z value.

Experiment #3 Voltage Regulator

3.1 Purpose

The purpose of this experiment was to design a voltage regulator to regulate the dc voltage across the load. This was done using the Zener diode 1N750 and the obtained values of the second experiment.

3.2 Theoretical Background

To introduce this experiment, the Zener diode (1N750) was used to regulate the voltage as shown in Fig.11 below. Zener diodes are basically the same as a standard PN junction diode, but they are specifically designed the have a low and specified to reverse breakdown voltage which controls any reverse voltage applied to it. To further explain, based on Fig. 10 below, when a Zener diode is biased toward the forward direction, the anode is positive with respect to the cathode and behaves normally with respect to the current passing through. In the reverse direction, when the cathode becomes more positive than the anode, as soon as the reverse voltage reached a predetermined value, the Zener diode begins to conduct in the reverse direction, due to the reverse voltage exceeding the rated voltage. This occurs in the depletion layer and a current start to flow through the diode to limit the increase in voltage. The current flowing increases dramatically to the maximum circuit value and once achieved, the reverse saturation current remains fairly constant over a wide range of reverse voltages. The voltage value at which causes the current to flow through the diode can be accurately controlled in the doping stage of the diode's semiconductor construction.

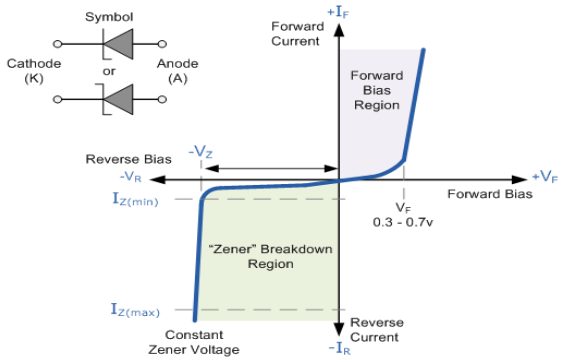

Figure 10: Zener Diode characteristics

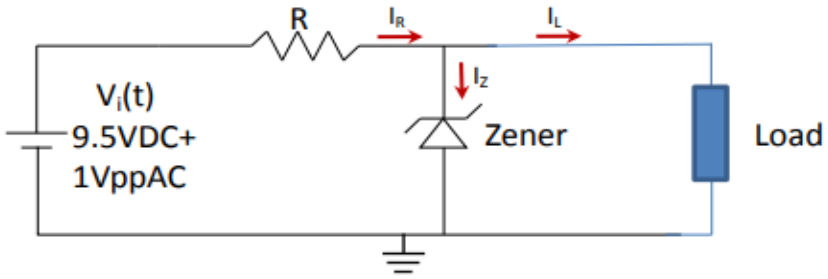

Figure 11: Voltage regulator using Zener diode.

As represented in Fig.10, the voltage regulator can supply a load with current ranging 0-10 mA. Then using the values found in experiment 2 to design the value of R so that the minimum Zener current is less than 10 mA with current load maximum is 10 mA and supply voltage is $9.5 + .5sin(\omega t)@\ 60\ Hz$ with load voltage regulated at around 4.7 V was found to be 215 Ω by using equation (5) to get $V_z = 4.7\ V$ and Ohms law at R.

3.3 Procedure

1. LTSPICE was used to construct the circuit shown in Fig. 11 with the R calculated in prelab.
2. Then the effect of the load current on the load voltage at the nominal input voltage was investigated by having the input voltage be 9.5 V DC and the load current set at 10 mA be downward. With a DC Analysis with a sweep from 0 to 10 mA and a step size of 0.1 mA to then plot the load current and Zener diode current vs the load voltage to record the no load and full load voltage values.
3. Then the ripple voltage was investigated based on the change in load current and the Zener diode current. This was done be deleting the DC value from the input voltage to then make it a sinewave of 9.5 V and DC offset of .5 at 60 Hz. Then current source was also removed, and a transient analysis was set at 100 ms with step size of 10 us. Once set, the V_L(t) was plotted to record the maximum value, the minimum value and ripple (peak-to-peak) value using cursors 1 &2. Then the V_L(t) and V_i(t) was plotted and scaled to be between 0 and 12 V to note how well regulated V_L(t) was on the plot. Then I_Z (-I_D) was plotted to record the maximum and the minimum values and ripple (peak-to-peak) values using cursors 1 &2.
4. Lastly a 1 kΩ load resistor was added across the Zener diode to repeat step 3.

3.4 Results & Analysis

Fig. 12 below shows the LTSPICE model of Fig. 11 with the parameters specified in step 2 of the procedure with the calculated R being 215 Ω.

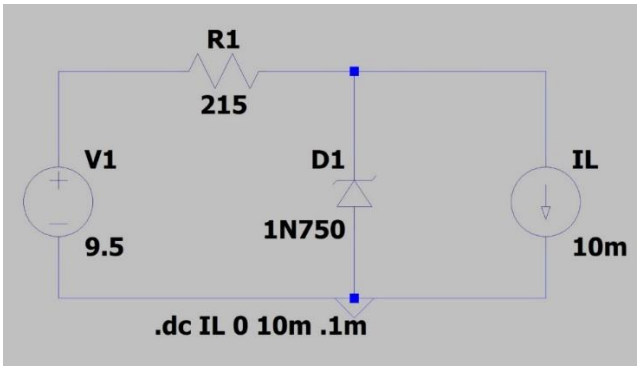

Figure 12: LTSPICE model of Fig. 11 with parameters specified in step 2 of the procedure.

Fig. 13 below shows the load current and the Zener diode current versus the load voltage. By using the cursor to find the load voltage and the Zener diode current values at no current load and at full current load was found to be $I_L(0A) => I_Z = 22.3\ mA$ and $V_L = 4.706\ V$ then $I_L(10\ mA) => I_Z = 12.44\ mA$ and $V_L = 4.675\ V$. The overall behavior of the graph shown in Fig. 13 is that the plotted points are the left most and right most points and the I_Z and I_L lines seem to mirror each other.

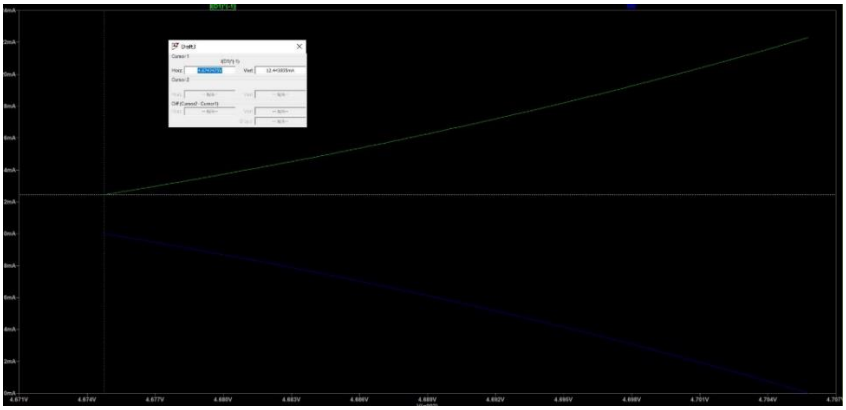

Figure 13: Plot of Fig. 12 showing load current and Zener diode current vs the load voltage.

Fig. 14 below shows the LTSPICE circuit of Fig. 11 with the added 1 kΩ load resistor, stated in step 4, and specified parameters explained in step 3 of the procedure.

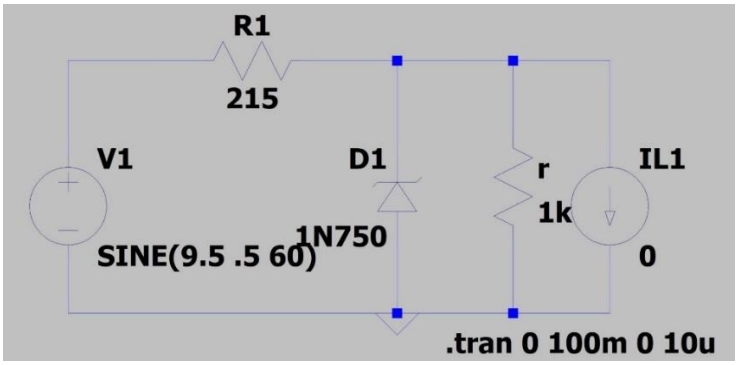

Figure 14: Circuit of Fig. 11 with parameters specified in step 3 and 4 of the procedure.

Figs. 15-17 are graphs of Fig.14 without the 1 kΩ load resistor as indicated in step 3 of the procedure. Fig. 15 is the resulting sinewave of V_L(t) showing the minimum of 4.701 V, the maximum of 4.711 V, and the ripple of 10.83 mV all found using the cursors. This being a .21% error for the minimum form the ideal 4.7 V and a .234% for the maximum. Fig. 16 shows V_L(t) compared to V_i(t) which shows that V_L(t) is significantly less rippled than V_i(t), meaning V_L(t) is much more regulated. Fig. 17 shows the plot of the Zener diode current I_Z(t) to which the minimum was 20.04 mA, the maximum was 24.57 mA, and the ripple was 4.53 mA all found using the cursors. This being a 100.4% error from the ideal 10 mA for the minimum and a 145.75 error for the maximum.

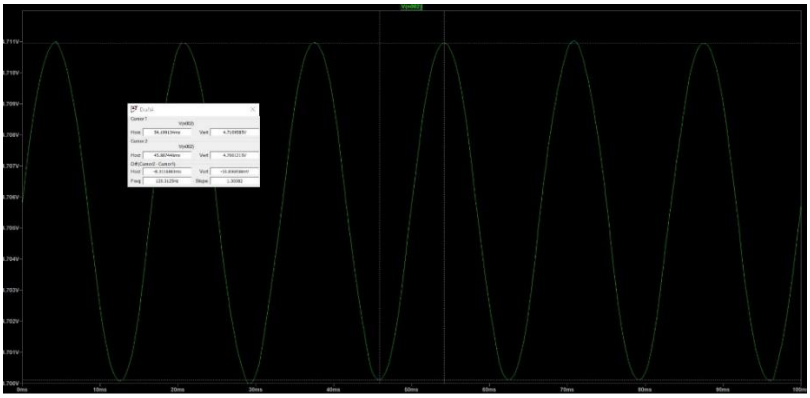

Figure 15: Plot of Fig. 14 without the 1 kΩ load resistor, showing the V_L(t).

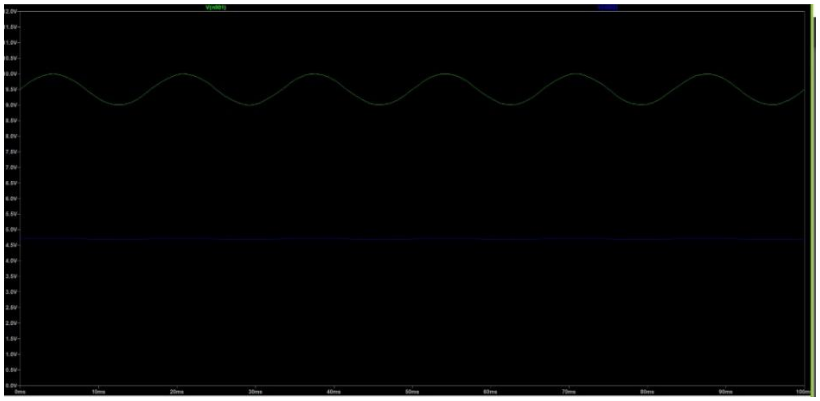

Figure 16: Plot of Fig. 14 without the 1 kΩ load resistor, showing the V_L(t) and V_i(t).

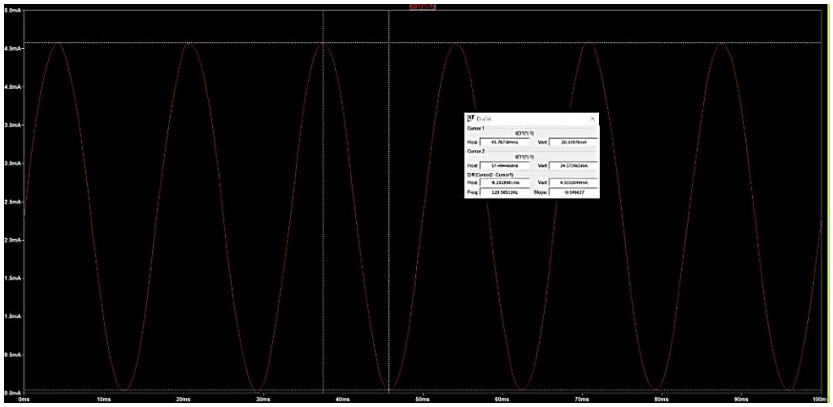

Figure 17: Plot of Fig. 14 without the 1 kΩ load resistor, showing the $I_Z(\mathrm{t})$.

Figs. 18-20 are graphs of Fig.14 with the 1 kΩ load resistor as indicated in step 4 of the procedure. Fig. 18 is the resulting sinewave of $V_L(\mathrm{t})$ showing the minimum of 4.686 V, the maximum of 4.699 V, and the ripple of 13.62 mV all found using the cursors. These being a .0029% error for the theoretical 4.7 V for the maximum, and a .298% error for the minimum due to the ripple. Fig. 19 shows $V_L(\mathrm{t})$ compared to $V_i(\mathrm{t})$ which shows that $V_L(\mathrm{t})$ is significantly less rippled than $V_i(\mathrm{t})$, meaning $V_L(\mathrm{t})$ is much more regulated. Fig. 20 shows the plot of the Zener diode current $I_Z(\mathrm{t})$ to which the maximum was -15.4067 mA, the minimum was -19.62 mA, and the ripple was 4.514 mA all found using the cursors. This being a 54% error from the theoretical 10 mA current value for the maximum and 96.2% error for the minimum.

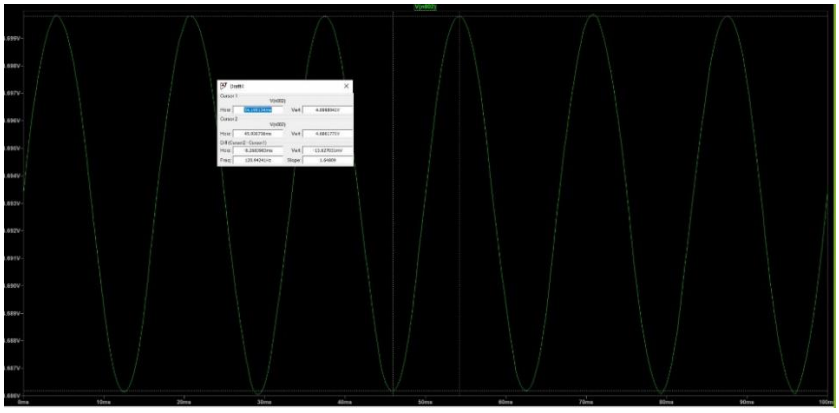

Figure 18: Plot of Fig. 14 showing the $V_L(\mathrm{t})$.

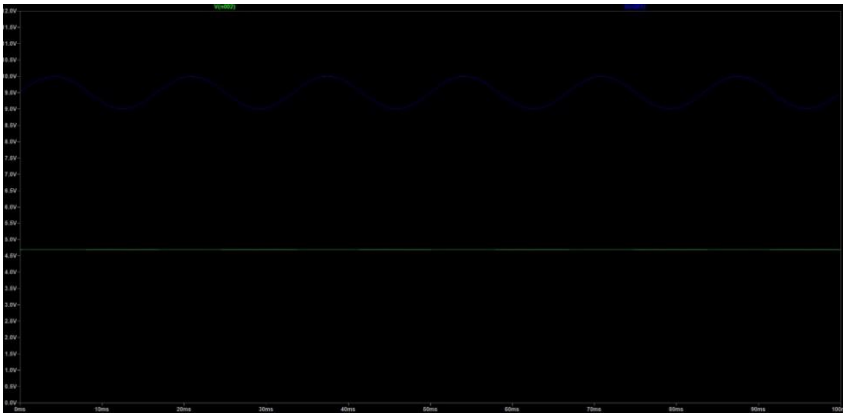

Figure 19: Plot of Fig. 14 showing the V_L(t) and V_i(t).

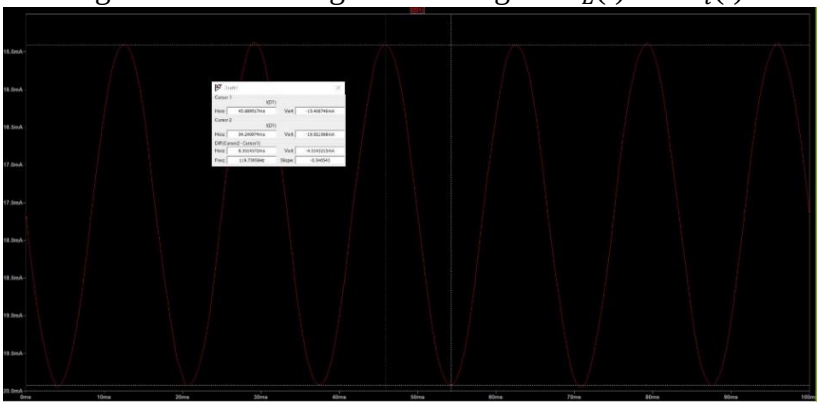

Figure 20. Plot of Fig. 14 showing the I_Z(t).

3.5 Conclusion

To conclude this experiment, the minimum, maximum and ripple values for the loading voltage at no loading current were 4.701 V, 4.711 V, and 10.83 mV respectively without the 1 kΩ load resistor and 4.686 V, 4.699 V, and 13.62 mV respectively with the 1 kΩ load resistor. Then for the minimum, maximum, and ripple of the Zener diode current, 20.04 mA, 24.57 mA, and 4.53 mA respectively without the 1 kΩ load resistor and -15.4067 mA, -19.62 mA,4.514 mA respectively with the 1 kΩ load resistor.

Experiment #4 Voltage Limiting/Clipping Circuit

4.1 Purpose

The purpose of this experiment was to study a voltage limiter for the purpose of limiting the output voltage.

4.2 Theoretical Background

A current limiting diode (CLD) regulates the amount of current over a voltage range similar to a Zener diode. Though for the CLD, it limits current over a wide voltage range and is diffused using a "Field effect" process with electrical characteristics optimized for high output impedance and current regulating capability. The CLD begins to conduct when a reverse biased voltage is applied from the cathode to the anode or PN junction. As the reverse biased voltage is increased to V_L, the current increases due to the bulk resistance of the N region. As the current approaches the knee section of the curve, a depletion region develops between the N region and the P-type gate. This depletion region decreases the current path in the N region slowing the increase of current flow. Eventually, the depletion region meets the P-type gate and pinch-off occurs, allowing current flow to become constant and almost independent of applied voltage until PN junction breakdown occurs somewhere above POV. When the polarity of the applied voltage is reversed and a forward bias is applied to the PN junction, the CLD exhibits characteristics similar to those of a forward biased diode.

For the prelab, the objective was to plot voltage between nodes A and B as function of time for the circuit shown in Fig.21 below. The parameters were the diode having a .7 V drop when forward biased and the applied voltage V_{in} is set with a frequency of 1 KHz. These plots are shown below in Fig. 22 with specified peak-to-peak voltages of 2 V, 7 V, and 10 V respectively.

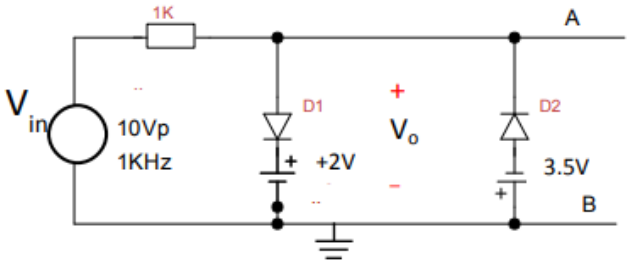

Figure 21: Voltage Limiting/Clipping Circuit

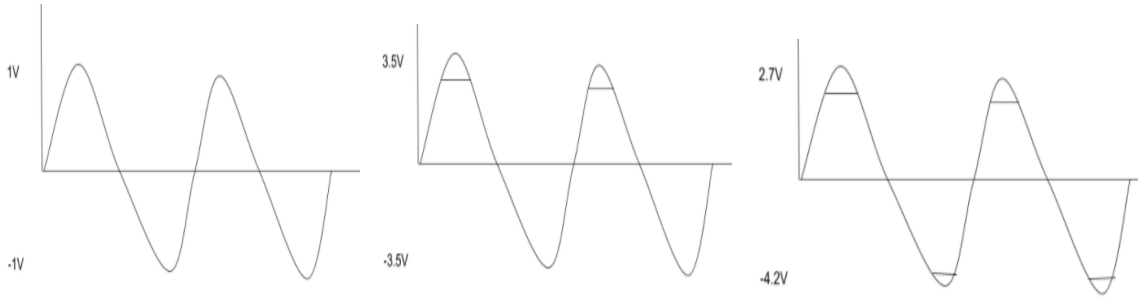

Figure 22: (a) $V_{PP} = 2V$ sketched plot, (b) $V_{PP} = 7V$ sketched plot, (c) $V_{PP} = 10V$ sketched plot

4.3 Procedure

1. Fig. 21 was built in LTSPICE with switching diodes 1N914 and R set at 1 kΩ.

2. The input voltage was set to be a sine wave at 1kHz with 2 V peak-to-peak with a transient analysis set at 10 ms and maximum step size of 1 μs to plot $V_0(t)$.

3. Step 2 was then repeated with input voltage, $V_{PP} = 7$ V and again with $V_{PP} = 10$ V.

4.4 Results & Analysis

Fig. 23 below shows the LTSPICE model of Fig. 21 with specified parameters in step 2 with $V_{PP} = 10$ V.

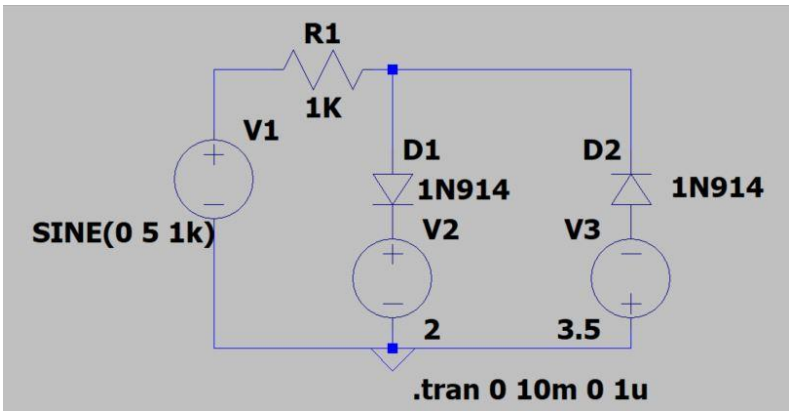

Figure 23: LTSPICE model of Fig. 21 with specified parameters in step 2 with $V_{PP} = 10$ V.

Figs. 24-26 show the resulting peak-to-peak output voltage sinewave behavior with 2 V peak-to-peak in Fig. 24, 7 V peak-to-peak in Fig. 25, and 10 V peak-to-peak in Fig. 26. The maximum and minimum values for each figure are as stated in table 1 below.

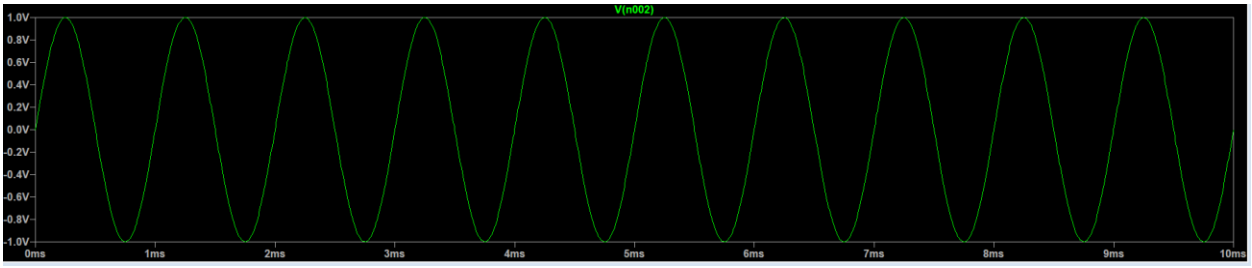

Figure 24: Plot showing 2 V peak-to-peak.

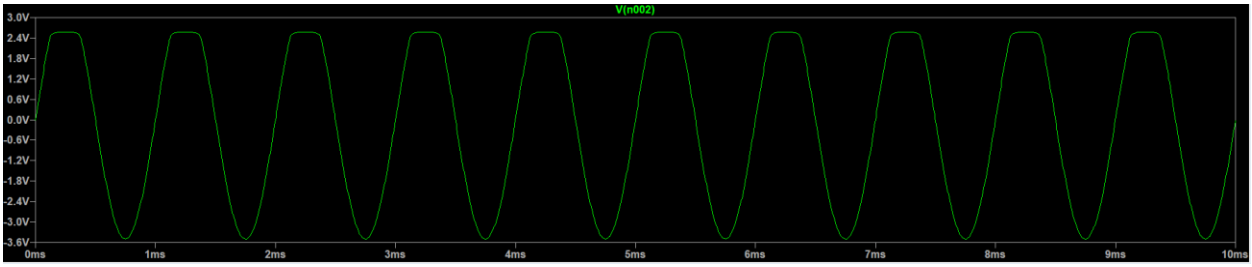

Figure 25: Plot showing 7 V peak-to-peak.

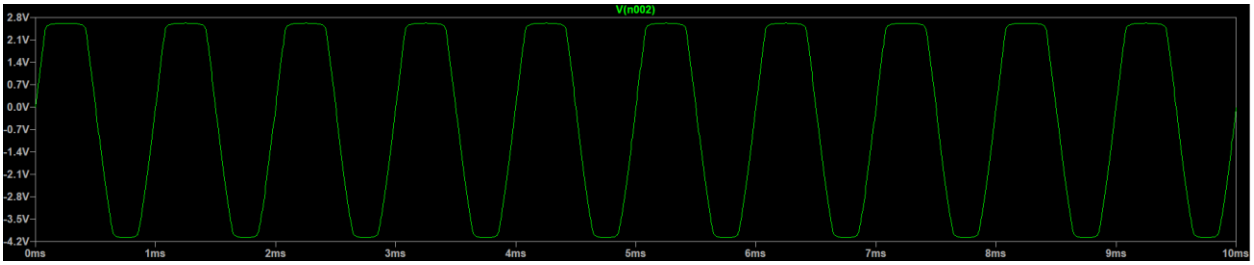

Figure 26: Plot showing 10 V peak-to-peak.

Table 1: Minimum and Maximum Values of the indicated V_{PP} values.

V_{PP}	2 V	7 V	10 V
Max(V)	1	2.581	2.62
Min(V)	-1	-3.5	-4.081

4.5 Conclusion

To conclude this experiment, as predicted in the prelab, the $V_{PP} = 2\ V$showed no clipping, the $V_{PP} = 7\ V$showed clipping on the top, and the $V_{PP} = 10\ V$ showed clipping on both the top and bottom of the sinewave.

Experiment #5 Voltage Doubler

5.1 Purpose

The purpose of this experiment was to construct a voltage doubler circuit to study the output voltage and ripple voltage as the output load was changed.

5.2 Theoretical Background

Fig. 27 below represents a voltage doubler circuit that was constructed to study resulting output voltages and ripple voltages as the output load is changed. A voltage doubler is a type of voltage multiplier that multiplies the input peak by the specified integer. As the load changes, this also lowers the resulting output voltage.

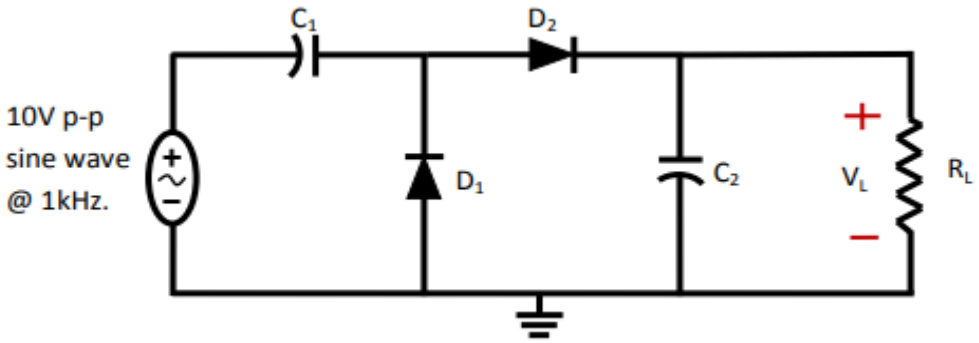

Figure 27: Voltage doubler circuit.

To find the voltage max and the ripple voltage, that was found by tracing the resulting graphs on LTSPICE. To find the average load voltage, the values found on the graph was used as well as equation (6) below.

$$V_L = V_{Max} - \frac{1}{2}V_r \qquad (6)$$

Where V_L is the average voltage load, V_r is the voltage ripple, and V_{Max} is the voltage peak.

5.3 Procedure

1. Fig. 27 was built using LTSPICE with a 10 V (p-p) at 1 kHz sine wave, a 1N914 diode, $C_1 = C_2 = 1\mu F$ and an initial RL = ∞ (open circuit).
2. A Transient Analysis was then applied for 200ms and maximum step size of 1us.
3. Then V_L(t) was plotted to find V_L at 190 ms.
4. Then an R_L =10 kΩ was applied with the same Transient Analysis as step 2.
5. Then V_L(t) was again plotted to measure the ripple around 190 ms and measure the average load voltage using equation (6).
6. Steps 4 and 5 was then repeated with an R_L of 1 kΩ then at 10kΩ, ensuring that V_0 reaches steady state.

7. Then both capacitors were changed to be $C_1 = C_2 = 10\ \mu F$ to then repeat steps 1 through 6.
8. Lastly, using Matlab, V_r was plotted as a function of load resistance for both capacitors on the same graph, and V_0 (DC) was plotted as a function of load resistance for both capacitors on the same graph. Then the effect of the capacitors on the ripple output voltage and the DC output voltage was commented on.

5.4 Results & Analysis

Fig. 28 below shows the LTSPICE model of Fig. 27 with parameters specified in steps 1 and 2 of procedure.

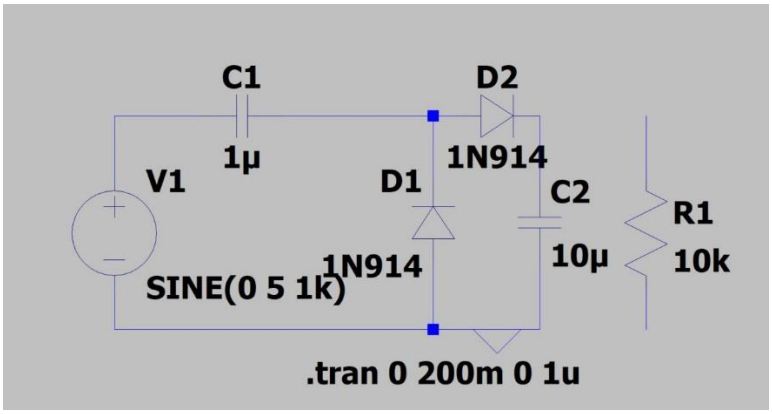

Figure 28: LTSPICE Circuit model of Fig. 27 with parameters specified in steps 1 and 2 of procedure.

Fig. 29 is the graph of Fig. 28 showing V_L(t) when R=∞ and $C_1 = C_2 = 1\mu F$. Figs. 30-32 are the graphs of Fig. 29 showing V_L(t) when R=1 kΩ, 5 kΩ, and 10 kΩ respectively, and $C_1 = C_2 = 1\mu F$, also R is attached to rest of the circuit to be parallel with C_2.

Figure 29: Plot of Fig. 27 showing V_L(t) when R=∞ and $C_1 = C_2 = 1\mu F$.

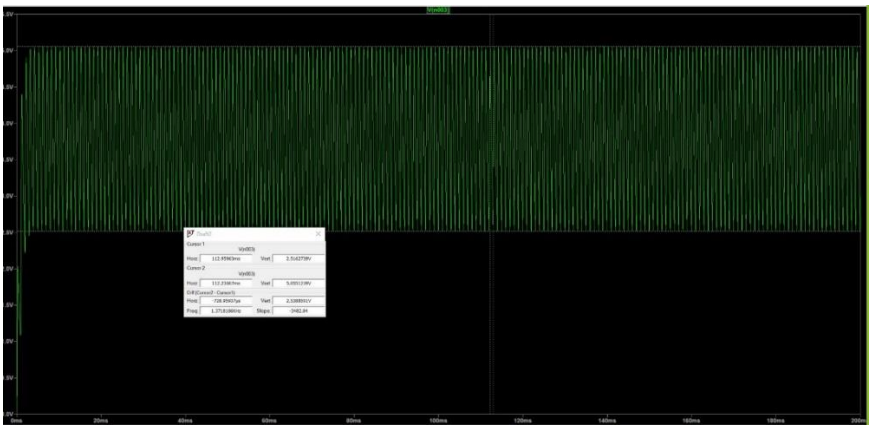

Figure 30: Plot of Fig. 27 showing the load resistor at 1 kΩ and $C_1 = C_2 = 1\mu F$.

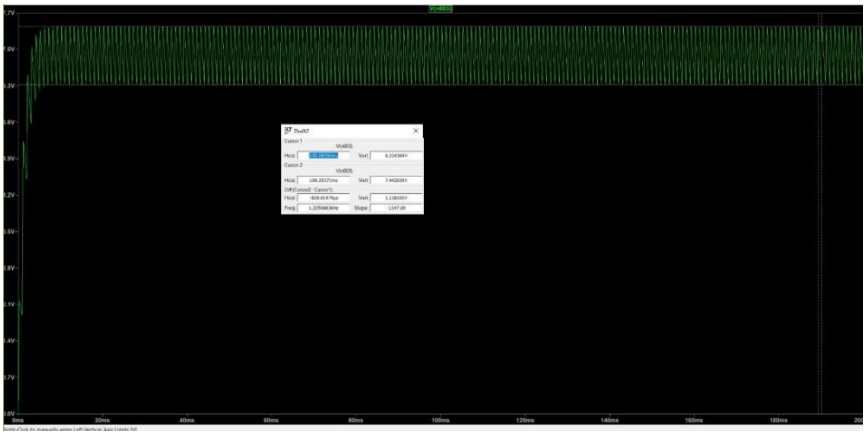

Figure 31: Plot of Fig. 27 showing the load resistor at 5 kΩ and $C_1 = C_2 = 1\mu F$.

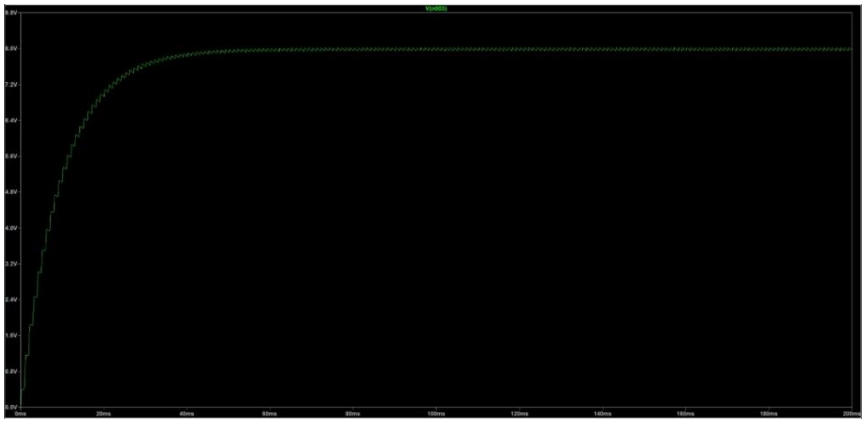

Figure 32: Plot of Fig. 27 showing the load resistor at 10 kΩ and C1=C2=1uF.

Fig. 33 is the graph of Fig. 28 showing V_L(t) when R=∞ and $C_1 = C_2 = 10\ \mu F$. Figs. 34-36 are the graphs of Fig. 29 showing V_L(t) when R=1 kΩ, 5 kΩ, and 10 kΩ respectively, and $C_1 = C_2 = 10\ \mu F$, also R is attached to rest of the circuit to be parallel with C_2.

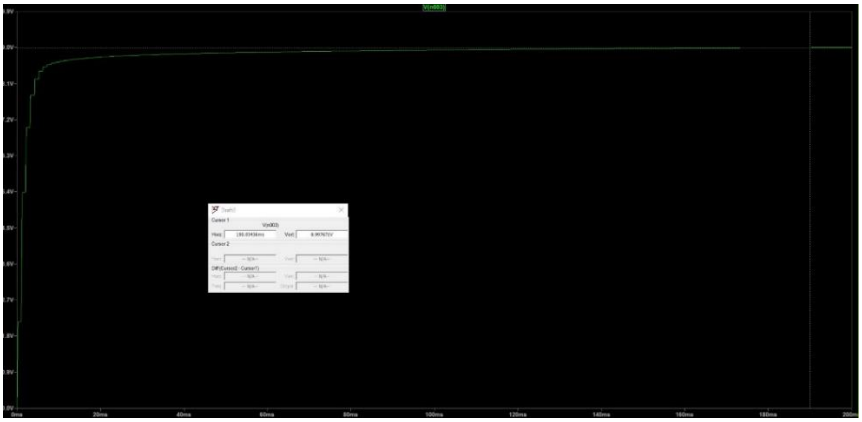

Figure 33: Plot of Fig. 27 showing V_L(t) when R=∞ and $C_1 = C_2 = 10\ \mu F$.

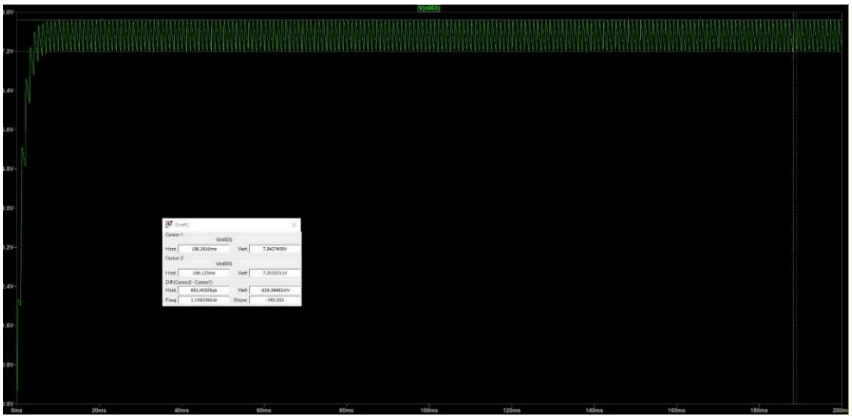

Figure 34: Plot of Fig. 27 showing the load resistor at 1 kΩ and $C_1 = C_2 = 10\ \mu F$.

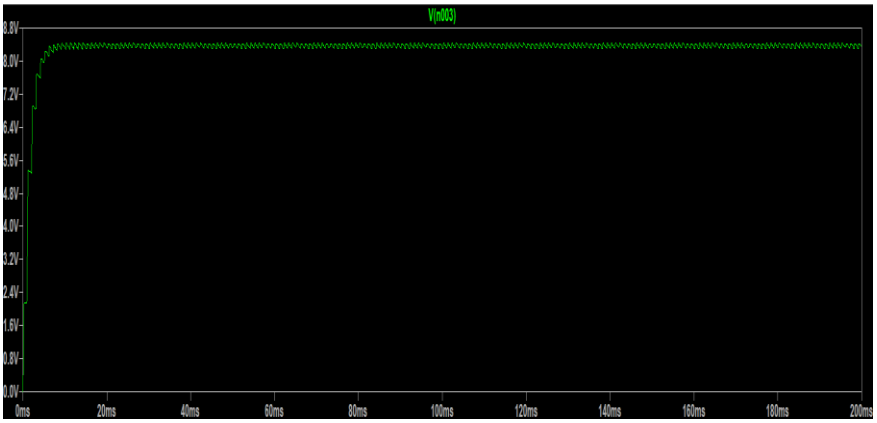

Figure 35: Plot of Fig. 27 showing the load resistor at 5 kΩ and $C_1 = C_2 = 10\ \mu F$.

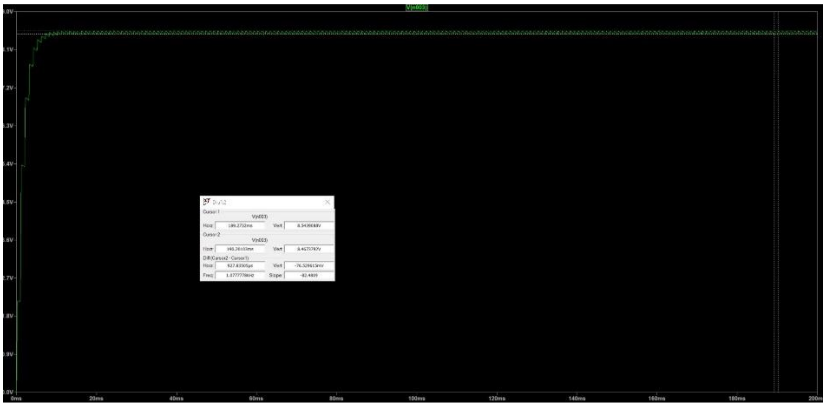

Figure 36: Plot of Fig. 27 showing the load resistor at 10 kΩ and $C_1 = C_2 = 10\ \mu F$.

Table 2 below illustrates the voltage, V_p at about 190 ms, the max voltage of the sinewave around 190 ms, V_{max}, and the ripple voltage of the sinewave at around 190 ms, V_r, and the average load voltage, V_L. V_L is found by using equation (6), and the correlating V_{max} and V_r values.

Table 2: Showing the voltages found or calculated using Figs. 29-36 as directed in steps 3, 5, 6, and 7 of the procedure.

Voltages	V_p (V)	V_{max} (V)	V_r (V)	V_L (V)
R=∞, C=1 uF	9.2	NA	NA	NA
R= 1 kΩ, C= 1 uF	3.52	5.055	2.539	3.785
R= 5 kΩ, C= 1 uF	6.428	7.44	1.118	6.881
R= 10 kΩ, C= 1 uF	7.464	8.046	.6498	7.72
R=∞, C=10 uF	8.998	NA	NA	NA
R= 1 kΩ, C= 10 uF	7.288	7.84	.6394	7.52
R= 5 kΩ, C= 10 uF	8.32	8.446	.1496	8.371
R= 10 kΩ, C= 10 uF	8.48	8.544	.07652	8.506

Fig. 37 shows the resulting Matlab graphs from the code found in appendix C that is the product of step 8 of the procedure. To comment on the effect of the capacitors on the ripple output voltage and the DC output voltage is that the output voltage was greater with higher capacitance and the ripple voltage was smaller. The input voltage in all these scenarios was the same meaning the current to the resistor was roughly the same. With this being said, the greater the capacitance and resistance, the smaller the discharge. Then the smaller the capacitance and resistance, the larger the discharge due to the current equation of a capacitor. When the voltage ripple is small, the average load voltage is greater, meaning that the greater the capacitance, the greater the average voltage.

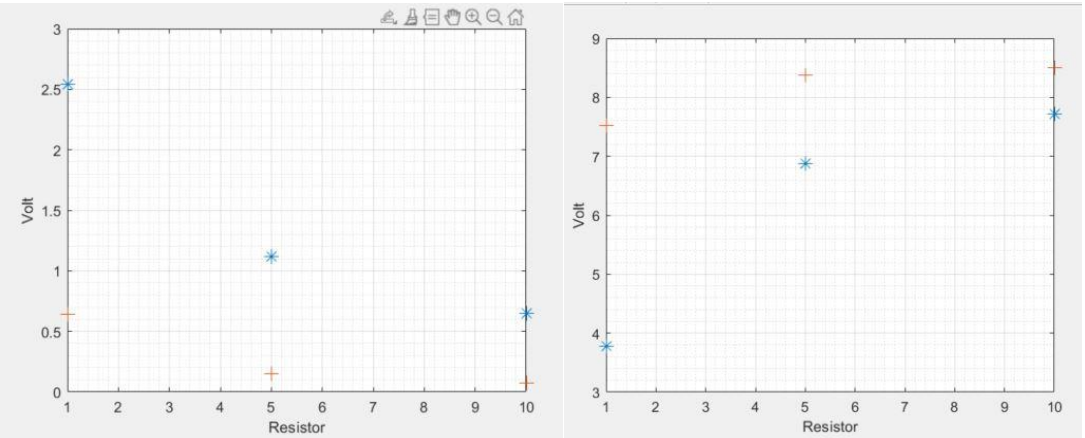

Figure 37: Matlab graphs of (a) V_r and (b) V_L.

5.5 Conclusion

To conclude this experiment, some distinct relations were proved. These relationships being that the greater the capacitance and resistance, the smaller the discharge and the greater the average load voltage. The other relationship being that the smaller the capacitance and resistance, the larger the discharge and the smaller the average load voltage. These relationships were best shown in Fig. 37, which shows the plots comparing the two capacitor values at three different resistance values.

Appendix

Appendix A:

Lab 5 Checklist:

Name:_____

Lab title and introduction

- Lab title, your name, date, and lab partner.
- Brief introduction (two or three sentences) explaining the purpose of this lab.

I. Diode Forward Characteristics. (30 pts total)

(a) Switching Diode 1N914 and Rectifier diode 1N4001

1. Diagram of circuit (Fig. 1) with measured value for R.
2. Table and Graph of measured (I_D, V_D) for switching and rectifier diodes.

(b) Diode Parameter Calculations

1. Values of Is and n based on two data points
2. Values of Is and n based on least-squares fit of data

II. Zener Diode Characteristics (15 pts total)

(a) Diagram of circuit in Figure 2 with the measured value of R.
(b) Zener Diode, 1N4735

1. Table of measured values and plot of data.
2. Calculated V_{z0}, r_z and I_z,*min*

III. Zener Diode Voltage Regulator (25 pts total)

1. Draw circuit diagram in Figure 3 with measured value of resistor.
2. Plot load voltage as a function of load current and Zener current.
3. Plot output ripple voltage V_r (p-p) at 5mA .

IV. Diode Clipping/Limiting Circuit (15 pts total)

1. Draw circuit diagram used in Figure 4.
2. Plot input and output voltages for all three voltages.
3. Discussion of circuit's operation (how does it work?).

V. Voltage Doubler Circuit: (15 pts total)

1. Draw circuit diagram (Figure 5).
2. Discussion of circuit's operation.
3. Plot V_{out} and $V_{r(p-p)}$ as a function of load resistor.

Appendix B

```
Vt=.026;
n=1.87;
Vd= linspace(0,.8);
Is=6.3e-9;
Id=Is*exp(Vd/(n*Vt));
plot(Vd,Id);
grid on
grid minor
```

Figure B: Experiment 1 Matlab code.

Appendix C

```
clear all
close all
clc
% To plot data
% 1- enter the x variable as a vector (here it is R)
R=[1 5 10];
% 2- Enter the y variable as a vector
V1=[2.539 1.118 .64976];
V2=[.6394 .14955 .07652];
% 3- plot the data
figure
plot(R,V1,'*',R,V2,'+','MarkerSize',10);
xlabel('Resistor')
ylabel('Volt')
grid on
grid minor

%Example of ploting two or more functions on the same grph.
% 1- enter the x variable as a vector (here it is R)
R=[ 1 5 10];
% 2- Enter the y variables as a vector
V3=[3.785 6.881 7.72];
V4= [7.52 8.371 8.50374];

figure
plot(R,V3,'*',R,V4, '+','MarkerSize',10);
xlabel('Resistor')
ylabel('Volt')
grid on
grid minor
```

Figure C: Experiment 5 Matlab code.