Washington State University

School of Electrical Engineering and Computer Science

EE 352 Electrical Engineering Laboratory

Lab # 8

MOSFET Amplifier Circuits

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Due Date: 04/12/21

Lab Overview

This lab was about the practical MOSFET circuits. In this lab, single source common source MOSFET amplifiers as an example of a discrete amplifier circuit were designed, simulated and experimentally validated. Then a current mirror source was designed using a pair of matched transistors. Last, a CMOS inverter was then built using complementary NMOS and PMOS transistors to determine its voltage transfer curve then finally the inverter was properly biased to work as a single stage CMOS amplifier.

Experiment #1 Single Stage Common Source Amplifier

1.1 Purpose

The purpose of this experiment was to design, simulate and analyze a single stage common source MOSFET amplifier. The variables found in this experiment were the mid-band gain of the amplifier, and the low cutoff frequency and high cutoff frequency. Then to verify the drain voltage both before and after the capacitor on the circuit.

1.2 Theoretical Background

Metal Oxide Semiconductor Field Effect Transistor, or MOSFET for short, is used for small signal linear amplifiers as their input impedance is extremely high making them easy to bias. The main goal of a MOSFET amplifier, or really any amplifier, is to produce an output signal that is a consistent reproduction of its input signal but linearly amplified in magnitude. This input signal could be a current or a voltage, but for a MOSFET device to operate as an amplifier it must be biased around a centrally fixed Q-point to operate within its saturation region.

There are two basic types of enhancement-mode MOSFETs, n-channel (NMOS) and p-channel (PMOS). Then NMOS is operated with positive gate and drain voltages relative to the source as opposed to the p-channel PMOS which is operated with negative gate and drain voltages relative to the source.

The saturation region of a MOSFET device is its constant-current region above its threshold voltage (V_T). Once correctly biased in the saturation region the drain current (I_D) varies because of the gate-to-source voltage (V_{GS}) and not by the drain-to-source voltage (V_{DS}) since the drain current saturated. The threshold voltage is the minimum gate bias required to enable the formation of the channel between the source and the drain when the value is greater than the threshold voltage, the drain current increases in proportion to $(V_{GS} - V_T)^2$in the saturation region allowing it to operate as an amplifier.

A single stage common source MOSFET amplifier circuit is shown in Fig. 1(a) below, and Fig. 1(b) shows Fig. 1(a) as a DC circuit.

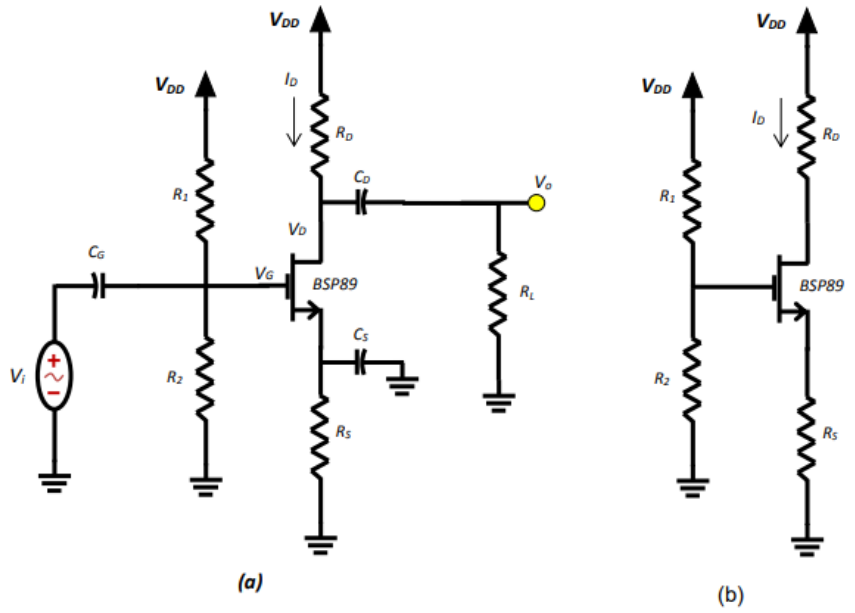

Figure 1: (a) Common Source MOSFET Amplifier (b) DC Circuit of the Amplifier.

For the prelab, the objective was to design the amplifier to meet the specifications listed on Table 1 below by choosing $R_1, R_2, R_D, and\ R_S$ resistors as well as the bias current I_D. To calculate both the theoretical and experimental values for R_{in}, R_o, G_v, and g_m, equation (1), (2), (3), and (4) below were used. R_{in} and R_o are the input and output resistances of the circuit, G_v is the mid-band gain of the amplifier, and g_m is the transductance of the amplifier.

Table 1: List of Variables and their Specifications for the Circuit shown in Fig. 1.

Variables	Specifications			
Resistances	$R_L = 100\ k\Omega$	$R_{in} > 200\ k\Omega$		
Gain/ constants	$G_v = -50 \pm 20\%$	$\lambda = .01\text{V}^{-1}$	$k_n \approx .1\ A/V^2$	Nominal: $\approx 34\ dB$
Voltages	$V_{DD} = 15\ V$	$V_T \approx 1.7\ V$	$V_A = 100\ V$	$V_{DD} > V_D > V_G - V_T$
Voltages	$V_G = \frac{1}{3}V_{DD} = 5\ V > V_T$			
Capacitors	$C_G =$ 10 µF	$C_S =$ 47 µF	$C_D =$ 10 µF	
Current	$I_D \approx$ .3 mA			

$$R_{in} = R_1 \,||R_2 \quad (1)$$

$$r_o = \frac{1}{\lambda I_D} \qquad (2)$$

$$R_o = R_D \,||R_L||r_o \qquad (3)$$

$$g_m = -\frac{G_v}{R_o} = -\frac{\left(\frac{V_o}{V_i}\right)}{R_o} = \sqrt{2k_n I_D} = k_n(V_{GS} - V_T) \qquad (4)$$

The values chosen for $R_1, R_2, R_D, and\ R_S$ as well as I_D were 900 $k\Omega$, 450 $k\Omega$, 5.405 $k\Omega$ (found using equation (3)), 6.4 $k\Omega$ (justified with Ohms law), and .5 mA respectively. r_o was calculated using

equation (2) and known variables and resulted in 200 $k\Omega$. From there, using equation (3), g_m was found to be .01, V_{GS} was 1.8 V, V_S was found to be 3.2 V, and R_o was 5 $k\Omega$.

1.3 Procedure

1. Using LTSPICE, Fig. 1(b) was built using BSP89 NMOS transistor and the prelab design values with DC operating point analysis to measure the DC current and verify the transistor is in the saturation region.

2. Using LTSPICE, Fig. 1(a) was built with a 1V AC input voltage, and AC

Analysis with a decade sweep of 1000 points per decade, and starting frequency from

10 Hz to 10 MHz. This was plotted to measure mid-band gain at 20 kHz to be about 34 dB and the low cutoff frequency f_L and the high cutoff frequency f_H.

3. The LTSPICE 1(a) circuit then had a changed input voltage of a 20 mV peak-to-peak (10mV peak) sinusoidal input signal at 20 kHz with a transient analysis with stop simulation time =500 µs and maximum simulation time 50 ns. The output voltage to the right of the capacitor (C_D) was plotted to determine gain and then separately the drain voltage to the left of the capacitor (C_D) was plotted to find the middle voltage value.

4. The amplitude of the input sine wave was then increased to 1 volt at 20 kHz and the drain voltage was plotted to observe the clipping at the max and min of the voltage range.

1.4 Results & Analysis

Fig. 2 below shows the LTSPICE model of Fig. 1(b), and Fig. 3 shows the LTPICE model of Fig. 1 (a), both using the calculated, chosen and assigned values from the prelab and steps 1 and 2 from the procedure. When running the DC operating point analysis, the DC current was measured to be .538 mA. The transistor is verified to be in the saturation region because the operating analysis also reveals that V_{DS} is measured to be at 3.44 V, while V_G is measured to be 5 V. This means then when inserting these values into the inequality $V_{DS} > V_G - V_T$, 3.44 V> 3.33 V, which is true.

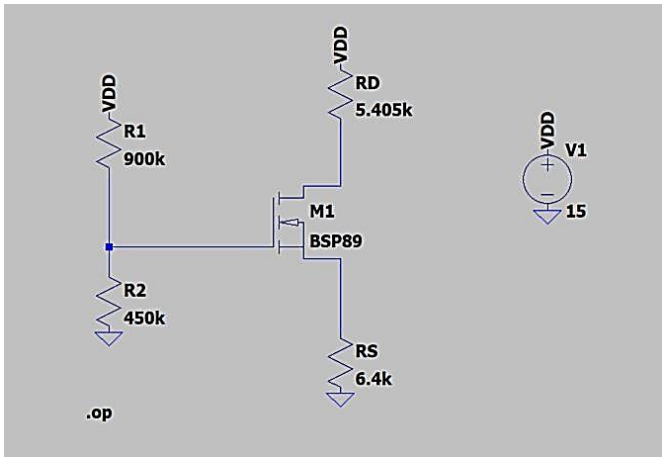

Figure 2: LTSPICE Circuit of Fig. 1(b).

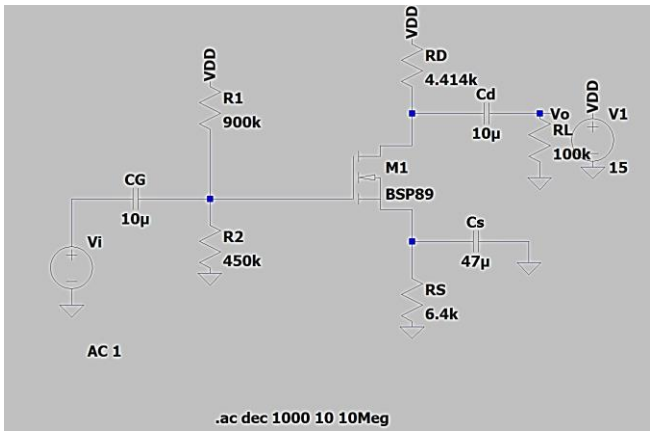

Figure 3: LTSPICE Circuit of Fig. 1(a) with AC input voltage.

Fig.4 below shows the gain plot of Fig. 3 with the measured midband gain value at 20 kHz. As shown in Fig.3, R_D was adjusted by $\sqrt{\alpha}$ because the gain with the original $R_D$value was 35.728 dB which is too off from the desired midband gain of 34 dB or 50.11 V/V. $\sqrt{\alpha}$ was determined by converting the gains to V/V then dividing the desired midband gain by the original midband gain. $\sqrt{\alpha}$ was then multiplied by 5.405 $k\Omega$ to get the new value of 4.414 $k\Omega$. With the new R_D value, the midband gain at 20 kHz was found to be 34.104 dB, which is within 20% error of the desired midband gain of 34 dB, being .306% error. The cutoff frequencies were found by using the cursors for both the left and right of the midband gain by a difference of $\pm 3\ dB$. The high cutoff frequency was measured to be .588 MHz and the low cutoff frequency was measured to be 41.02 Hz.

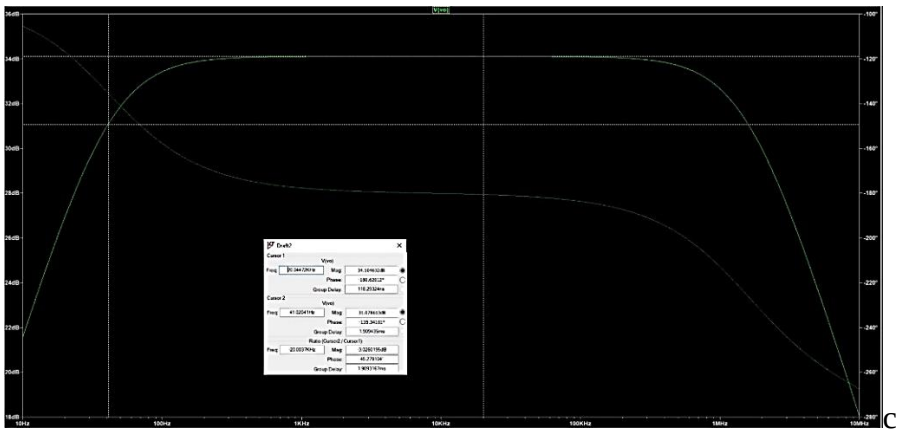

Figure 4: Gain plot of Fig. 3 with measured midband gain and cutoff frequency.

Fig. 5 below shows the circuit of Fig. 3 with a sinusoidal input voltage with a $V_{P-P} = 20\ mV$, and the other specifications stated in step 3 of the procedure.

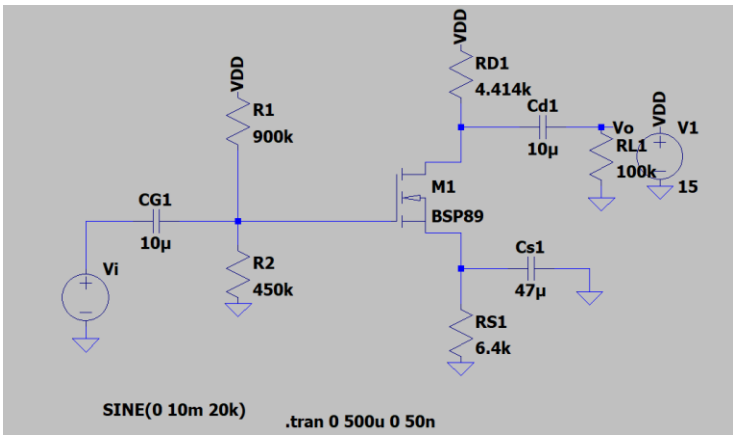

Figure 5: Fig. 3 with Sine Input Voltage with 20 mV_{P-P}.

Fig. 6 below is the plot of the load output voltage of Fig. 5 after C_D, and Fig. 7 below shows the drain voltage before C_D. The peak-to-peak voltage for both graphs were measured to be 1.017 V, with the mid-voltage being 0 V for the load output and 12.79 V for the drain voltage. From these plots, it is known that there is sign inversion because the peak closest to 0 Hz is negative.

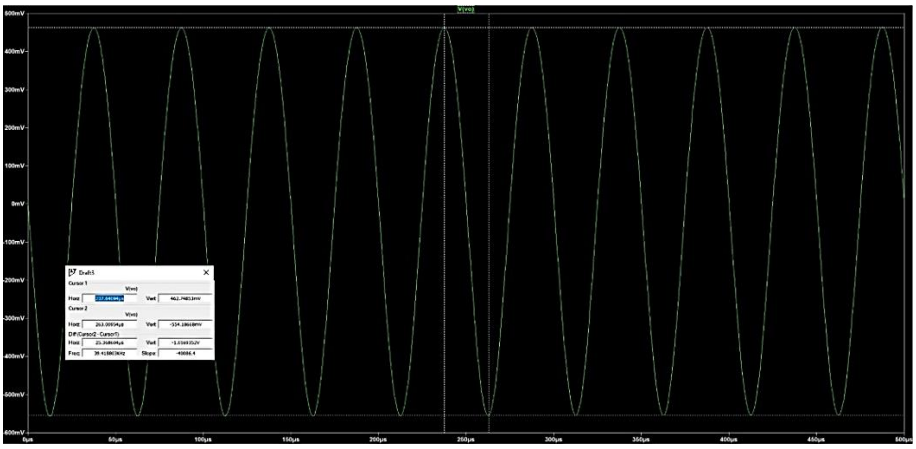

Figure 6: Plot of Fig.5 showing load output voltage (V_o) after C_D.

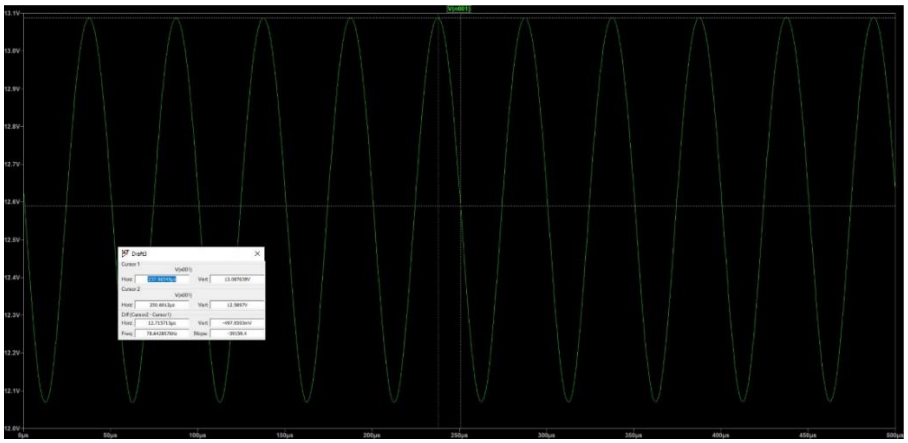

Figure 7: Plot of Fig.5 showing drain voltage (V_D) before C_D.

Fig. 8 below shows the same circuit as in Fig. 5, only now with a zero-to-peak voltage of 1 V instead of 10 mV. Fig. 9 below shows the plot of V_D for Fig. 8 with clipping at both the min and max voltage peaks. $V_{D,max}$ was measured to be 14.903 V and $V_{D,min}$ was found to be 3.46 V. The clipping is due to the transistor being past its limit of its max voltage magnitude.

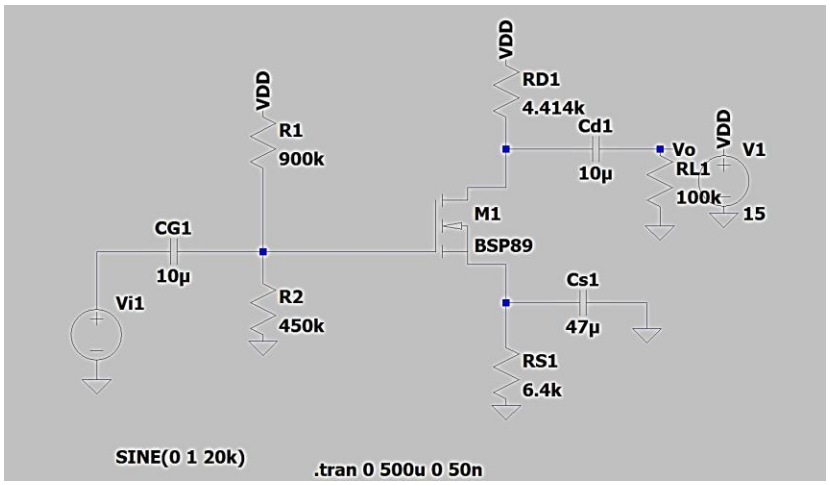

Figure 8: Fig. 3 with Sine Input Voltage with 1 V_{P-P}.

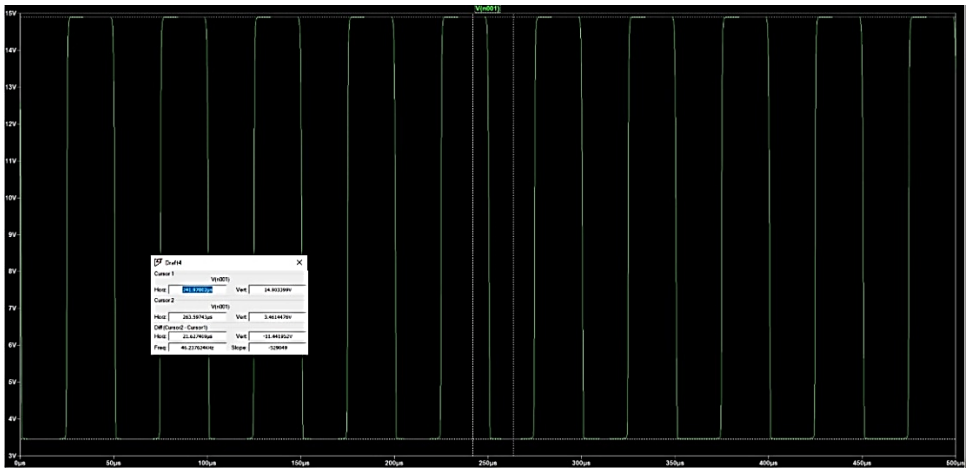

Figure 9: V_D plot of Fig. 8 showing clipping at both the max and min.

1.5 Conclusion

To conclude this experiment, the original midband gain of the AC circuit was initially a 22% error from the desired gain of 34 dB, or 50.11 V/V. Once R_D was adjusted by $\sqrt{\alpha}$, the new gain was only a .302% error from the desired gain, which is within 20% error, as specified in Table 1.

Experiment #2 Current Mirror Circuit

2.1 Purpose

The purpose of this experiment was to design a current mirror source circuit to have $I_2 \approx 2I_1$.

2.2 Theoretical Background

In an analog VLSI design, amplifiers are biased using current mirror sources due to their efficient structure in terms of area and power consumption. Usually, VLSI designers adjust the W/L ratio for each transistor to provide desired bias current. In the circuit shown in Fig. 10, Q1 as a reference transistor that provides I_{Ref} through R which biases the gate voltage to a predetermined V_G value. The gate voltage is then reflected to Q2 which acts as the biasing current source that biases the circuit. The current of Q2, or the bias current, is adjusted by designing the proper W/L ratio of Q2. In this experiment, a current mirror source was built to supply constant DC current using matched NMOS transistor within the CD4007 IC chip. Fig. 10 is the current mirror source circuit that was designed. This circuit contains two transistors, Q1 and Q2, which are ideally identical since they have the same processing parameters $(V_t, K_n, \gamma, \dots)$.

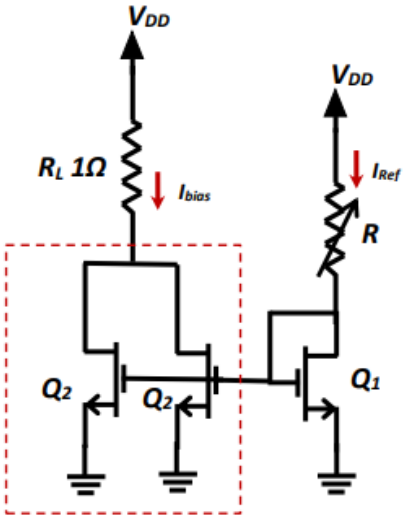

Figure 10: Current mirror source.

Equation (5) below is the set of equations used to determine the current in Q2. This equation expresses that I_2 can easily be designed by controlling the size of the transistors.

$$\frac{I_2}{I_1} = \frac{\frac{1}{2}K_n'\left(\frac{W}{L}\right)_2(V_{GS}-V_T)^2(1+\gamma V_{DS2})}{\frac{1}{2}K_n'\left(\frac{W}{L}\right)_1(V_{GS}-V_T)^2(1+\gamma V_{DS1})} = \frac{\left(\frac{W}{L}\right)_2(1+\gamma V_{DS2})}{\left(\frac{W}{L}\right)_1(1+\gamma V_{DS1})} \approx \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \quad (5)$$

For the prelab, the objective was to use equation (5) and the given variables to calculate a R for the circuit. The information given was that I_{Ref} was 1 mA through the NFET Q1, V_{DD} was given as 5 V, K_n was given as . 1 A/V^2, V_t was given as 1.7 V, and λ was given as 0. Using equation 5 for just I_1, R was found to be 3.16 $k\Omega$.

2.3 Procedure

1. Fig. 10 was built using LTSPICE, with BSP89 NMOS transistors and the prelab designed value for R. The current mirror circuit of Fig. 10 fit the parameters given in the prelab with a I_{Bias}≈ 2 mA by connecting the transistors in parallel to build Q2.

2. DC operating point analysis was used to measure I_{Ref}≈1 mA, and I_{Bias}≈ 2 mA.

3. Then it was investigated when Q2 is in the saturation region, where the bias current was roughly constant. This was done by using the .step param command to vary the load resistor for 1 Ω to 5 kΩ with steps of 100Ω. R_L was changed from 1Ω to {X} and the command '.step param X 1 5k 100' was entered into the schematic. Then the DC operating point was used to simulate the circuit to plot I_{Ref} and I_{Bias}vs. R_L.

2.4 Results & Analysis

Fig. 11 below shows the LTSPICE circuit model of Fig. 10 with the parameters specified in step 1 of the procedure. As specified in step 2 of the procedure, after conducting the DC operating analysis, the I_{Ref} was shown to be 1.078 mA, and I_{Bias} was shown to be 2.22 mA.

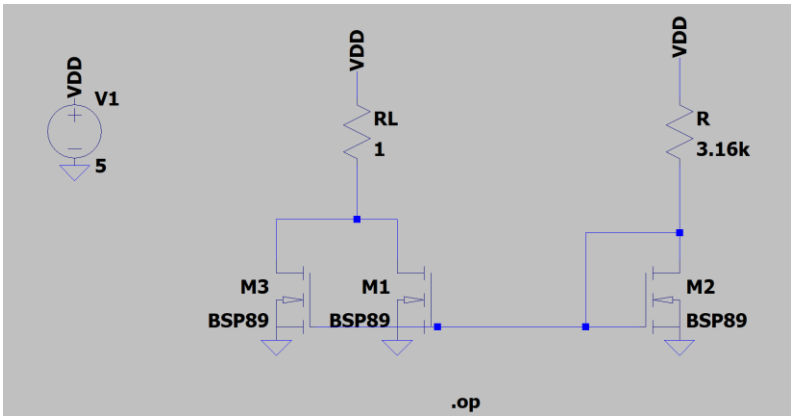

Figure 11: LTSPICE model of Fig. 10 with op. Analysis.

Fig. 12 below shows the circuit in Fig.11 with changed parameters stated in step 3 of the procedure. Fig. 13 is the plot specified in step 3 of the procedure for Fig. 12. The behavior of the graph fit the description of the expected behavior in the lab assignment where when Q2 is in the triode region, the bias current is not well regulated so drops linearly, in the saturation region, Q2 shows a roughly constant biased current.

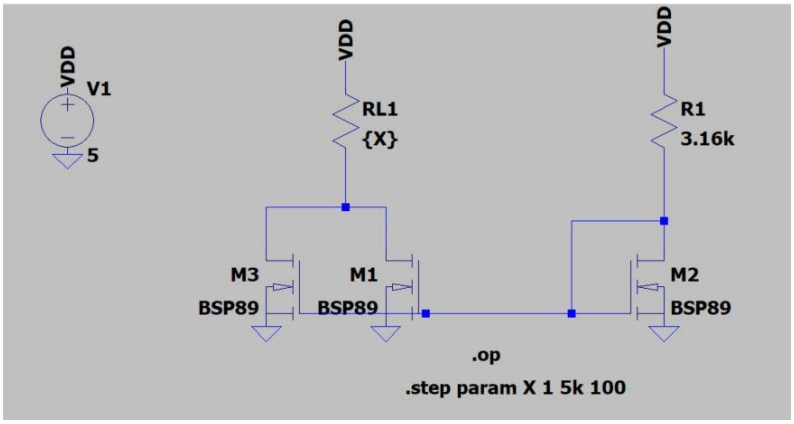

Figure 12: Fig. 11 Circuit with .step param Analysis.

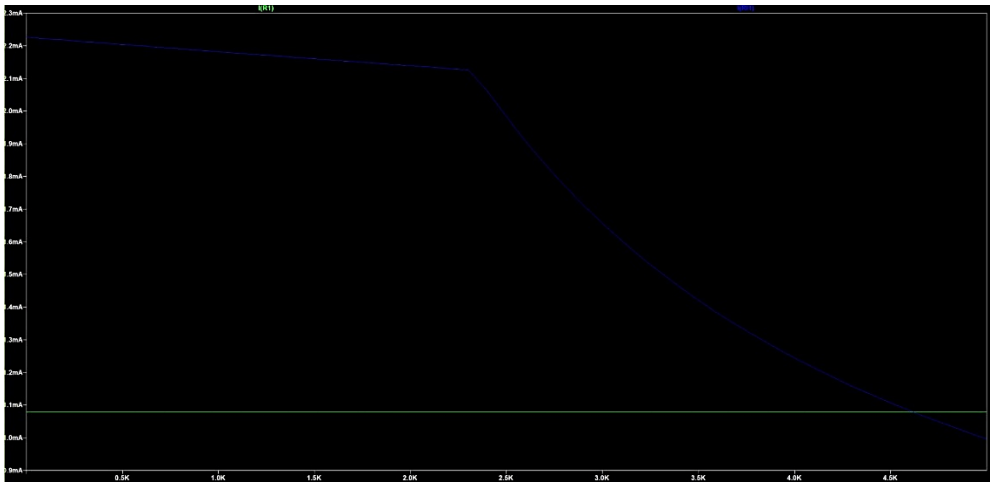

Figure 13: Graph of Fig. 12 Showing I_{Ref} and I_{Bias}vs. R_L.

2.5 Conclusion

To conclude this experiment, the I_{Ref} and I_{Bias}vs. R_L shown in LTSPICE showed the expected behavior where when Q2 is in the saturation region, the bias current is roughly constant. In the triode region, the bias current is not well regulated, so it drops linearly. Also, the values for I_{Ref} and I_{Bias} were around 1 mA and 2 mA respectively at 1.078 mA and 2.22 mA.

Experiment #3 Function Generator and Oscilloscope

3.1 Purpose

The purpose of this experiment was to build a CMOS inverter to investigate the different regions of the inverter, then the inverter in region 3 was biased and tested as an amplifier.

3.2 Theoretical Background

CMOS technology uses NMOS and PMOS transistors that act as complementary switching transistors on the same wafer (substrate) or chip. The complementary transistors work in a push-pull mechanism such that when one transistor is ON then it becomes a short circuit, but when it is OFF it acts as open circuit. The push-pull switching mechanism is commonly used in building digital circuits. The simplest digital CMOS circuit is the inverter which is made of a PMOS transistor and an NMOS transistor as shown in Fig.14. When the CMOS inverter's input V_i=0 V (logical low) then the NMOS transistor is OFF ($V_{GSn} < V_{Tn}$) but the PMOS transistor is ON ($V_{GSp} > |V_{Tp}|$) and I_D=0 because NMOS is off and PMOS is ON which means PMOS is operating in the triode region and V_{DSp} =0 which implies $V_o = V_{Dp} = V_{Sp} = V_{DD}$ (Logical High). Similarly, when $V_i = V_{DD}$ (logical High) then the NMOS is ON, PMOS is OFF and I_D=0. In this scenario, the NMOS is in the Triode region and V_{DSn} = 0 which implies that $V_o = V_{Dn} = V_{Sn}$ = 0 (logical Low).

During the transition from 0 V (low) to V_{DD} (high), the CMOS inverter transitions through five operating regions as shown in Fig. 15; these regions are summarized in Table 2. Here, the current is non-zero when the output of the inverter is transitioned; so, the power dissipation is non-zero which means it is proportional to the switching frequency. In Region 3 of the figure, $\left|\frac{dV_o}{dV_i}\right|$ is maximum, acting as an amplifier.

Table 2: Summary of the five CMOS inverter transition regions

	NMOS	PMOS	V_i	I_D	V_o
Region 1	OFF	Triode	LOW	0	High V_{DD}
Region 2	Saturation	Triode	LOW	Small	High ≈ V_{DD}
Region 3	Saturation	Saturation	Medium	High	Mixed > 0 & < V_{DD}
Region 4	Triode	Saturation	High	Small	Low ≈ V_{DD}
Region 5	Triode	OFF	High	0	Low (0 V)

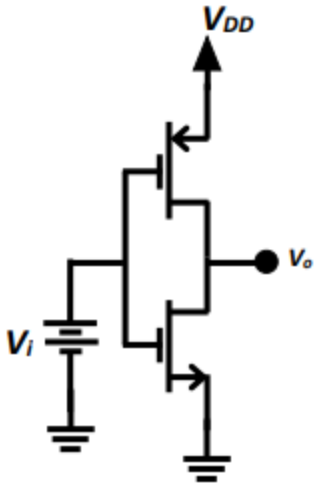

Figure 14: CMOS inverter.

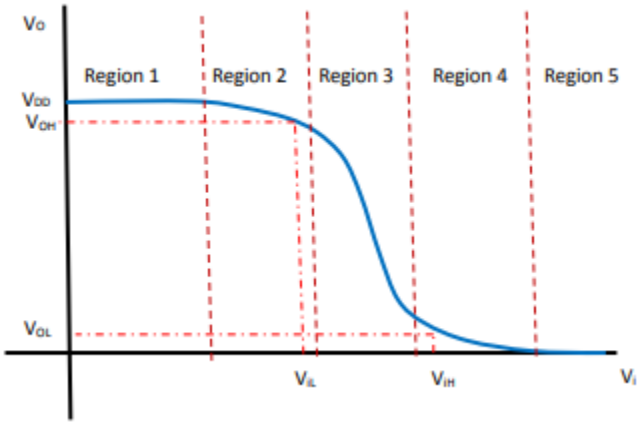

Figure 15: The voltage transfer curve of CMOS inverter.

There was no prelab for this experiment.

3.3 Procedure

1. LTSPICE was used to build the CMOS inverter using the BSP89 NMOS and BSS 84 PMOS transistor with V_i applied to be DC voltage source.

2. A DC Sweep Analysis was used to sweep V_i linearly from 0 V to 5 V with a step size of 1 µV to plot the voltage transfer curve (V_o vs. V_i). Then a cursor was used to record V_i when V_o =2.5V (mid voltage value). Then the gain ($\frac{\Delta V_o}{\Delta V_i}$) was found at the midpoint voltage.

3. Then the input voltage was changed to a sine wave with the offset voltage being the midpoint voltage found in step 2, and amplitude was set to 2mV peak-to-peak, and the frequency was set to be 1 kHz.

4. A transient analysis was applied for 10ms with maximum step size of 1us. Then V_o (t) was plotted to record the peak-to-peak output voltage and determine the gain. The sign inversion was also observed.

3.4 Results & Analysis

Fig. 16 below shows the LTSPICE circuit model of Fig. 14 with specified parameters in steps 1 and 2 of the procedure. Fig. 17 is the resulting plot of Fig.16 showing V_o vs. V_i to find the V_i of 2.024 V at V_o =2.5 V. The gain was then found to be 961.54 V/V using $\frac{\Delta V_o}{\Delta V_i}$ with using the points (2.024159,2.4) V and (2.024367, 2.6) V.

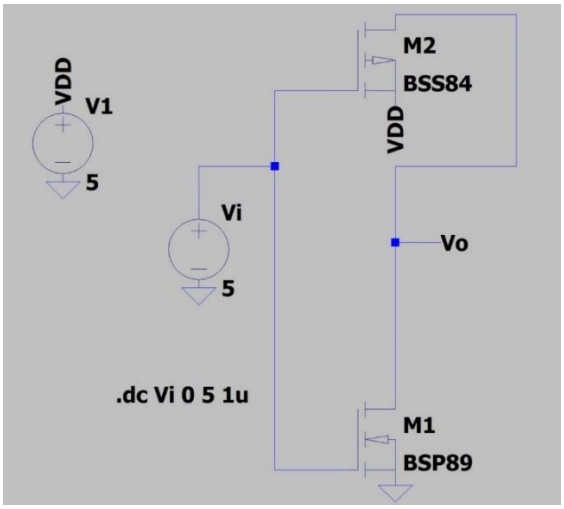

Figure 16: LTSPICE model of Fig. 14 with DC analysis.

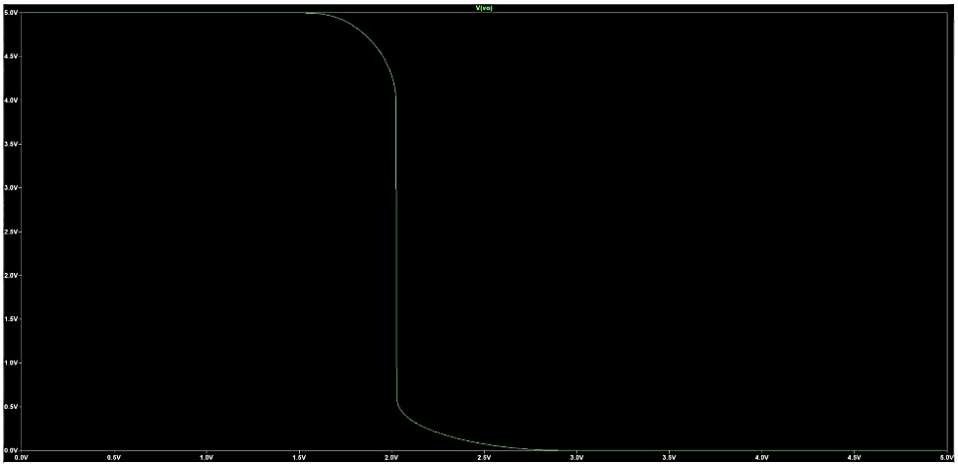

Figure 17: V_o vs. V_i plot of Fig. 16 showing AC drop.

Fig. 18 below shows the circuit in Fig. 16 with input sine voltage with the 2.024 V for the offset voltage. The other parameters were from step 3 of the procedure. Fig. 19 was the resulting V_o (t) plot showing inversion due to the first peak to the left of the plot being negative. The gain of

V_o (t) was 963.5 V/V and the peak-to-peak value was 1.927 V for the output voltage. The error between the two gains were .203% which means the circuit is relatively accurate.

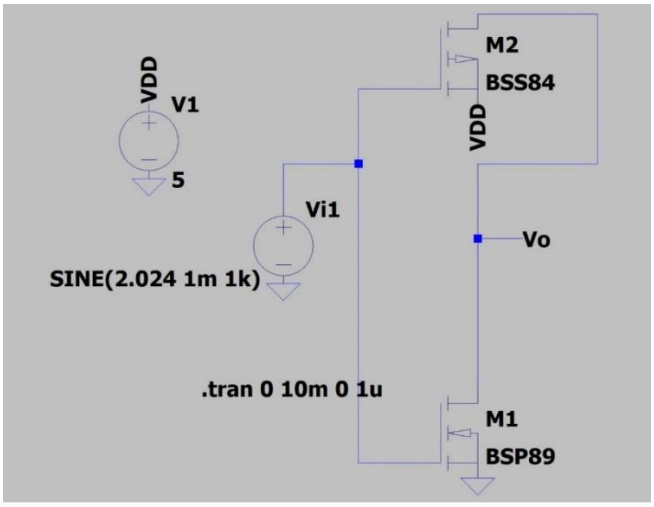

Figure 18: Fig. 16 with Sine Input Voltage with Mid-Voltage Value.

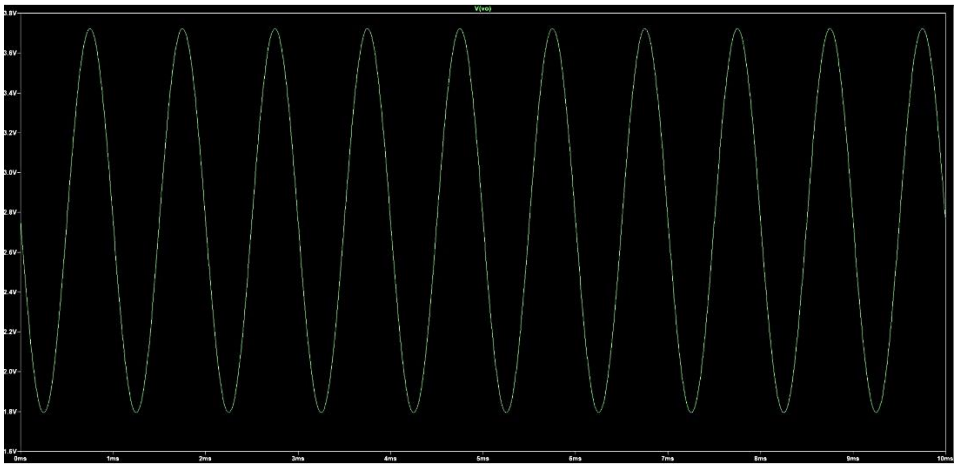

Figure 19: Sinewave Plot for Fig. 18 for V_o (t).

3.5 Conclusion

To conclude this experiment, the V_o vs. V_i plot showed the midpoint V_i to be 2.204 V and the calculated gain to be 961.54 V/V or 59.66 dB. This led to the V_o (t) having a sign inversion between the two voltages of about a 963.5 V/V gain and a peak-to-peak value of 1.927 V for the output voltage. The error between the two gains were .203%. This means the circuit was relatively accurate.

Appendix

Appendix A

Lab 8 Checklist

Name:_____

Lab title and introduction

- Lab title, your name, date, and lab partner.
- Brief introduction (two or three sentences) explaining the purpose of this lab.

I. Single Stage MOSFET Amplifier (45 pts total)

1. Diagram of amplifier.
2. Measured component values: R_1, R_2, R_S, R_D, R_L, C_G, C_D, C_S
3. Measured DC voltages: V_G, V_S, V_D, I_D
4. Measured mid-band gain.
6. Measured values of upper and lower corner frequencies.
8. Plot of measured gain vs. frequency.
9. Plot of the Midband gain at 20kHz sine wave
9. Plot of the Maximum peak-to-peak output swing.

II. Current Mirror Source (25 pts total)

1. Diagram of current mirror circuit.
2. Table of measured values of I_{Ref} and I_{Bias} compared with expected values
3. Plot of the bias current vs the load resistance.

III. CMOS Inverter (30 pts total)

1. Diagram of CMOS inverter.
2. Table of measured V_i vs. V_o for the voltage transfer curve.
3. Plot the voltage transfer curve.
4. Measured amplifier gain at the midpoint of V_o.
5. Plot of the output voltage with the sine wave input voltage.