Washington State University

School of Electrical Engineering and Computer Science

EE 352 Electrical Engineering Laboratory

Lab # 7

MOSFET Circuits

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Lab Overview

In this lab, the I-V characteristic was experimentally obtained for two types of the MOSFET transistors, NMOS and PMOS. This was done using LTSPICE as a Curve Tracer to obtain the I-V curves for the NMOS and PMOS. After the curves were obtained, the essential parameters were estimated from the curves. Then ZVN2110A NMOS was used as a voltage controlled variable resistance in the deep triode region. Finally, the IRF510 NMOS power transistor was used as a power amplifier. The outcome of the power amplifier was that initially it received a weak power signal and then amplified its power at the output.

Experiment #1 MOSFET I-V Characteristics

1.1 Purpose

The purpose of this experiment was to use LTSPICE as a curve tracer to obtain I-V curves for the BSP89 NMOS and the BSS 84 PMOS transistors. Using the curves, then the purpose was to experimentally calculate the essential parameters.

1.2 Theoretical Background

The MOSFET is the most commonly used compact transistor in digital and analog electronics. It has revolutionized electronics in the information age. The flow of current is established in a MOSFET device due to the formation of an inverted charge layer. This inversion of charge is controlled by the controlling terminal called the “Gate terminal.” Thus, this controlling action of the current between two terminals called the “Drain,” and the “Source” by a third “Gate” terminal is what gives us the transistor action. The enhancement mode MOSFET is related to n-channel which has no inversion layer when a zero voltage is applied at the gate terminal; this is the NMOS transistor. The depletion mode MOSFET has an inversion channel referred to the p-type, due to the threshold voltage of a MOS having a p-type substrate being present at zero voltage. Other differences between the PMOS and NMOS is that the threshold voltage is negative for the PMOS while it is positive for the NMOS, the majority carriers in the inversion channel are mostly electrons for the NMOS and holes for the PMOS, and the NMOS can be switched faster than the PMOS.

The I-V graphs for each transistor, including a $I_D vs\ V_{DS}$ and a family of $I_D vs\ V_{DS}$ curves at multiple steps of V_{GS} were plotted and the parameters ($k_n, k_p, V_t, g_m, and\ \lambda$)were experimentally calculated using the curves and the equations listed in table 1.

For the prelab, section 5.2 of the Sedra and Smith textbook were read, and Fig. 5.14 on pg. 264 and Fig. 5.17 on pg. 268 were referred to for this experiment. The I-V equations for the NMOS and PMOS transistors in the cutoff, triode, and saturation regions with the stated conditions for each region is as follows in equations (1) to (7) below represented in table 1. Equations (8) and (9) represent the two equivalent expressions for the transductance in each saturation for the NMOS and PMOS.

Table 1: Showing Region measured, The Equations and Conditions for the NMOS and then for the PMOS

Region	NMOS		PMOS	
	Equation	Conditions	Equation	Condition
Cutoff	$I_D = 0$	$V_{GS} < V_{TN}$, Q = off	$I_D = 0$	$V_{GS} > V_{TP} < 0$, Q = off
Triode	$I_D = k_n[(V_{GS} - V_{TN})V_{DS} - \frac{1}{2}V_{DS}^2$ (1)	$V_{GS} > V_{TN}$ $V_{DS} < V_{GS} - V_{TN}$=V_{OD}	$I_D = k_p[(V_{SG} - abs(V_{TP}))V_{SD} - \frac{1}{2}V_{SD}^2$ (5)	$V_{GS} < V_{TN}$ More negative $V_{DS} > V_{GS} - V_{TP}$=V_{OD}
Deep Region	$I_D = k_n[(V_{GS} - V_{TN})V_{DS}]$ (2) $r_D = \frac{V_{DS}}{I_D} = \frac{1}{k_n[(V_{GS} - V_{TN})]}$ (3)	$V_{DS} \ll V_{GS} - V_{TN}$	$r_D = \frac{V_{DS}}{I_D} = \frac{1}{k_p[(V_{SG} - abs(V_{TP})]}$ (6)	$V_{DS} \gg V_{GS} - V_{TP}$=$V_{OD}$
Saturation	$I_D = \frac{1}{2}k_n(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$ (4)	$V_{GS} > V_{TN}$ $V_{DS} > V_{GS} - V_{TN}$=V_{OD}	$I_D = \frac{1}{2}k_p(V_{GS} - abs(V_{TP})^2(1 + \lambda V_{SD})$ (7)	$V_{GS} < V_{TP}$ $V_{DS} < V_{GS} - V_{TP}$ λ Is very small
Transductance (g_M) in Saturation	$g_M = \frac{di_D}{dv_{GS}} = \frac{2I_D}{V_{GS} - V_{TN}} = \sqrt{2I_D k_n}$ (8)		$g_M = \frac{di_D}{dv_{GS}} = \frac{2I_D}{(V_{SG} - abs(V_{TP})} = \sqrt{2I_D k_P}$ (9)	

To find λ, equation (10) below was used.

$$\lambda = \frac{1}{r_D I_D} \qquad (10)$$

The circuits used to find the essential variables were Figs. 1 to 4 below.

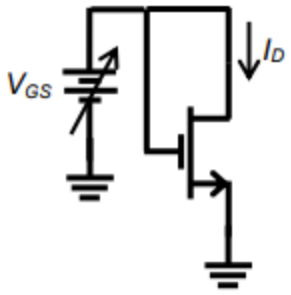

Figure 1: Diode connected circuit for NMOS.

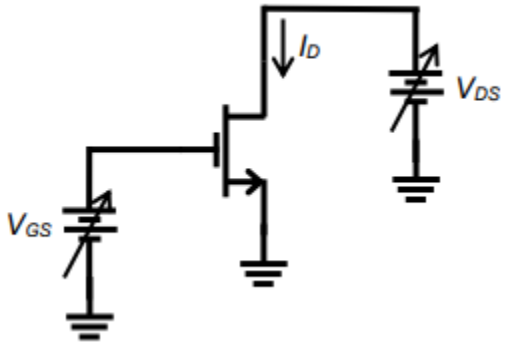

Figure 2: Circuit to obtain a family of $I_D vs\ V_{DS}$.

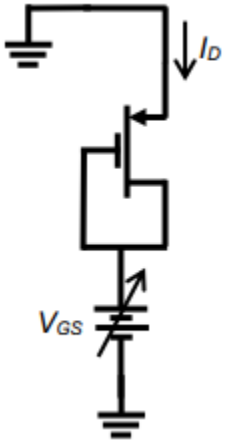

Figure 3: Diode connected circuit of PMOS.

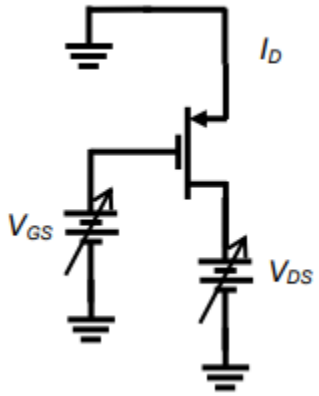

Figure 4: Circuit to obtain a family of $I_D vs\ V_{DS}$ curves.

1.3 Procedure

Part A: The $I_D vs\ V_{GS}$ curve for the BSP89 NMOS transistor using LTSPICE was obtained.

1. LTSPICE was used to create the circuit in Fig. 1. The BSP89 MOSFET was used, and the voltage source was set at 3V DC.

2. The circuit was then simulated with a linear DC sweep from 0 to 3 volts with a step size of 0.001V for V_{GS}.

3. Then the $I_D vs\ V_{GS}$ was plotted to obtain and record the threshold voltage, V_T.

Part B: The $I_D vs\ V_{DS}$ curves were obtained at multiple steps of V_{GS} for the BSP89 NMOS transistor.

1. LTSPICE was used to create the circuit in Fig. 2. The BSP89 MOSFET was used, and the voltage source was set at 3V DC.

2. The circuit was then simulated with a linear DC sweep. The first sweep was for V_{DS} from

0 to 10V with a step size of 0.001. The second sweep was for V_{GS} from 2 to 3 volts with a step size of 0.2V.

3. I_D was plotted showing six curves with a V_{GS} ranging from 2V and jumping .2V from bottom to up each curve.

Part C: The $I_D vs\ V_{GS}$ curve for the BSS84 PMOS transistor using LTSPICE was obtained.

1. LTSPICE was used to create the circuit in Fig. 3. The BSS84 MOSFET was used, and the voltage source was set at -3V DC.

2. The circuit was then simulated with a linear DC sweep from 0 to -3 volts with a step size of 0.001V for V_{GS}.

3. Then the $I_D vs\ V_{GS}$ was plotted to obtain and record the threshold voltage, $V_T = +V_{GS}$.

Part D: The $I_D vs\ V_{DS}$ curves were obtained at multiple steps of V_{GS} for the BSS84 PMOS transistor.

1. LTSPICE was used to create the circuit in Fig. 4. The BSS84 MOSFET was used, and the voltage source was set at -3V DC.

2. The circuit was then simulated with a linear DC sweep. The first sweep was for V_{DS} from

0 to -10V with a step size of 0.001. The second sweep was for V_{GS} from -3 to -4 volts with a step size of 0.2V.

3. I_D was plotted showing six curves with a V_{GS} ranging from -3V and jumping -.2V from bottom to up each curve.

Part E: The parameters from the obtained graphs were estimated.

1. For the NMOS and PMOS transistors and from the $I_D - V_{GS}$ curves, the value of

the threshold voltages were estimated noting V_{TN} >0 but V_{TP} <0.

2. The transconductance,g_M, defined at a specific current, I_D, was measured from the slope to estimate k_n from equation (8) and (9).

3. Step 2 was repeated for the PMOS transistor.

4. The channel modulation index, λ, was estimated for both transistors.

5. For the NMOS $I_D - V_{DS}$ family of curves, 6 different points on the curve were picked with three points being in the saturation region and three in the triode region then they were recorded in table 2 below in the results. Then k_n was estimated with equations (1), (4), rearranged to find k_n. Then the average k_n was calculated. Results were then commented on.

6. Step 5 was repeated for the PMOS transistor recording values in table 3 and equations (5) and (7).

1.4 Results & Analysis

Fig. 5 below shows the resulting circuit in LTSPICE of Fig. 1 with specified parameters of steps 1 and 2 of part a of the procedure, and Fig. 6 below is the corresponding plot showing $I_D vs\ V_{GS}$. V_{TN} was found to be 1.6 V, using the cursors.

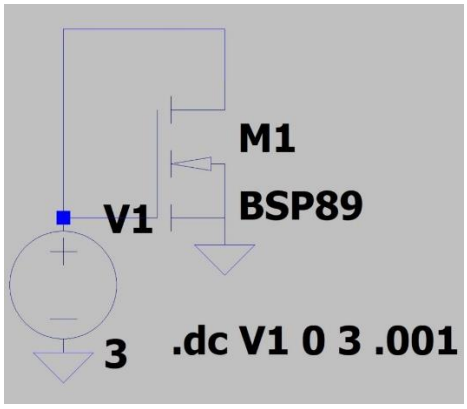

Figure 5: LTSPICE Circuit of Fig. 1 with DC sweep.

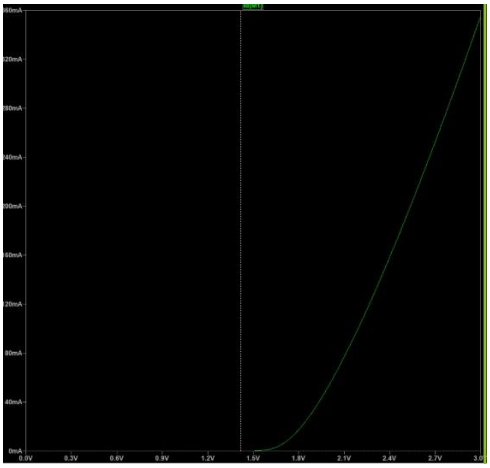

Figure 6: Plot of Fig. 5 showing $I_D vs\ V_{GS}$.

Fig.7 below shows Fig.2 in LTSPICE with the indicated specifications stated in steps 1 and 2 of part b of the procedure. Fig.8 show the family of curves of Fig. 7 with the indicated parameters of step 3 of part b of the procedure.

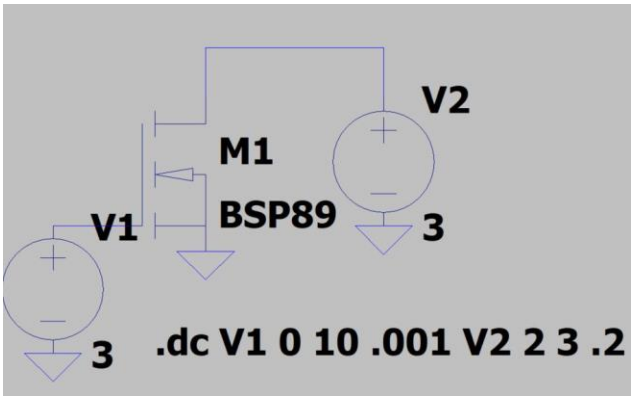

Figure 7: LTSPICE Circuit of Fig. 2 with DC sweep.

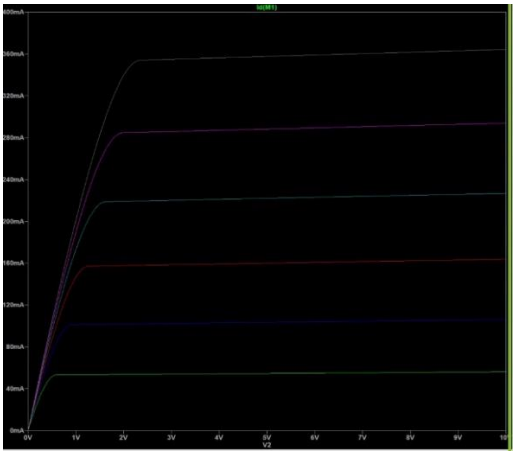

Figure 8: Plot of Fig. 7 showing $I_D vs\ V_{DS}$.

Fig. 9 shows the LTSPICE circuit of Fig.3 with the indicated parameters of steps 1 and 2 of part c of the procedure. Fig. 10 below is the corresponding plot showing $I_D vs\ V_{GS}$. V_{TP} was found to be 2 V, using the cursors.

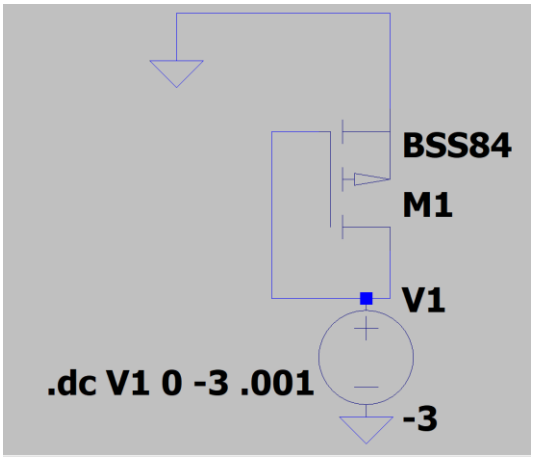

Figure 9: LTSPICE Circuit of Fig. 3 with DC sweep.

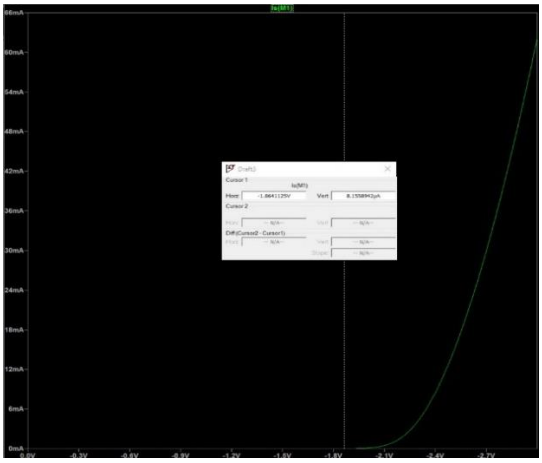

Figure 10: Plot of Fig. 9 showing $I_D vs\ V_{GS}$.

Fig.11 below shows Fig.2 in LTSPICE with the indicated specifications stated in steps 1 and 2 of part d of the procedure. Fig.12 show the family of curves of Fig. 11 with the indicated parameters of step 3 of part d of the procedure.

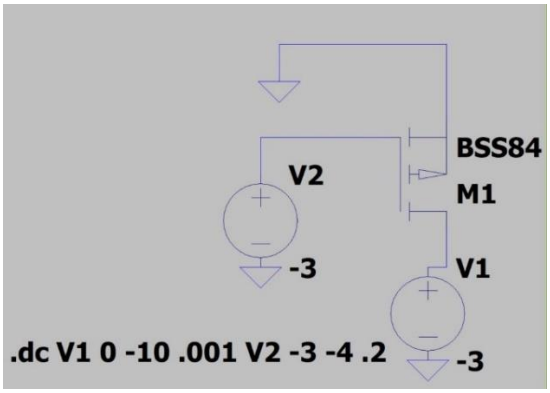

Figure 11: LTSPICE Circuit of Fig. 4 with DC sweep.

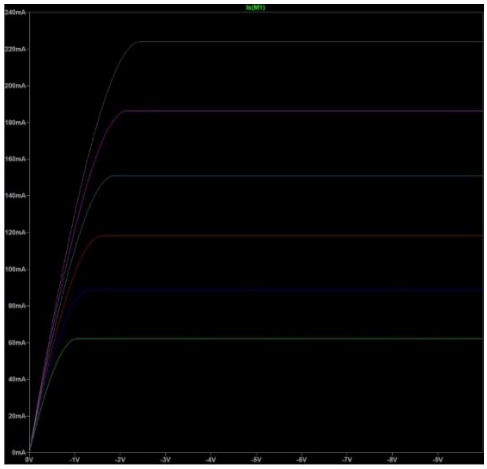

Figure 12: Plot of Fig. 11 showing $I_D vs\ V_{DS}$.

As indicated in step 2 of part e of the procedure, g_M was estimated to be .294 A/V, and using equation (8) rearranged to solve for k_n, k_n was found to be .2756 A/V^2. The points on the graph used was (2.389 V,155 mA) and (2.423 V, 165 mA) since it needed to be around 160 mA from Fig. 6.

As indicated in step 3 of part e of the procedure, g_M was estimated to be -.091 A/V, and using equation (8) rearranged to solve for k_p, k_p was found to be .138 A/V^2. The points on the graph used was (-2.64 V,25 mA) and (-2.75 V, 35 mA) since it needed to be around 30 mA from Fig. 10.

To find the channel modulator index, λ, first equation (3) was used to find r_D for the NMOS and equation (6) was used to find r_D for the PMOS since they can be translated to $r_D = \frac{1}{slope}$, where the slope is g_M. Once r_D was found to be 3086 V/uA for the NMOS and infinity for the PMOS,

then using equation (10), λ was found to be .00589 $V^{-1}$for NMOS and 0 for the PMOS. These were found using the bottom curve of Fig. 8, and 12.

Table 2 below shows the indicated values specified in step 5 of part e for NMOS and table 3 shows the indicated values specified in step 6 of part e for PMOS. For both tables, the color curve was picked in Fig. 8 and Fig. 12, the current and voltage variables were measured, the triode or saturation were labeled based on spot on the graph picked, and the k_n or k_p values were calculated. k_n was calculated using equation (1) for the points in the triode region, and equation (4) in the saturation region as well as the estimated or found variables. k_p was calculated using equation (5) for the points in the triode region and equation (7) for the saturation region as well as the estimated or found variables. These equations were rearranged to solve for k_n or k_p.

Table 2: Showing Color Curve, I_D, V_{GS}, V_{DS}, Triode/Saturation Indication, and Calculated k_n for Fig. 8.

Color Curve	I_D (mA)	V_{GS} (V)	V_{DS}(V)	Triode/Saturation (T,S)	k_n (A/V^2)
Pink	51.64	2.8	.25	T	.1922
Red	45.94	2.4	.25	T	.272
Green	32.7	2	.25	T	.486
Pink	287	2.8	4	S	.3894
Red	159.29	2.4	4	S	.4863
Green	54.33	2	4	S	.6635
Average k_n= .4131 A/V^2					

Table 3: Showing Color Curve, I_D, V_{GS}, V_{DS}, Triode/Saturation Indication, and Calculated k_p for Fig. 12.

Color Curve	I_D (mA)	$abs(V_{GS}) = V_{SG}$ (V)	$abs(V_{DS}) = V_{SD}$(V)	Triode/Saturation (T,S)	k_p (A/V^2)
Green	42.575	-3	.5	T	.1135
Red	56.264	-3.4	.5	T	.0978
Pink	65.77	-3.8	.5	T	.0849
Green	62.127	-3	4	S	.124
Red	118.21	-3.4	4	S	.121
Pink	186.25	-3.8	4	S	.115
Average k_p= .1094 A/V^2					

The error between the k_n found in Fig. 6 and the average k_n shown in table 2 was 49.9%. This is due to k_n changing between the 6 points, ideally k_n should not be changing at all. The error between the k_p found in Fig. 10 and the average k_p shown in table 3 was 20.72%. This is due to k_p changing between the 6 points, ideally k_p should not be changing at all.

1.5 Conclusion

To conclude this experiment, the error between the k values was significant between the plots and the tables. This is due to k fluctuating between the 6 points picked, this should not happen.

Experiment #2 FET as Voltage Controlled Resistor

2.1 Purpose

The purpose of this experiment was to plot the output voltage versus the VGS and find how the transistor in the deep triode region acts as a voltage controlled resistance by varying VGS.

2.2 Theoretical Background

Experiment 1 allowed the observation between I_D and V_{DS}, the conclude that it is a linear relationship in the deep triode region. This means that the drain-source channel of the transistor acts as a voltage-controlled resistor that depends on V_{GS}. The equations to express the current source and the drain resistance can be found in table 1, equations (1), (2), and (3). This then concludes that the transistor in the deep triode region acts as a voltage-controlled resistor that is controlled by varying V_{GS}, and the transistor can be replaced with the variable resistance as shown in Fig. 13 below.

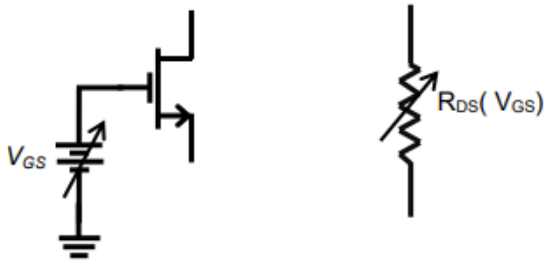

Figure 13: NMOS as a variable resistance in the deep triode region.

Fig. 14 below shows the figure actually to be plotted and drawn in LTSPICE to produce r_{DS}, V_o, and V_{GS}values required in the following procedure.

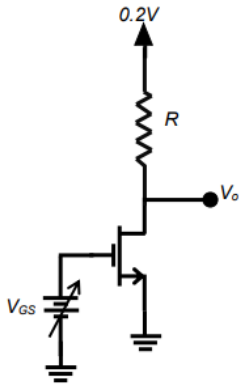

Figure 14: NMOS as a variable resistance in a voltage divider circuit.

For the pre-lab, the chosen V_{GS} was 2.25 V, then using equation (3), the r_{DS} was calculated to be 5.59 Ω. Using the voltage divider between V_o=.02 and $V_{CC} = .2\ V$, the resulting R was found to be 50.37 Ω. Then when $V_o = .1\ V$, $r_{DS} = R = 50.37\ \Omega$ and the KVL to find V_{GS} was 1.674 V.

2.3 Procedure

1. LTSPICE was used to build the circuit of Figure 14 with the designed values and BSP89 NMOS.

2. A linear DC Sweep was varied for V_{GS} from 0 to 5V with a step size of 0.0001. Then V_o vs. V_{GS} was plotted. The cursors were then used to find V_{GS} at V_o =0.1V and 0.02V. Then the cursors were used to find V_o at the calculated V_{GS} values, from the pre-lab.

2.4 Results & Analysis

Fig. 15 shows the LTSPICE circuit shown in Fig. 14 with specified parameters from steps 1 and 2 of the procedure. Fig. 16 is the resulting V_o vs. V_{GS} graph from Fig. 15.

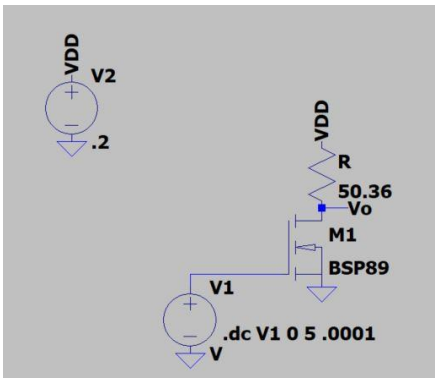

Figure 15: LTSPICE Circuit of Fig. 14.

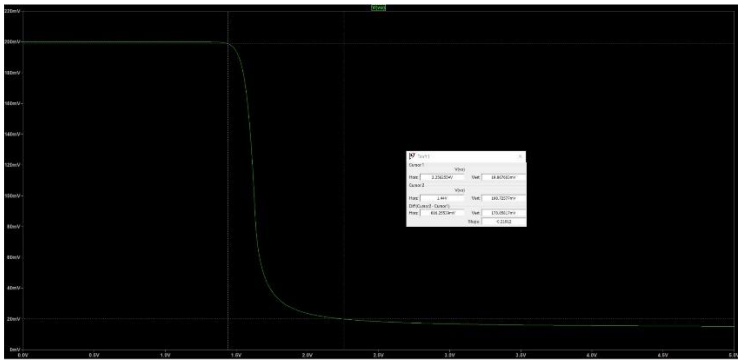

Figure 16: Plot of Fig.15 showing V_o vs. V_{GS}.

The resulting values for the specified voltages is as follows in table 4 below.

Table 4: V_o, V_{GS}.

V_o (V)	V_{GS} (V)
.02	2.24
.1	1.624
.019926	2.25
.0553	1.674

The errors between the calculated and traced values varies between .37% error for output voltage of .02 V, 44.7% for output voltage of .1 V, 2.98% for V_{GS} of 1.674 V, and 4.44% for V_{GS} of 2.25 V.

2.5 Conclusion

To conclude this experiment, the expected voltages did not output much error between the calculated and the measured except when the output voltage was supposed to be at .1 V. This is due to the transistor having unique settings in LTSPICE.

Experiment #3 MOSFET as Buffer Amplifier

3.1 Purpose

The purpose of this experiment was to investigate the large signal transfer characteristics from the input to the output of the amplifier by varying the input voltage from 0 to VDD.

3.2 Theoretical Background

For this experiment, a buffer amplifier was used. A buffer amplifier is used when the input signal source is not capable of supplying the load with large current causing power. This occurs while also maintaining the same voltage level as the input. There are many practical situations in which this occurs in electronics such as in sending am audio signal to a speaker, where the output voltage is desired to be equal to the input voltage but the current, or power, needs to be much larger than what the input signal source can handle. Since the current greatly increases and voltage remains the same, ideally the output power would also greatly increase. The circuit of Fig. 17 below is called a Buffer Amplifier (or Common Drain amplifier), which is a type of power amplifier.

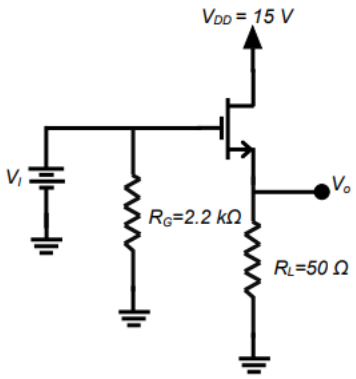

Figure 17: NMOS Buffer Amplifier.

For the prelab, the range of power for the input and output voltage was done by using equations (11) and (12) below. The resulting input power was determined to be between 0 W and 100 mW, the resulting output power was determined to be between 0 and 4.5 W. Assumptions made was that the voltage range would be between 0 and 15 V.

$$P_i = \frac{V_i^2}{R_G} \qquad (11)$$

$$P_o = \frac{V_o^2}{R_L} \qquad (12)$$

3.3 Procedure

1. LTSPICE was used to create Fig. 17 with IRF510 NMOS power transistor and a DC analysis with a varying V_i from 0 V to 25 V with a step size of 0.001.

2. The voltage transfer curve (V_o vs. V_i) was plotted to determine and record the threshold voltage of the transistor.

3. Using the cursor and starting from zero all the way to 25 V, V_o was recorded on a table in excel at increments of 1 V for V_i. At each recorded V_i value, the P_i was calculated using equation (11) and the P_o was determined using equation (12). Then the region of operation of the transistor was determined.

4. Then P_o vs P_i was plotted.

3.4 Results & Analysis

Fig. 18 below shows the created circuit done in LTSPICE with specified parameters from step 1 in the procedure. Fig. 19 below shows the resulting voltage plot with red marks indicating the measured 1V increments based on the input voltage. Threshold voltage was determined to be 3.8 V.

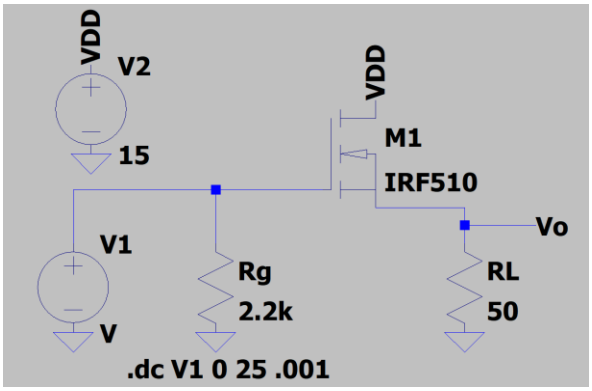

Figure 18: LTSPICE Circuit of Fig. 17.

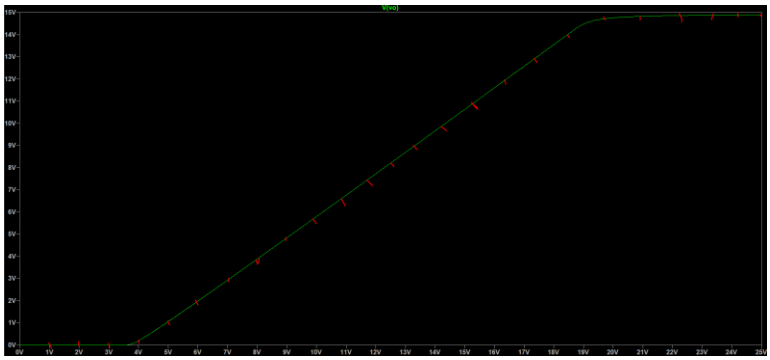

Figure 19: Plot of Fig. 18 showing V_o vs. V_I.

Table 5 below shows the input voltage in increments of 1 V from 0 V to 25 V, the output voltage associated with each input voltage, the input power determined using equation (11), and the output power determined using equation (12).

Table 5: Showing V_I, V_o, P_I, and P_o.

V_I (V)	V_o (V)	P_I (W)	P_o (W)
0	2.350E-06	0.000	1.105E-13
1	2.350E-06	0.000	1.105E-13
2	2.350E-06	0.002	1.105E-13
3	4.966E-05	0.004	4.932E-11
4	0.194	0.007	7.543E-04
5	1.051	0.011	2.209E-02
6	1.976	0.016	7.809E-02
7	2.920	0.022	0.171
8	3.872	0.029	0.300
9	4.830	0.037	0.467
10	5.792	0.045	0.671
11	6.756	0.055	0.913
12	7.735	0.065	1.197
13	8.676	0.077	1.505
14	9.658	0.089	1.866
15	10.621	0.102	2.256
16	11.605	0.116	2.694
17	12.560	0.131	3.155
18	13.545	0.147	3.669
19	14.475	0.164	4.191
20	14.757	0.182	4.355
21	14.825	0.200	4.396
22	14.855	0.220	4.413
23	14.871	0.240	4.423
24	14.881	0.262	4.429
25	14.888	0.284	4.433

Based on table 5, the input power overshot the max by 184% due to the LTSPICE setting for the transistor. The output voltage was within range of the expected minimum and maximum, so there was no error for the output power. Fig. 20 shows the resulting graph between the input and output power. The triode range was estimated to be between 0 and .03 V. The saturation zone was estimated to be between .03 V and .164 V and the cutoff range was estimated to be between .164 V to .284 V or infinity. These ranges are based on the output voltage.

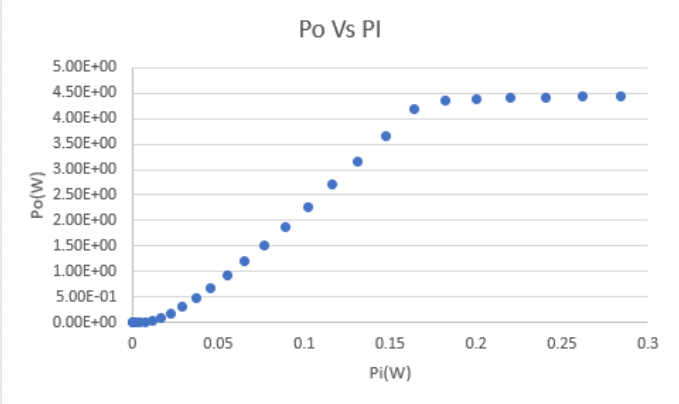

Figure 20: Excel calculated Power Plot showing P_o vs. P_I.

3.5 Conclusion

What is the conclusion of this experiment.

Based on this experiment, it can be concluded that the buffer amplifier does significantly increase the power as proven theoretically and through LTSPICE. The expected input power range was overshot by 184% to be 284 mV, simply due to the settings of LTSPICE for the transistor used.

Appendix

Appendix A: Components Packages and Pins Assignments

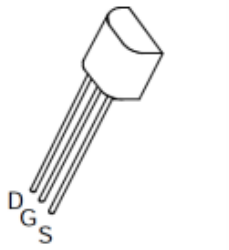

Figure A1. TO-92 Package for ZVN2210A and ZVP2110A and their pin assignments.

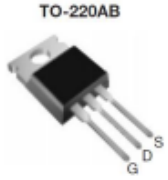

Figure A2. TO-220AB Package for IRF510 power NMOS transistor.

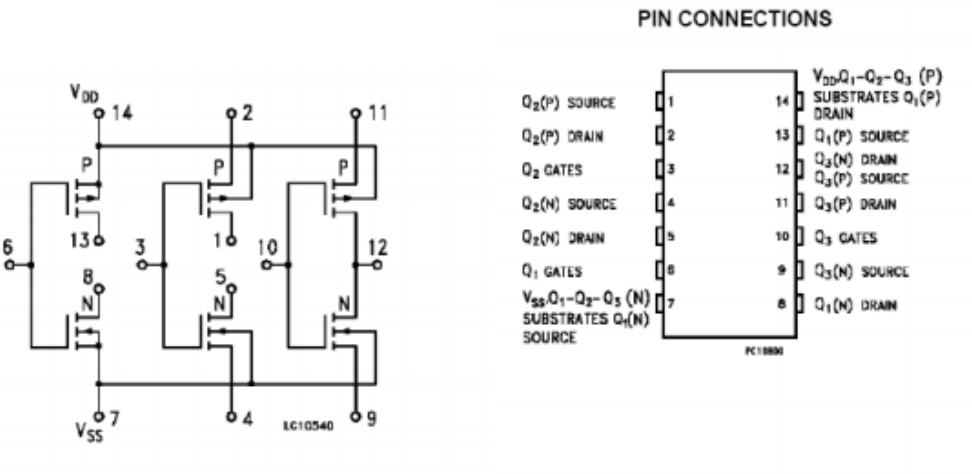

Figure A3. Package and pin assignment for CD4007 complementary dual CMOS transistors.

Appendix B

Lab 7 Checklist

Name: ~~Sarah~~ Rock

Lab title and introduction

- Lab title, your name, date, and lab partner.
- Brief introduction (two or three sentences) explaining the purpose of this lab.

I. MOSFET Characteristics (50 pts total)

1. Printout of measured NMOS I-V curves
2. Printout/sketch of measured PMOS I-V curves
3. Calculated values of V_T, K_n, λ, and g_m for the NMOS
4. Calculated values of V_T, K_P, λ, and g_m for the PMOS

_____ 5. **DEMO:** Have a TA initial this sheet, indicating that he/she has observed your calculations of the NMOS parameters.

II. Voltage Controlled Resistor (25 pts total)

1. Circuit diagram.
2. Explanation of how you computed R_{DS} for a given V_{GS}.
3. Designed and measured values of R.
4. Estimated and measured values of V_o at 10% and 50% of V_{DD}.
5. Estimated and measured values of V_{GS} at 10% and 50% of V_{DD}.

_____ 6. **DEMO**: Have a TA initial this sheet, indicating that they he/she has observed your circuit's operation.

III. MOSFET Buffer Amplifier (25 pts total)

1. Circuit diagram used to measure voltage transfer characteristic with measured values for R_G and R_L.
2. Determine the threshold voltage of the IRF510 transistor.
3. Plot of voltage transfer characteristics, V_o vs. V_I.
4. Plot of output vs. input power transfer characteristics.

_____ 5. **DEMO**: Have a TA initial this sheet, indicating that he/she has observed your circuit's operation.

- Show TA your plot of the system power transfer characteristic.