Washington State University

School of Electrical Engineering and Computer Science

EE 352 Electrical Engineering Laboratory

Lab # 10

BJT Amplifier circuits

Name: Sarah Rock

Partner: Zach Nett, Isobel Beatz

Due Date: 04/19/21

Lab Overview

The purpose of this lab is to continue with what was being done in Lab 9 where BJT characteristics were being obtained. For this lab, the common emitter amplifier with a set of given specifications was designed and studied.

Experiment #1 Single Stage Common Emitter Amplifier

1.1 Purpose

The purpose of this experiment was to design a common emitter BJT amplifier as shown in Fig. 1 using a 2N3904 npn transistor with a list of specifications.

1.2 Theoretical Background

The Common Collector Amplifier is another type of bipolar junction transistor, (BJT) configuration where the input signal is applied to the base terminal and the output signal taken from the emitter terminal. Thus, the collector terminal is common to both the input and output circuits. This type of configuration is called Common Collector, (CC) because the collector terminal is effectively "grounded" or "earthed" through the power supply. The CC and the common emitter (CE) are opposite in configuration where the load resistor is moved from the collector terminal (R_C)to the emitter terminal (R_E). The common collector is typically where a high impedance input source needs to be connected to a low impedance output load requiring a high current gain. In Fig. 1 below the R_1 and R_2 resistors form a simple voltage divider network to bias the NPN transistor with a light load that allows the base voltage to be easily calculated shown in equation (1) below.

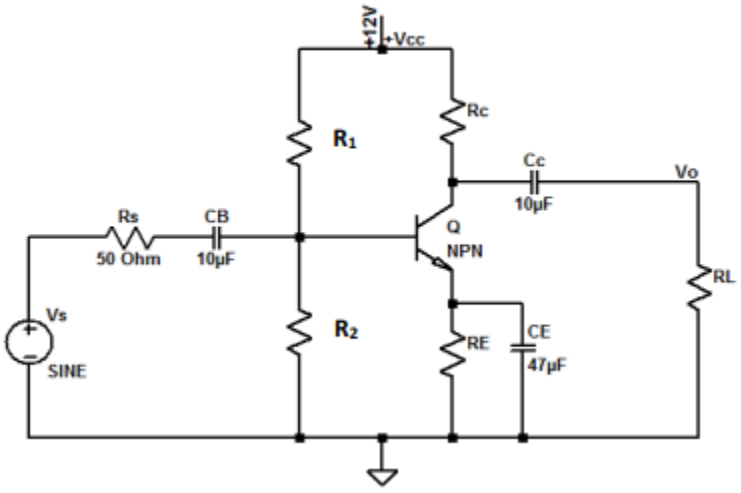

Figure 1: Single stage Common Emitter Amplifier.

$$V_{BB} = \frac{R_2}{R_1+R_2} V_{CC} \qquad (1)$$

When the collector terminal of the transistor is connected directly to VCC and there is no collector resistance, (R_C = 0) any collector current will generate a voltage drop across the emitter

resistor R_E. Ideally, we would want the DC voltage drop across R_E to be equal to half the supply voltage, VCC to make the transistors quiescent output voltage sit somewhere in the middle of the characteristics curves allowing for a maximum unclipped output signal. Thus, the choice of $R_E$depends greatly on I_B and the transistors current gain Beta, β. As the base-emitter pn-junction is forward biased, base current flows through the junction to the emitter causing a much larger collector current, I_C to flow. Thus, the emitter current is a combination of base current and collector current is expressed as: $I_E = I_B + I_C$. The base current is extremely small compared to the collector current which concludes that the emitter current is therefore approximately equal to the collector current. With the (CE) amplifier configuration, the input signal goes through a singular forward biased pn-junction to the transistor's base terminal where the amplifiers output signal is taken from the emitter terminal. This allows any input signal applied to the base to pass directly through the junction to the emitter, meaning the output signal present at the emitter is in-phase with the applied input signal at the base. The base emitter voltage signal in this case is .7 V which allows for the input and output voltage to be in the same phase. Due to the forward bias, the thermal voltage is 25mV.

The base current which flows through this internal base-emitter junction resistance also flows out and through the externally connected emitter resistor, R_E, usually in the kilohms (kΩ) range, which means the magnitude of the amplifiers output voltage is less than its input voltage.

For the prelab, the objective was to design a single stage common emitter amplifier by choosing appropriate values to meet the gain, input, and output requirements. The given values and the specified requirements are shown in Table 1 below.

Table 1: List of Variables and their Specifications for the Circuit shown in Fig. 1.

Variables	Specifications			
Resistances	$R_L = 47\ k\Omega$	$R_{in} > 1.2\ k\Omega$	$R_1 = 2R_2$	$R_S = 50\ \Omega$
Gain/ constants	$G_v = -85 \pm 20\%$	$\lambda = .01\text{V}^{-1}$	$k_n \approx .1\ A/V^2$	$\beta = 100$, $\alpha = \frac{100}{101}$
Voltages	$V_{CC} = 12\ V$	$V_T \approx 25\ mV$	$V_A = 100\ V$	$V_{BB} = \frac{1}{3}V_{CC} = 4\ V > V_T$
Voltages	$V_{BE} = .7\ V$			
Capacitors	$C_B =$ 10 μF	$C_E =$ 47 μF	$C_C =$ 10 μF	
Current	$I_C = \frac{V_{CC}}{3}$	For R_1, R_2: $\frac{I_E}{10}$		

To design a successful circuit of Fig. 1, R_1 was chosen to be 300 kΩ and R_2 was chosen to be 150 kΩ. Using equation (1), and the specifications indicated in table 1, V_{CC} was proved to be 12 V. Using equation (2) below, R_B was found to be 100 kΩ. Then choosing R_E to be 30 kΩ and equation (3) below, I_E was found to be 106 μA. Using equation (4), I_C was found to be 105.4 μA. Then using equation (5) the gain (g_m) was found to be 4.2 mV/A. Using equation (6), r_π was found to be 23.7 kΩ. To find, the input resistance R_i, equation (7) was used to find that it was 19.167 kΩ. Using equation (8), r_o was found to be 948.8 kΩ. The voltage gain ($A_v = G_v$) equation, equation (9), was then used to find R_o which was 20.21 kΩ. Lastly, R_C was then determined using equation (10) to be 36.8 kΩ.

$$R_B = R_1 II R_2 \quad (2)$$

$$I_E = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta+1} + R_E} \quad (3)$$

$$I_C = \alpha I_E \quad (4)$$

$$g_m = \frac{I_C}{V_T} \quad (5)$$

$$r_\pi = \frac{\beta}{g_m} \quad (6)$$

$$R_i = R_B II r_\pi = \frac{|V_b|}{|i_s|} \quad (7)$$

$$r_o = \frac{V_A}{I_C} \quad (8)$$

$$A_v = -g_m R_o \left(\frac{R_i}{R_i + R_S}\right) = -\frac{V_{op-p}}{V_{ip-p}} \quad (9)$$

$$R_o = R_o \,||R_L||r_o \quad (10)$$

Once these values were all chosen or calculated or given, the inputted into the circuit for Fig. 1 in LTSPICE. The last part of the experiment was to evaluate the Fig. 1 with the component shown in Fig. 2 below to find the gain and input resistance with the added emitter resistance.

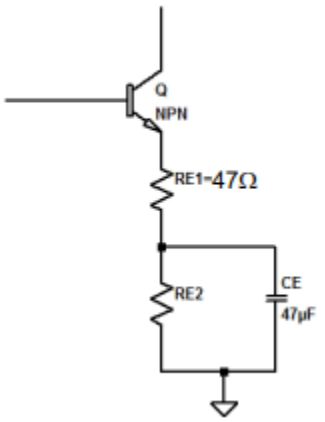

Figure 2: Un-bypassed Emitter Resistance Circuit of a BJT Common Emitter Amplifier.

1.3 Procedure

1. The circuit given in Fig. 1 was simulated using LTSPICE with Q2N3904.

2. Then the DC bias points was validated with no AC signal applied, and the DC operating point was run to determine the DC bias point of the transistor to then compare the DC values to the design values and to estimate the value of gm from the prelab measurements.

3. The gain at 20 kHz was then validated using Transient analysis with a 20 mV peak-to-peak, 20 kHz sinusoidal input signal at the input. The simulation stop time was set at 500 µs with time step of .5 µs. The output voltage across the load was measured and the mid-band voltage gain was calculated to meet the specification.

4. Next, the input resistance was measured by finding the peak-to-peak values of the base voltage and the peak-to-peak of the current across R_S.

5. Then the clipping voltages at the collector were found by setting the frequency to be 20 kHz sinusoidal signal and increasing the input level voltage to 1V, then measuring and recording this voltage at the collector and recording the and minimum voltage swing.

6. The frequency response was then obtained by using LTSPICE to apply 1 AC voltage for AC sweep to then determine the low cutoff frequency f_L and the high cutoff frequency f_H.These were 3 dB away from the gain at 20 kHz.

7. Lastly, the gain and input resistance were determined with the common emitter having added resistance in the emitter as shown in Fig. 2. The RE1 = 47 Ω and RE2=RE-47Ω with a 20 kHz sinewave.

1.4 Results & Analysis

Fig. 3 below shows the circuit of Fig. 1 with no AC signal applied. The reason why all components with capacitors are cut off is because in the DC form, the capacitors go to zero which leaves the remaining components shown in Fig. 3. When running the operating point analysis, the following values found were $V_{BB} = 3.96411\ V$, $I_C = 111.857$ µA, $V_{CC} = 12\ V$, and $V_C = 7.88368\ V$. There respective errors between the experimental and calculated values were .9%, 6.13%, 0%, and 1.454%. Using equation (5), the $g_m$of the operational analysis was found to be 4.47 mA/V which was a 6.43% error from the calculated 4.2 mA/V value.

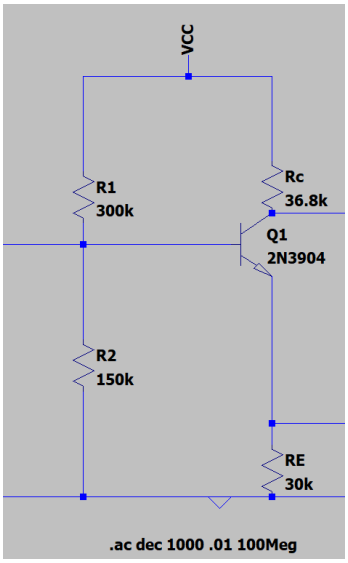

Figure 3: DC Circuit of Fig. 1 showing active circuit when Capacitors=0.

Fig. 4 shows the circuit of Fig. 1 with the parameters specified in step 3 of the procedure. Fig. 5 and 6 are the resulting plots of Fig. 4 showing the output voltage in Fig. 5, and the base voltage and signal current in Fig. 6. Using equation (9), and the input peak-to-peak voltage value of 20 mV and the output peak-to-peak voltage value of 1.7826 V, the midband gain was found to be -89.13 V/V which is within the midband gain specification with a 4.86% error.

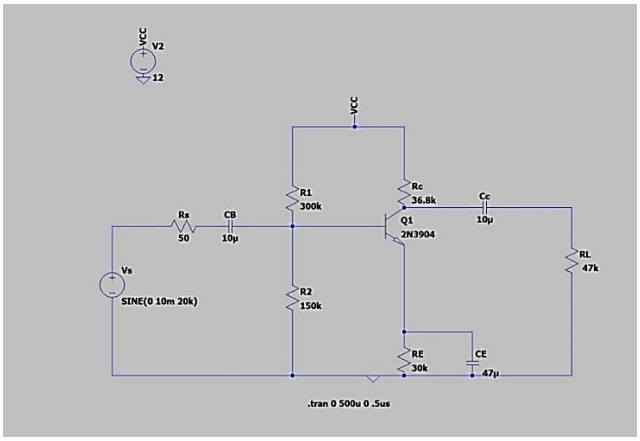

Figure 4: AC Circuit with Sine Input Voltage 20 mV_{P-P}.

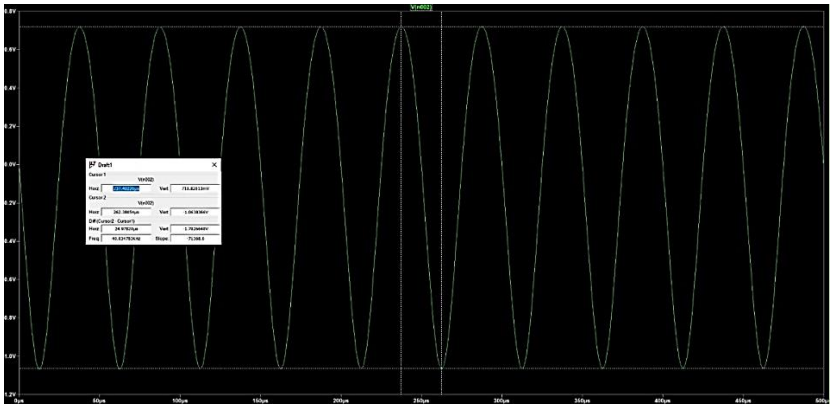

Figure 5: Output Voltage used to find G_v.

To calculate the input resistance, the peak-to-peak values of V_b and i_s were found to be 19.905 mV and 730.78 nA, respectively. Then using equation (7), R_i was found to be 27.238 kΩ which is a 42.11% error from the calculated value in the prelab. The reason for this error is because in LTSPICE, they use a beta of 300 and the calculations use a beta of 100.

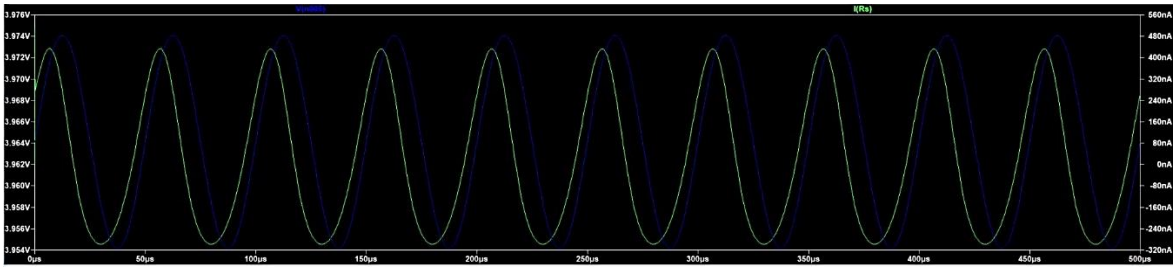

Figure 6: Sinewaves of V_b and i_s to find R_i.

Fig. 7 below is the circuit shown in Fig.4 with an input voltage amplitude of 1 V_{0-P}. This was plotted to show the collector voltage clipping at $V_{Cmax} = 10.196\ V$ and $V_{Cmin} = 3.405\ V$ as shown in Fig. 8. The reason for this clipping is because the circuit is large enough to leave the active region and enter the saturation region.

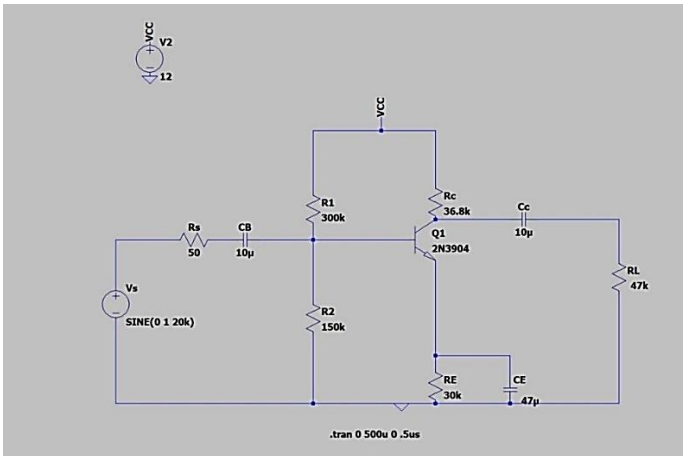

Figure 7: Fig. 4 Circuit with 1 V_{0-P}.

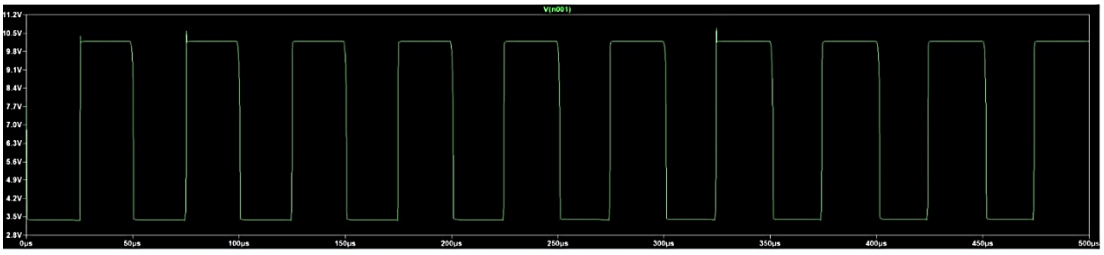

Figure 8: Fig. 4 plot showing the collector voltage (V_C) clipped.

Fig. 9 shows the circuit in Fig. 4 with an AC input voltage of 1 V, as specified in step 6 of the procedure. Fig. 10 is the resulting plot of Fig. 9 used to find the midband gain and cutoff frequency. The range was increased to 1MHz to show both the low and high cutoff frequencies. Using the cursors, the gain was measured to be 38.85 dB or 87.6 V/V at 20 kHz, the low cutoff frequency was measured to be 14.79 Hz and the high cutoff frequency was measured to be 2.7416 MHz. The gain was 3.05% error from the ideal 85 V/V value, which is within the 20% error.

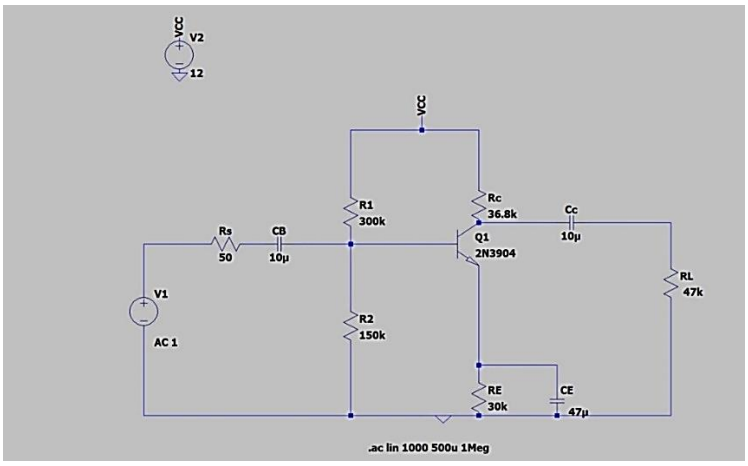

Figure 9: Fig. 4 Circuit with 1 AC voltage and AC sweep.

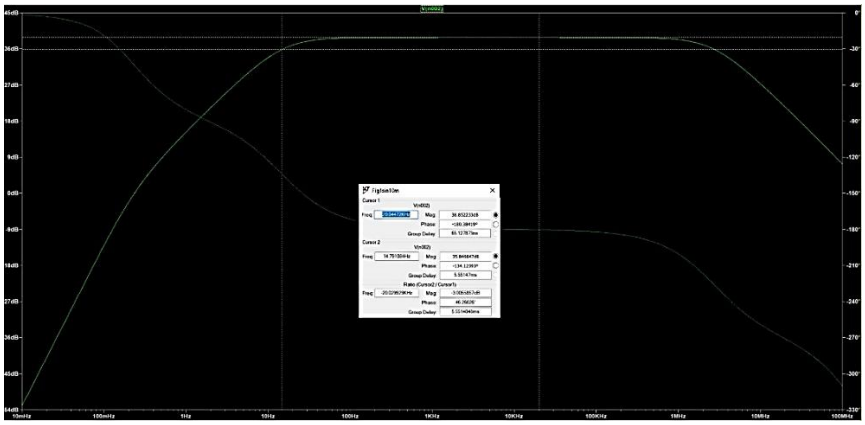

Figure 10: Fig. 9 plot showing measured midband gain and cutoff frequencies.

Fig. 11 shows the circuit of Fig.4 with the added emitter resistor as directed in Fig. 2 with the RE1 and RE2 specifications stated in step 7 of the procedure. Fig. 12 and 13 are the resulting plots of Fig. 11 showing the output voltage in Fig. 12, and the base voltage and signal current in Fig. 13. Using equation (9), and the input peak-to-peak voltage value of 20 mV and the output peak-to-peak voltage value of 1.46 V, the midband voltage gain was found to be 73.1475 V/V which is within the midband gain specification with a 13.9% error. To calculate the input resistance, the peak-to-peak values of V_b and i_s were found to be 19.93 mV and 620.9 nA, respectively. Then using equation (7), R_i was found to be 32.098 kΩ which is a 67.46% error from the calculated value in the prelab. The reason for these errors is because in LTSPICE, they use a beta of 300 and the calculations use a beta of 100. Also, when a resistor is added to the emitter, it causes the gain to drop and the resistance to increase.

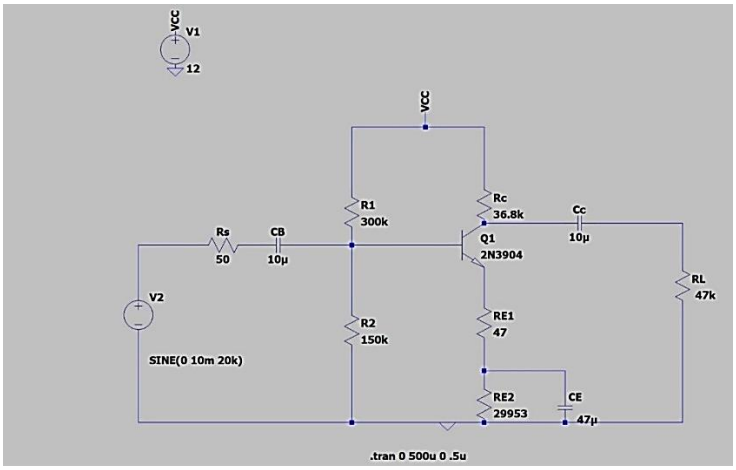

Figure 11: Fig. 4 Circuit with Fig. 2 added Emitter Resistor.

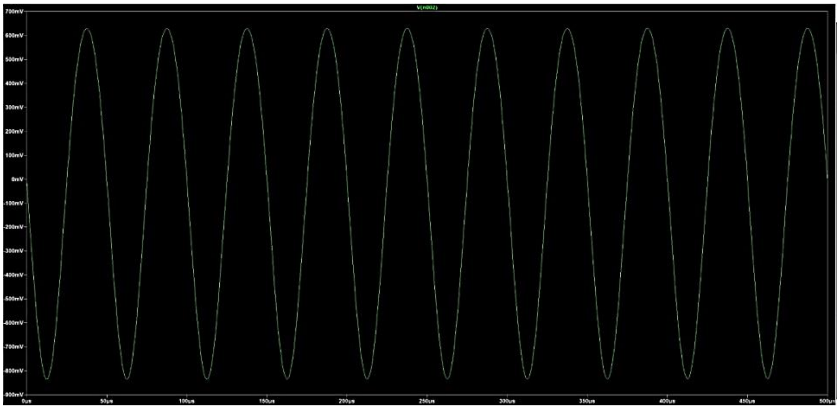

Figure 12: Fig.11 Output Voltage Plot used to find G_v.

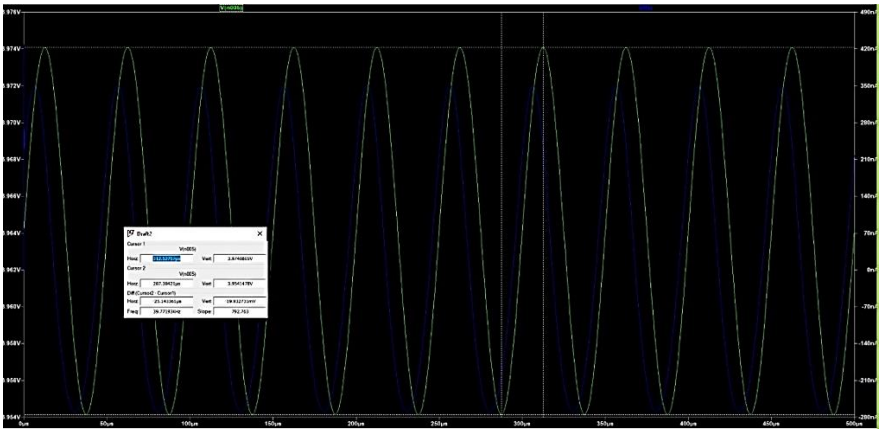

Figure 13: Fig. 11 plot showing Sinewaves of V_b and i_s to find R_i.

1.5 Conclusion

To conclude this experiment, the measured and calculated values all differed due to beta being 100 in the calculations and 300 in LTSPICE. This experiment is deemed successful due to all the values, both in the prelab and in the experiment, meeting the specifications shown in Table 1.

Appendix

Appendix A:

No checklist provided.