Washington State University School of Electrical Engineering and Computer Science

EE 352 Electrical Engineering Laboratory

Lab # 4

Non-Ideal Operational Amplifier Behavior

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Lab Overview

The main objective of this lab was to be exposed to the practical aspects of operational amplifiers that impose limitations to their behavior. These being obtaining key information about OP-27 from the data sheet, designing op-amps with specific gains and determine bandwidth based on the constant gain-bandwidth product. Another is determining experimentally the slew rate of the OP27 as well as the input offset voltage then comparing these values to the ones on the data sheet. Gaining understanding of the importance of the inverting and non-inverting inputs to be used as unstable Schmitt trigger circuit with positive feedback will be achieved. Lastly, determining experimentally the differential open loop gain and the common mode gain to then determine the common mode rejection ratio for OP27 then comparing it to the data sheet.

Experiment #1 The effects of the open-loop gain bandwidth product on op-amp circuits

1.1 Purpose

The purpose of experiment one was to experimentally validate the gain- bandwidth product for the non-inverting configuration using the OP27 op-amp. This was done by designing three different gains for the same op-amp circuit then experimentally determining their corresponding 3dB corner frequencies using LTSPICE.

1.2 Theoretical Background

It is important to know that the open loop gain of a practical op-amp has a finite gain that depends on frequency where it behaves like a first-order system with a finite open loop gain (A_0) and a low cutoff frequency (f_b). This shows that the open loop gain can be expressed as

$$A(jf) = \frac{A_0}{1 + j\left(\frac{f}{f_b}\right)} \qquad (1)$$

When manipulated, equation (1) can be expressed as

$$A(jf) = \frac{A_0 f_b}{f_b + jf} \qquad (2)$$

To assure stability of the closed loop amplifier at unity gain, the op-amp must intentionally be built with a very small f_b. f_b is typically set to be less than 10Hz. If f_b is significantly smaller than f, then equation (3) can be used.

$$A(jf) \approx \frac{A_0 f_b}{jf} = \frac{f_t}{jf} \qquad (3)$$

For (3), there are two important observations, the first being that when $f = A_0 f_b$, the open loop gain is 1, the second is that the gain bandwidth is constant. For both observations, $f_t = A_0 f_b$.To investigate the effect of the open loop gain on the non-inverting configuration can be found using equation (4) which is the ideal overall gain of the non-inverting configuration.

$$\mathrm{G_{ideal}} = 1 + \frac{\mathrm{R_2}}{\mathrm{R_1}} \qquad (4)$$

Then by forcing equation (3) for the open loop gain, the overall gain for the non-inverting amplifier is given in equation (5). f_o is provided as the 3dB corner frequency.

$$G(jf) = \frac{1+\frac{R_2}{R_1}}{1+\frac{jf}{f_o}} = \frac{G_{ideal}}{1+\frac{jf}{f_o}} \qquad (5)$$

To use f_o to find f_t, equation (6) is used.

$$\left(1+\frac{R_2}{R_1}\right) f_o = (G_{ideal})(f_o) \approx f_t = constant \qquad (6)$$

For the prelab, the OP27 datasheet provided the minimum and typical gain-bandwidth product as $f_t(min) = 5\ MHz\ and\ f_t(typical) = 8\ MHz$. For the op-amp circuit shown in Fig. 1, R1=1 kΩ, the ideal gains are given as 11 V/V, 48 V/V, and 101 V/V. So when plugging in the retrospective gain values and the value of R1 into equation (4), the R2 values are shown to be 10 kΩ, 47 kΩ, and 100 kΩ. Then using equation (6) to find f_o for both the minimum and the typical are shown in table 1 below.

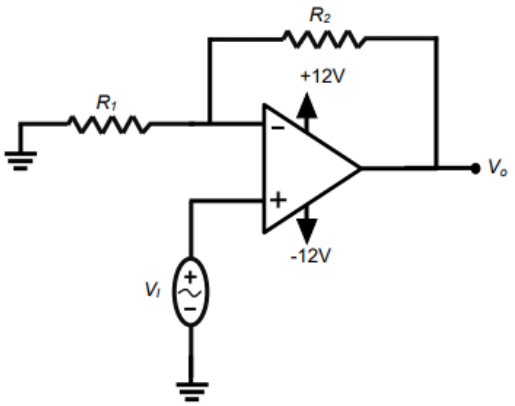

Figure 1: Non-inverting configuration of the op-amp

Table 1: Prelab Calculations for b and c

$G_{ideal}\ (\frac{V}{V})$	R_2 (kΩ)	$f_0(min)$ (kHz)	$f_0(typical)$ (kHz)
11	10	454	727
48	47	104.2	166.7
101	100	49.5	79.2

1.3 Procedure

1. Using LTSPICE, Fig. 1 was constructed using OP27 with the values found in table 1 for the gain of +11 V/V with a voltage source of 1V AC.
2. An AC Analysis was inserted with a sweep of a frequency ranging from 10 Hz to 10MEG Hz on a decade scale, with 1000 points per decade.

3. Once the circuit was constructed, the AC gain (Vo/VI) was plotted to measure the DC Gain in dB and convert to V/V, with the low frequency gain at 100 Hz. Then using Cursor 1 & 2 the 3dB corner frequency was measured to calculate the gain bandwidth product.
4. Repeated steps 1-3 for the gain of +48V/V
5. Repeated steps 1-3 for the gain of +101V/V
6. The results from 3-5 of the gain bandwidth products was compared with datasheet values.

1.4 Results & Analysis

Using LTSPICE, the circuit in Fig.1 was built using the +11V/V values connected in table 1 and the AC analysis with parameters stated in step 2 of the procedure. The product of this is shown in Fig. 2.

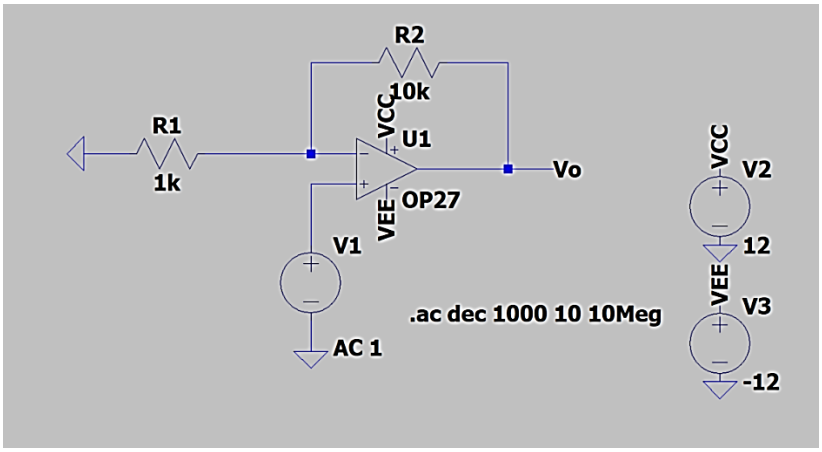

Figure 2: +11V/V Gain Circuit with AC analysis

Using the circuit shown in Fig. 2, [Vout/Vin] was graphed and the result is shown in Fig. 3. Using Cursor 1 and 2, the gain at 100 Hz was traced to be 20.82 dB. Then by subtracting 3 dB from the 20.82, the 3dB cutoff frequency was found to be 960.44 Hz. Using equation (6) with the ideal gain of +11V/V and the 3dB cutoff frequency of 960.44 Hz, the calculated gain bandwidth product (f_t) was found to be 10.5 MHz. This is a 31.25% error from the theoretical typical value of 8 MHz. The reason for this deviation is because the 8 MHz is based on averaging the f_t value of a million op-amps, and the gain equation uses approximate values, resulting in high potential error when comparing to one op-amp circuit.

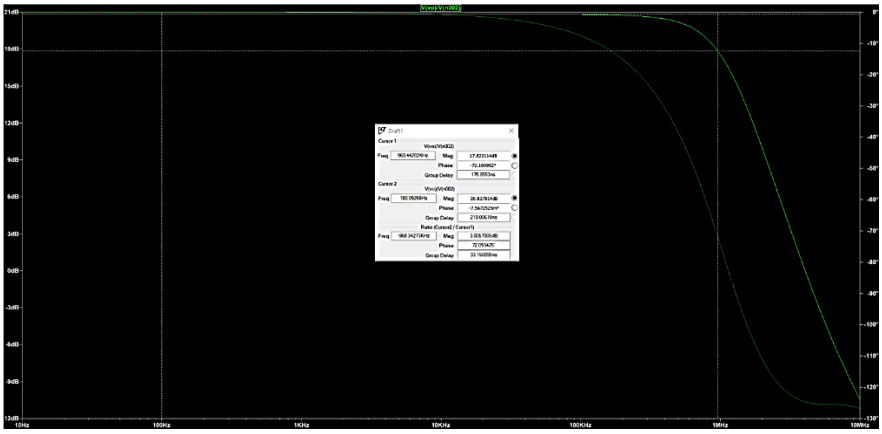

Figure 3: [Vout/Vin] plot for the Circuit in Fig. 2.

Fig. 4 to 7 are a repetition of Fig. 2 and Fig. 3 with Fig. 4 and Fig.6 being circuits with set ideal gains and Fig. 5 and Fig.7 being their respective [Vout/Vin] plots. The difference between each iteration is that Fig. 4 and 5 have the ideal gain of +48 V/V with associated values identified in table 1. While Fig.6 and 7 have the ideal gain of +101 V/V with associated values identified in table 1. Using the same technique as with the +11 V/V, the gain at 100 Hz for the +48 ideal gain was 33.62 dB and the f_t was 8.945 MHz. For the ideal gain of +101 V/V, the gain at 100 Hz was 40.08 dB and the f_t was 8.567 MHz. The f_t error for +48 V/V was 11.8%, and for +101 V/V the error for f_t was 7.08%. The reason for this error is the same as the error for +11 V/V ideal gain. The reason for the decrease in error as the gain increases is expressed in equation (1) where the larger the gain the smaller the frequency.

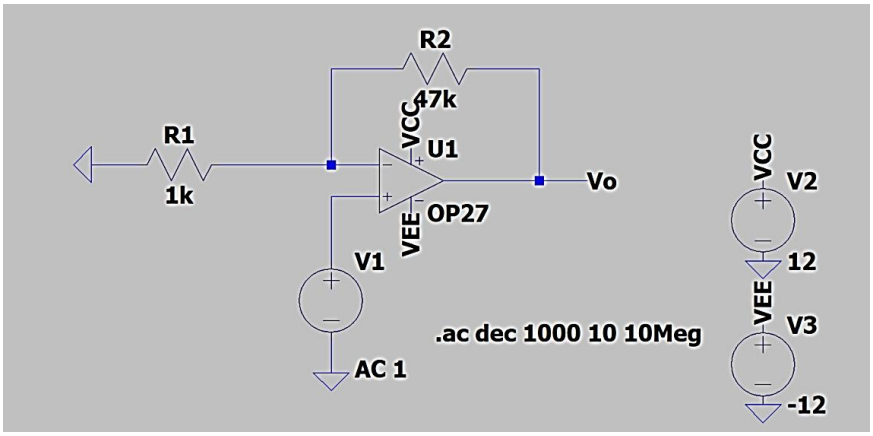

Figure 4: +48V/V Gain Circuit with AC analysis

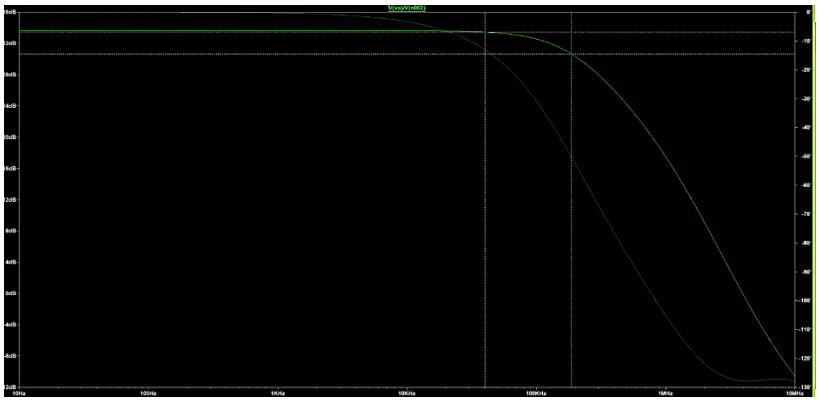

Figure 5: [Vout/Vin] plot for the Circuit in Fig. 4.

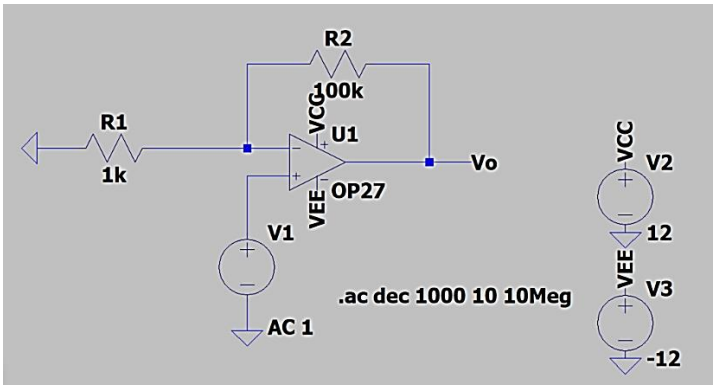

Figure 6: +101V/V Gain Circuit with AC analysis

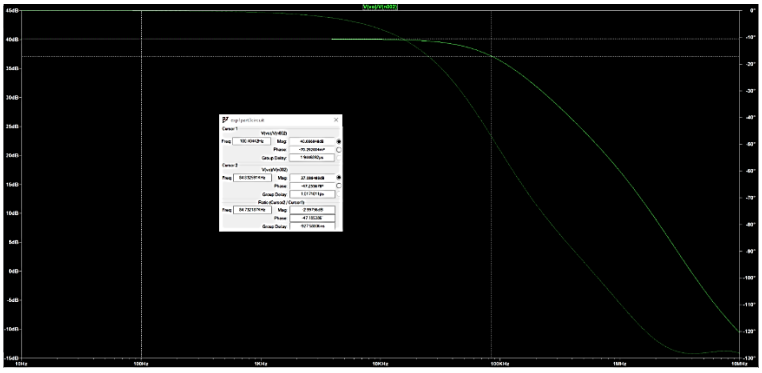

Figure 7: [Vout/Vin] plot for the Circuit in Fig. 6.

1.5 Conclusion

To conclude this experiment, as the ideal gain increased between +11 V/V to +48 V/V then +101 V/V the error between the typical f_t value and the experimental f_t value decreased due to the gain and frequency relationship expressed in equation (1). The significant error between them is due to the fact that the typical and minimum theoretical values are based on the deviation of a million op-amps.

Experiment #2 Slew Rate Distorion

2.1 Purpose

The purpose of experiment two was to determine the minimum and typical Slew Rate (SR) from the data sheet and compare them to the SR found experimentally using LTSPICE and the non-inverting amplifier. Using the SR value then to find fmax and identifying how the output voltage changes.

2.2 Theoretical Background

The focus for this experiment is to find the slew rate distortion. When considering a practical op-amp, they have limited maximum output current that supplies the load or sinks from the load. Other components of the practical op-amp is that is has an undesired output capacitance due to packaging, the internal design of the op-amp, the external layout, the breadboard and other factors. Equation (7) shows the current through the output capacitance below:

$$I_c = C\frac{dV_0}{dt} \qquad (7)$$

This can be rearranged to be solved for the output voltage derivative. When the maximum current supplied to the output capacitance is limited by the maximum output current, the maximum rate of the output voltage is limited. This defines the slew rate (SR), as shown in equation (8).

$$SR = \frac{dV_0}{dt}\Big| max = \frac{I_{o,max}}{C} \qquad (8)$$

Since the output current of the op-amp is limited, the rate of change for the output voltage is limited by its max value. The output signal as a sine wave is given in equation (9).

$$V_o(t) = V_m \sin(\omega t + \theta) \qquad (9)$$

Where the derivative is given in equation (10).

$$\frac{dV_0}{dt} = V_m \cos(\omega t + \theta) \qquad (10)$$

To find the maximum frequency, SR is used which is used before signal is distorted at the output which is shown in equation (11).

$$SR = \frac{dV_0}{dt}\Big| max = \omega V_m \qquad (11)$$

So then the maximum frequency in Hz before distorting the output signal is obtained in equation (12)

$$f_{max} < \frac{SR}{2\pi V_m} \qquad (12)$$

For the prelab calculations, the datasheet states that the SR(min)=1.7 V/us and the SR(typical)=2.8V/us. The drawn-out step response based on Fig.8 is shown in Fig. 9.

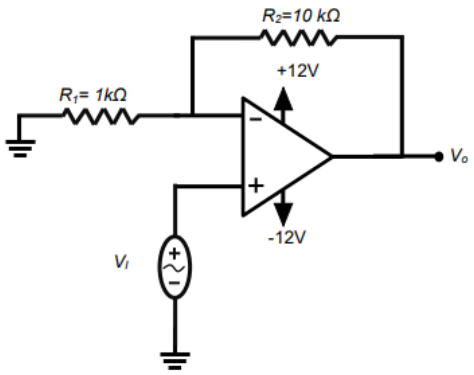

Figure 8: Non-inverting amplifier using OP27 op-amp.

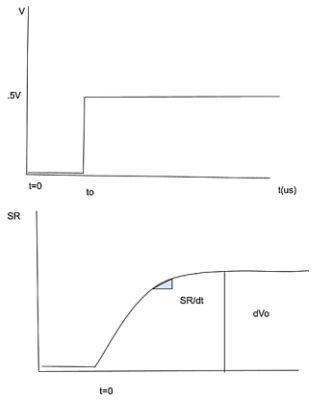

Figure 9: Step Response of Fig. 8.

Using equation (8) and the datasheet values, the t(min)= 3.23us and the t(typical)=1.96us. Then using equation (9) and (12) and the SR datasheet values, the $f_{max}(minSR) = 49.19\ kHz$ and $f_{max}(typicalSR) = 81\ kHz$. The peak-to-peak voltage is 1V for these values.

2.3 Procedure

1. Using LTSPICE and the OP27 op-amp, the non-inverting amplifier as shown in Figure 2 was connected.
2. A 0.5 V rectangular with time rise and time fall of 1ns, the ON Time (TON) of 10us and a period of 20us was applied.
3. A Transient Analysis was then applied to simulate two complete cycles with Maximum step size of 1ns to plot Vo(t). This was done by using 2 cursors to estimate slew rate in the linear region.
4. Using the SR experimental value obtained in step (3), $f_{max}$was estimated for the sine wave with amplitude of Vp = 0.5 V, R1= 1kΩ, R2=10 kΩ , and VI, Vo= +12V, -12V.
5. A Transient Analysis was applied to simulate 7-10 complete cycles with Maximum step size of 1ns to plot Vo(t).
6. Steps 4 and 5 were repeated with a f_{max} of 10X the first f_{max}.

2.4 Results & Analysis

The product of step 1 and step 2 and step 3 of the procedure is shown in Fig. 10.

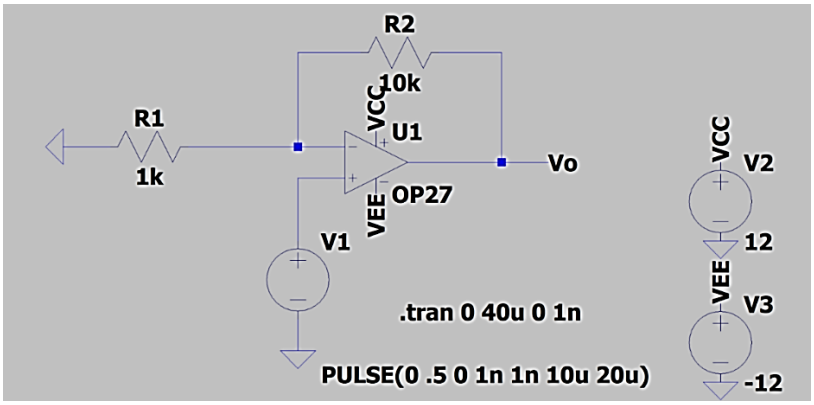

Figure 10: Non-Inverting Amplifier with Rectangular Pulse

Using the plot generated from the circuit in Fig.10 shown in Fig.11, SR was found by using 2 cursors to find the slope of the linear region. The experimental SR was found to be 3.14 V/us. Using equation (12), the ideal gain of +11 V/V and the experimental SR, the f_{max} was calculated to be 90.8 kHz. The error between the experimental and theoretical typical of f_{max} is 12.1%. This is due to the datasheet SR value being based on the deviation of million op amps.

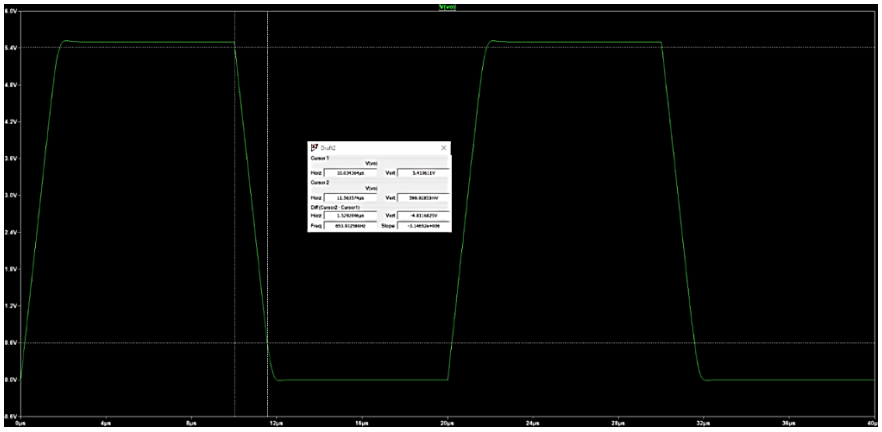

Figure 11: Rectangular Pulse Plot of Fig.10 to estimate SR.

The resulting circuit for step 4 and step 5 of the procedure is shown in Fig. 12. Fig. 13 shows the Vo graph of Fig.12.

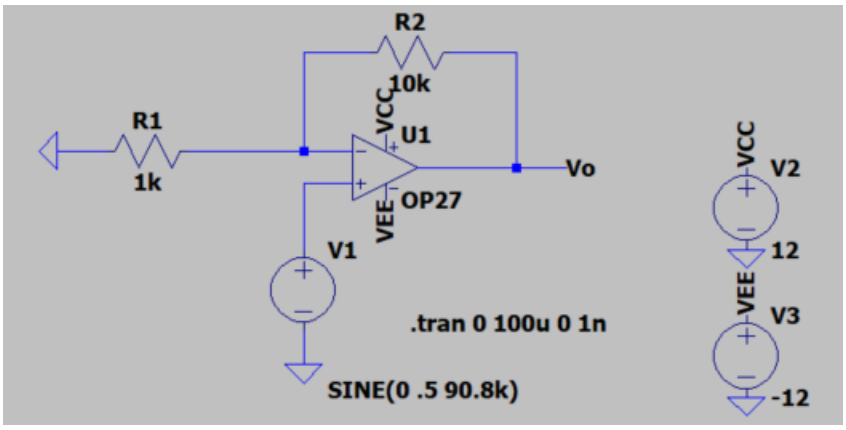

Figure 12: Fig. 8 Circuit with Sine wave, f_{max}, and Modified Trans Analysis

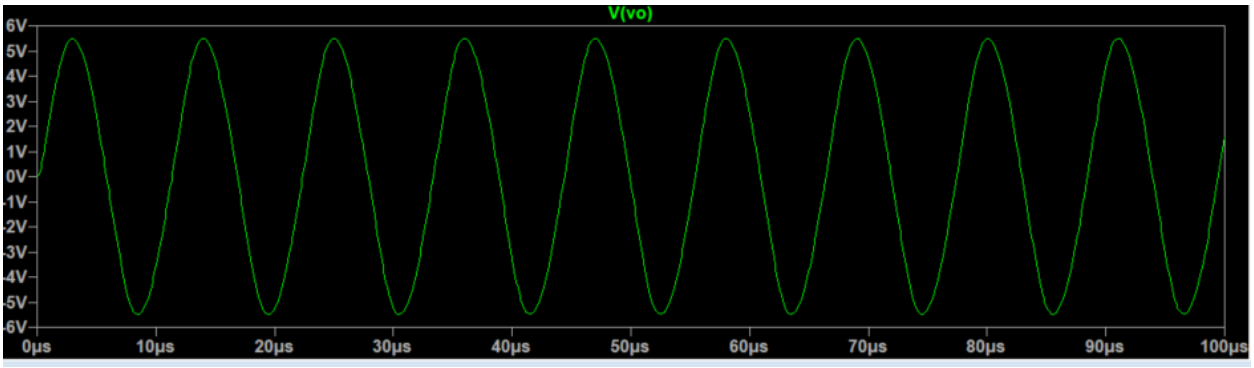

Figure 13: Plot of Fig. 12 Circuit for Vo

The resulting circuit for step 6 of the procedure is shown in Fig. 14. Fig. 15 shows the Vo graph of Fig.14.

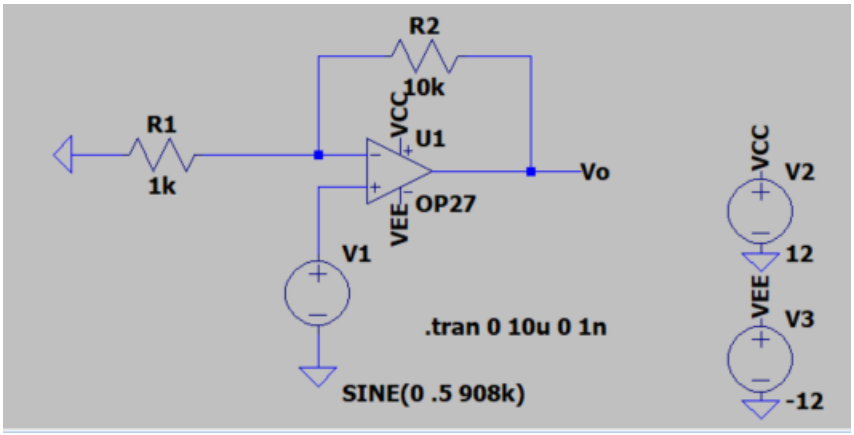

Figure 14: Fig. 8 Circuit with Sine wave,10* f_{max}, and Modified Trans Analysis

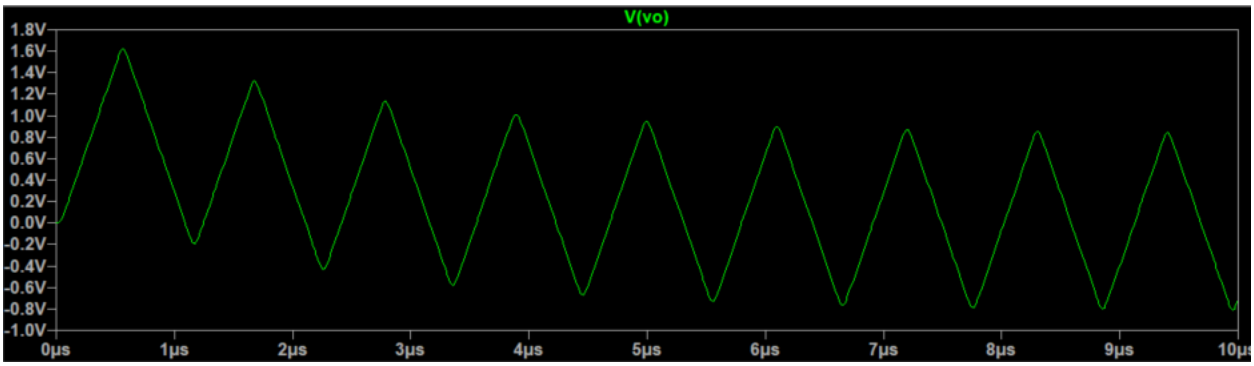

Figure 15: Plot of Fig. 14 Circuit for Vo

The difference between the sinewave plot of f_{max} and 10*f_{max} is that the sine becomes regular because as frequency increases the distortion increases.

2.5 Conclusion

To conclude this experiment, as the SR is found by identifying the slope of the linear region of a rectangular pulse graph. Using the SR, the f_{max} can be found using equation (12). Comparing the sinewave plot with f_{max} applied and the sinewave plot with 10*f_{max} the distortion increases, causing the sine to become more regular.

Experiment #3 DC Offset Voltage

3.1 Purpose

The purpose of the experiment is to find the input current to the inverting input and the non-inverting input. The strategy to find this is to find the output voltage and the output voltage due to the input offset voltage.

3.2 Theoretical Background

For ideal op-amps, they require the inverting and non-inverting inputs to be equal so that the voltage output is zero when the two inputs are equal. The op-amp shown in Fig. 16(a) has two inputs to be grounded, so Vo=0 ideally. In actuality, this is not the case, the inputs are not perfectly matched, and Vo is not zero. To demonstrate the mismatch imperfection, an internal dc voltage is assumed as shown in Fig.16(b). To further explain this figure, the op-amp has a very high differential gain so the output voltage will be saturated to one rail voltage in practice. The offset of the input voltage is typically extremely small, so measuring it directly is extremely difficult.

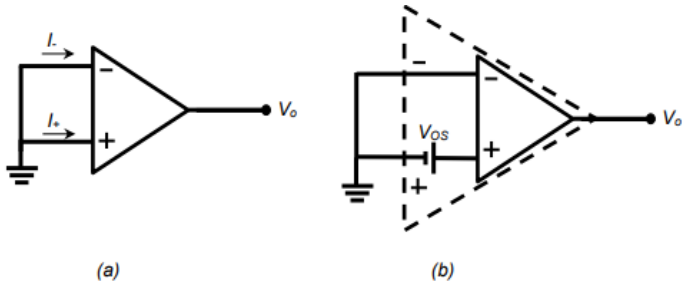

Figure 16: (a) both inputs are grounded (b) Modeling the mismatch as an input offset voltage.

Fig. 17 is used to estimate the input offset voltage of the LM308 op-amp with (a) and (b) demonstrating the same idea as Fig. 16 (a) and (b).

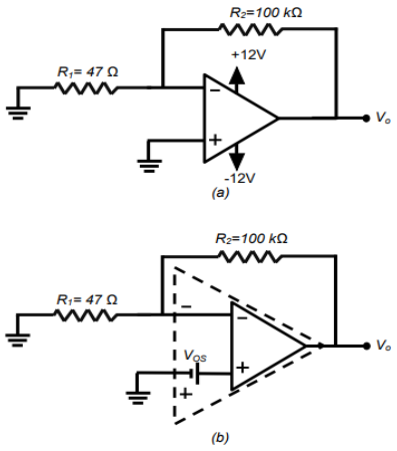

Figure 17: (a) The used circuit to estimate the input offset voltage (b) The circuit is modeled with the input offset voltage as a non-inverting amplifier

Highlighting further on the mismatched current inputs shown in Fig. 16. The inverting input (I-) and the non-inverting input (I+) are both non-zero. These are used to find the input bias current (I_B) and the input offset current (I_{OS}) defined in equations (13) and (14).

$$I_B = \frac{I_+ + I_-}{2} \qquad (13)$$

$$I_{OS} = |I_+ - I_-| \qquad (14)$$

To first find I_+ and I_-, the circuits in Fig. 18 (a) and (b) can be used, since they are too small to measure directly.

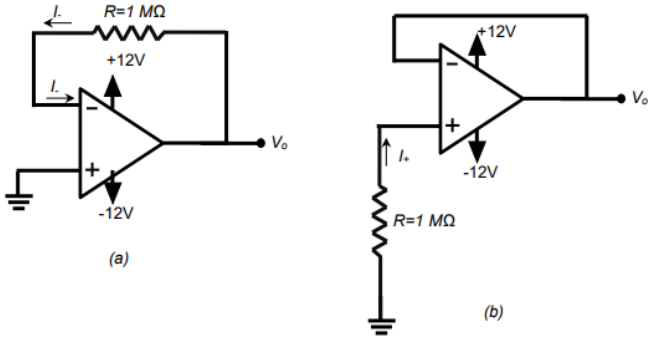

Figure 18: (a) The circuit used to estimate I-. (b) The circuit used to estimate I+.

Though measuring the currents directly cannot be done in lab, it is possible to minimize the DC imperfection of the op-amp circuit as shown in Fig. 19(a) by adding a compensated resistance (Rx) at the non-inverting input as shown in Fig. 19 (b).

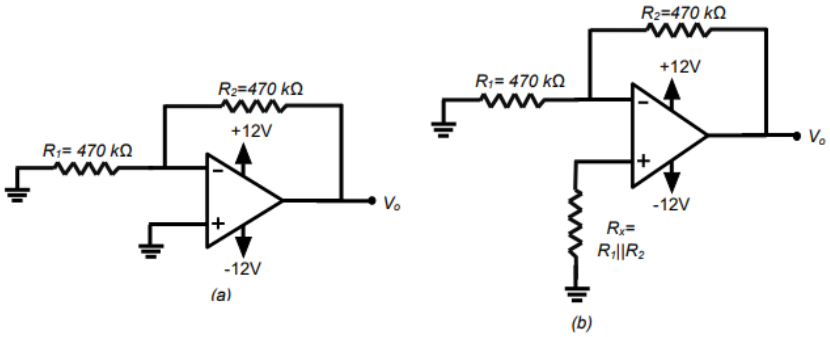

Figure 19: (a) Uncompensated circuit. (b) Compensated circuit.

As presented in the prelab, from the datasheet, the typical input offset voltage (V_O) is 2 mV and the maximum input offset voltage is 10 mV. The estimated V_{OS} typical and maximum using equation (15) and the datasheet V_O values was found to be 4.257V for the typical and 21.286V for the maximum.

$$V_{OS} = \frac{V_O}{1 + \frac{R_2}{R_1}} \qquad (15)$$

Using Fig. 18(a) and(b), the I_- is derived from Fig.18(a) using KCL at the node connect to the output voltage with the final equation shown in (16). I_+ is derived using the circuit in Fig.18(b) also using KCL. This is demonstrated in equation (17).

$$I_- = \frac{(V_O - V_{OS})}{R} \qquad (16)$$

$$I_+ = \frac{0 - V_x}{R} = \frac{0 - (V_O - V_{OS})}{R} = \frac{(V_{OS} - V_O)}{R} \qquad (17)$$

3.3 Procedure

1. Using LTSPICE the circuit of Figure 16(a) with LM308 was built.

2. Then Transient Analysis was applied with Stop Time of 10us and step size of 1ns, to then plot and record the output voltage Vo.

3. Then the circuit of Figure 17(a) with LM308 on LTSPICE was built.

4. This circuit used the same transient Analysis as in step 2 and the output voltage was plotted and recorded. This was used to calculate the input offset voltage.

3.4 Results & Analysis

Fig. 20 shows the resulting circuit built in LTSPICE to replicate Fig.16(a), Fig.21 shows the Vo plot of Fig.20. The Vo value was shown to be -3.0736V.

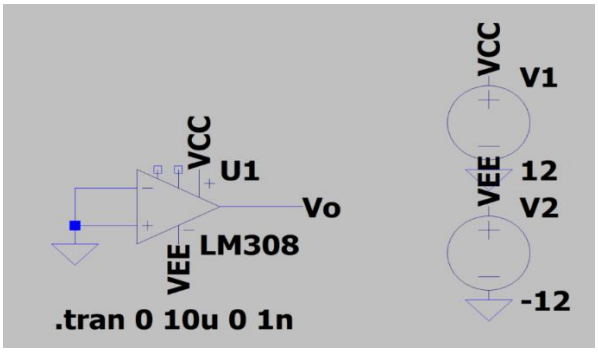

Figure 20: LTSPICE Replication of Fig.16(a).

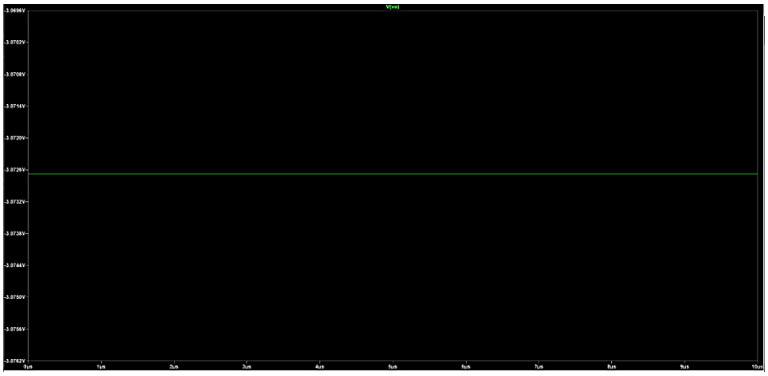

Figure 21: Plot of Vo for Fig.20.

Fig. 22 shows the resulting circuit built in LTSPICE to replicate Fig.17(a), Fig.23 shows the Vo plot of Fig.22. The Vo value was shown to be -3.4V.

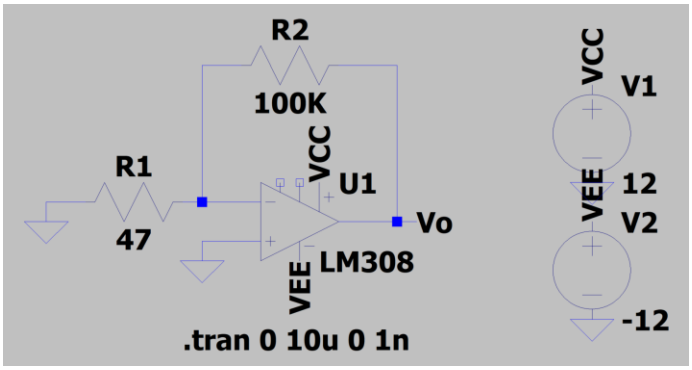

Figure 22: LTSPICE Replication of Fig.17(a).

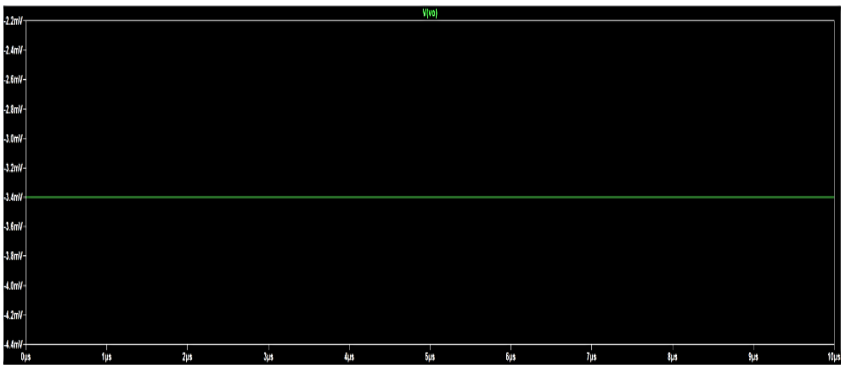

Figure 23: Plot of Vo for Fig.22.

The V_{OS} was then calculated using equation (15), Fig.22 values and Vo=-3.4 V, resulted in -1.597uV. This is a 99% error comparing to the theoretical due to LTSPICE using near ideal model and the theoretical is not ideal so the model is not accurate.

3.5 Conclusion

To conclude this experiment, the V_{OS} resulted in -1.597 uV which generates a 99% error. This is due to LTSPICE using a near ideal model. The input bias current and input offset current is difficult to measure because of how small it is value wise. The op-amp LM308 reveals that in LTSPICE, the Vo is not zero due to the inner Vos value and the unequal current input values.

Experiment #4 Common Mode Rejection Ratio

4.1 Purpose

The purpose of this experiment is to find the open loop common mode gain and the differential open loop gain of the op-amp. Then to use these values to find the common mode rejection ratio to then compare it to the datasheet value.

4.2 Theoretical Background

The ideal op-amps should only amplify the differential input voltage (V_d) and totally reject the common mode input voltage (V_{cm}). The mismatches and imperfections at the input stage do occur due to manufacturing limitations. The common mode rejection ratio (CMMR) is a metric used to quantify how good the op-amp is and the definition in dB is expressed in equation (18).

$$CMRR = 20log_{10}(\frac{A_d}{A_{CM}}) \qquad (18)$$

Where A_d is the open loop differential gain of the op-amp, and A_{CM} is the open loop common mode gain of the op-amp. To successfully calculate the CMRR, the A_{CM} and the A_d was experimentally measured, then compared to the datasheet value. To find the A_{CM}, Fig. 24 was built in LTSPICE to measure the peak-to-peak input and output voltage. Then equation (19) was used to calculate the A_{CM}.

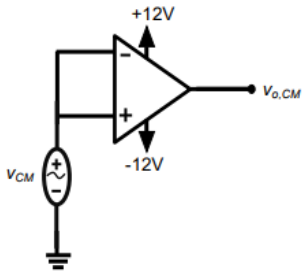

Figure 24: Common Mode Circuit

$$A_{CM} = \frac{v_{o,CM}}{v_{CM}} \qquad (19)$$

Then to find the A_d, Fig. 25 was used to find $v_{d,1}, v_{d,2}, v_{3,1}$, and $v_{3,2}$ to then calculate the differential gain with $v_{o,1}$, and $v_{o,2}$ being given as +9 V and -9 V. The equations used to do this are (20), (21) and (22).

$$v_{d,1} = \frac{-R_4}{R_4+R_3} v_{3,1} \approx \frac{-v_{3,1}}{1000} \qquad (20)$$

$$v_{d,2} = \frac{-R_4}{R_4+R_3} v_{3,2} \approx \frac{-v_{3,2}}{1000} \qquad (21)$$

$$A_d = \frac{v_{o,1} - v_{o,2}}{v_{d,1} - v_{d,2}} \qquad (22)$$

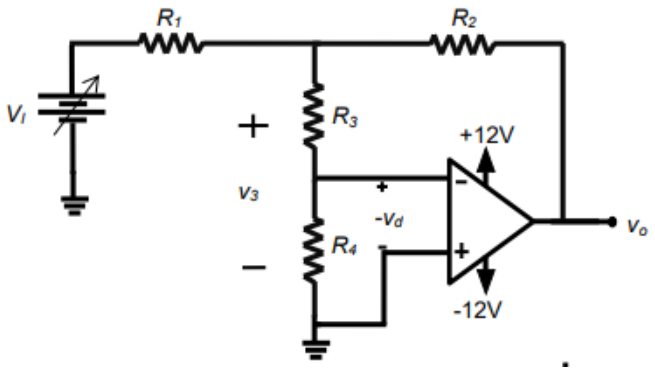

Figure 25: Differential Gain Circuit

Finally, once the A_{CM} and A_d are calculated, they can be plugged into equation (18) to find the CMRR. The CMRR datasheet value to compare to is between 80 and 100 dV.

4.3 Procedure

(a) Measuring the Common Mode Gain (A_{CM})

1. Using LTSPICE and LM308 op-amp, the circuit shown in Fig. 24 was built with a 10 V peak-to-peak sine wave at 200Hz applied. Also a transient analysis showing 10 cycles with proper step size was applied.
2. The output voltage (peak to peak) was measured using two cursors to record the r peak-to-peak input and output voltages to then calculate A_{CM} using equation (19).

(b) Measuring the Differential Gain (A_d)

1. Using LTSPICE and LM308 op-amp, Fig. 25 was built with R1=1 kΩ, R2=4.7 kΩ, R3=47 kΩ, and R4=47 Ω.
2. Then using linear DC analysis, the input voltage V_I was varied from -2.1V to 2.1V with step size of 0.0001 V.
3. This built circuit was then used to plot V_o vs. V_I which was used to measure $v_{i,1}$ when $v_{o,1}$ is +9 V and $v_{i,2}$ when $v_{o,2}$ is -9 V.
4. Once $v_{i,1}$ and $v_{i,2}$ were found, V_3 vs. V_I was plotted to find $v_{3,1}$, and $v_{3,2}$ at $v_{i,1}$ and $v_{i,2}$ respectively.
5. Using the variables found in steps 3 and 4 the differential input voltages were calculated using equations (20) and (21).
6. Then the differential gain was calculated using equation (22).
7. Finally, the experimental CMMR was calculated using the experimental gains and equation (18). Then this was compared to the CMRR on the datasheet.

4.4 Results & Analysis

Fig. 26 shows the LTSPICE built circuit of Fig. 24 with specified parameters from step (a)(1) of the procedure. Then Fig. 27 is the plot specified of Fig. 26 from step (a)(2) of the procedure used to find the input and output peak-to-peak voltages to calculate the common mode gain. $v_{o,P-P}$

was found to be 131.8 mV, and $v_{i,P-P}$ was found to be 9.995 V by using the cursors. Plugging this into equation (19) where $v_{o,P-P} = v_{o,CM}$and $v_{i,P-P} = v_{CM}$, the $A_{CM} = .013186\, V/V$.

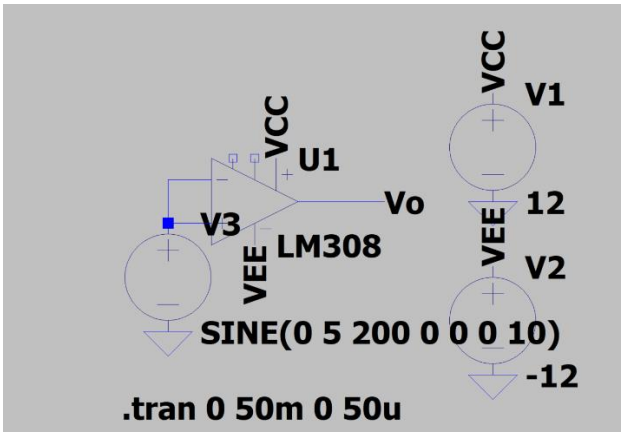

Figure 26: LTSPICE circuit of Fig. 24

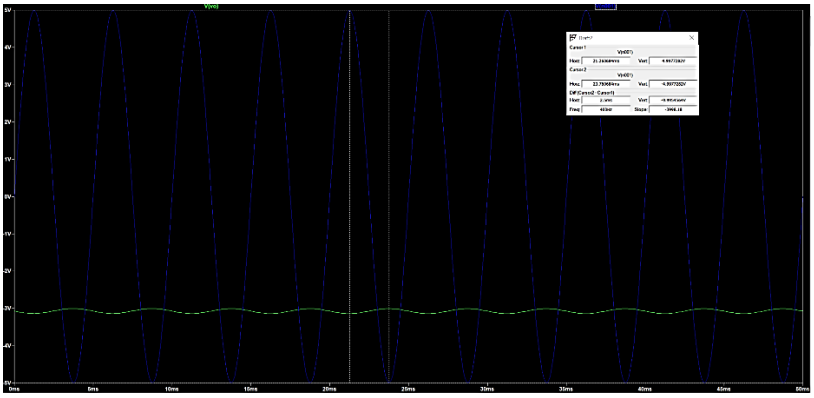

Figure 27: Plot of Fig. 26 showing Vo(P-P) and Vi(P-P) Sinewaves

Fig. 28 is the LTSPICE built circuit of Fig. 25 with the parameters specified in steps (b) (1) and (2) of the procedure. Fig. 29 and Fig. 30 are plots from Fig. 28 where Fig. 29 is the plot showing V_o vs. V_I and Fig. 30 is the plot showing V_3 vs. V_I. By tracing both graphs as specified in steps (b) (3) and (4), $v_{i,1}$ and $v_{i,2}$ were traced to be -1.9235 V and 1.919V respectively. $v_{3,1}$, and $v_{3,2}$ were traced to be -6.513 mV, and 3.219 mV respectively.

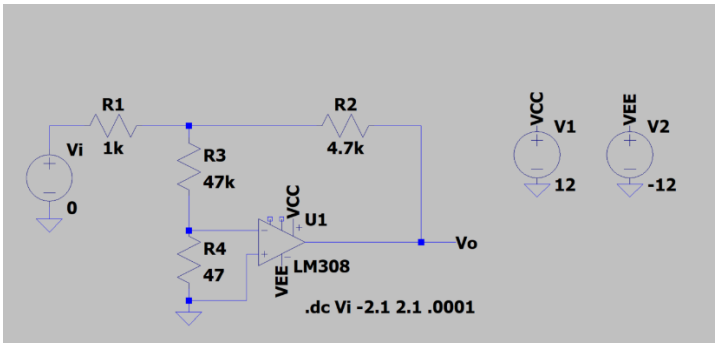

Figure 28: LTSPICE Circuit of Fig. 25 with given Parameters.

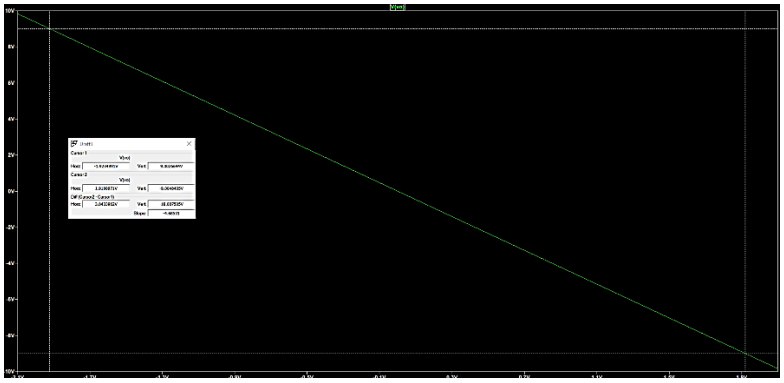

Figure 29: Plot of Fig. 28 showing V_o vs. V_I.

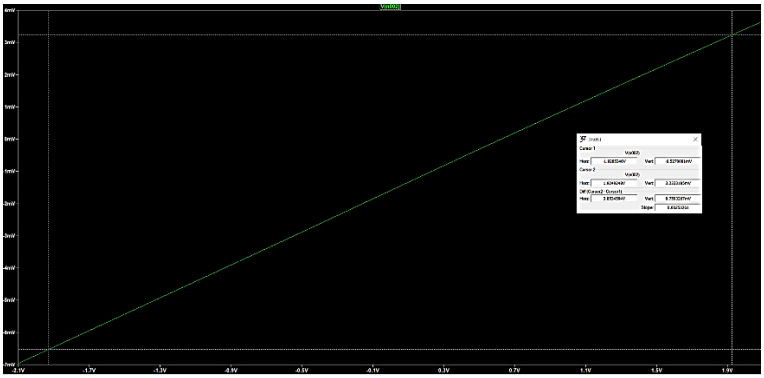

Figure 30: Plot of Fig. 28 showing V_3 vs. V_I.

Once these voltage variables were found $v_{3,1}$, and $v_{3,2}$ were used in equations (20) and (21) to find $v_{d,1}$ and $v_{d,2}$ which were calculated to be 6.513uV and -3.219 uV respectively. Then using $v_{o,1}$, and $v_{o,2}$ being given as +9 V and -9 V, and $v_{d,1}$ and $v_{d,2}$ that was calculated with equation (22), the A_d was found to be 1.85 MV/V. Lastly, using the experimental $A_d$and A_{CM} with equation (18), the experimental CMRR was found to be 162.94 dV which is higher than the 80 to 100 range found on the data sheet. This gives a 62.94% error from the 100 value. This error is due to LTSPICE using a near ideal model of LM308 which causes the circuit to be in accurate, as well as the theoretical value being based on the deviation of a million different op-amps.

4.5 Conclusion

To conclude this experiment, the near ideal model in LTSPICE warrants high inaccuracy for the differential gain, the common mode gain and the CMRR. Also the fact that the datasheet values are based on a million different op-amps, also warrants high error. The given datasheet CMRR was 80-100 dV which is a 62.94% from the experimental value of 162.94 dV.