Pipelining

Pipelining is the process of accumulating instruction from the processor through a pipeline. It allows storing and executing instructions in an orderly process. It is also known as pipeline processing. Pipelining is a technique where multiple instructions are overlapped during execution.

OR

Pipelining organizes the execution of the multiple instructions simultaneously. Pipelining improves the throughput of the system. In pipelining the instruction is divided into the subtasks. Each subtask performs the dedicated task.

1. In the first subtask, the instruction is fetched.
2. The fetched instruction is decoded in the second stage.
3. In the third stage, the operands of the instruction are fetched.
4. In the fourth, arithmetic and logical operation are performed on the operands to execute the instruction.
5. In the fifth stage, the result is stored in memory.

Types of Pipelining

Arithmetic Pipelining

It is designed to perform high-speed floating-point addition, multiplication and division. Here, the multiple arithmetic logic units are built in the system to perform the parallel arithmetic computation in various data format. Examples of the arithmetic pipelined processor are Star-100, TI-ASC, Cray-1, Cyber-205.

Instruction Pipelining

Here, the number of instruction are pipelined and the execution of current instruction is overlapped by the execution of the subsequent instruction. It is also called instruction lookahead.

Processor Pipelining

Here, the processors are pipelined to process the same data stream. The data stream is processed by the first processor and the result is stored in the memory block. The result in the memory block is accessed by the second processor. The second processor reprocesses the result obtained by the first processor and the passes the refined result to the third processor and so on.

Unifunction Vs. Multifunction Pipelining

The pipeline performing the precise function every time is unifunctional pipeline. On the other hand, the pipeline performing multiple functions at a different time or multiple functions at the same time is multifunction pipeline.

Static vs Dynamic Pipelining

The static pipeline performs a fixed-function each time. The static pipeline is unifunctional. The static pipeline executes the same type of instructions continuously. Frequent change in the type of instruction may vary the performance of the pipelining.

Dynamic pipeline performs several functions simultaneously. It is a multifunction pipelining.

Scalar vs Vector Pipelining

Scalar pipelining processes the instructions with scalar operands. The vector pipeline processes the instruction with vector operands.

Linear Pipeline Processors

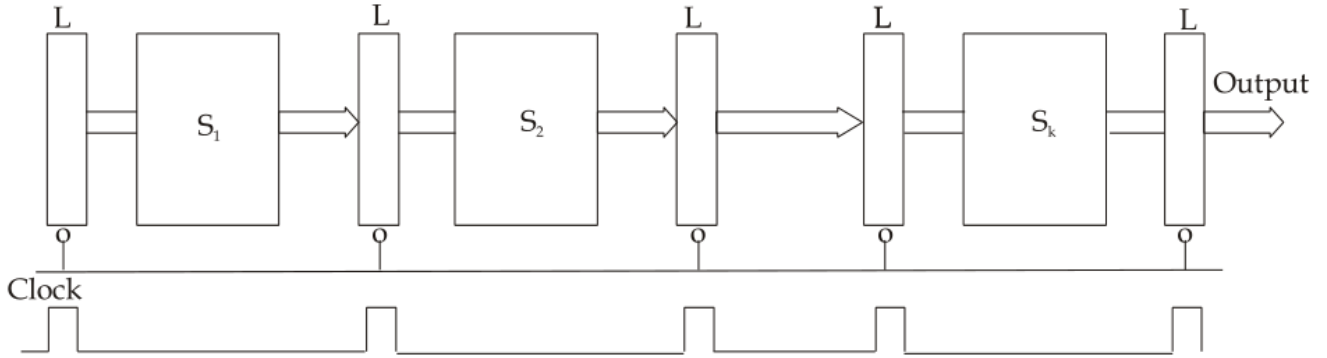
A linear Pipeline processor is a flow of processing stages which are linearly connected to perform a fixed function over a stream of data flowing from one end to other. In modern computers, linear pipelines are applied for instruction execution, arithmetic computation, memory access operations.

A linear pipeline processor is built with the processing stages. External inputs are inputted into the pipeline at the first stage S1. The processed results are passed from stage Si to stage Si+1 for all i = 1,2…….K-1.The final result appear from the pipeline at the last stage Sk.

Depending on the control of data flow along the pipeline, linear pipelines are formed in two group.

Asynchronous Model: Data flow amid adjacent stages in asynchronous pipeline is controlled by handshaking protocol. When stage S1 is ready to transmit, it sends a ready signal to Si + 1. After stage Si+1 receives the incoming data, it returns an acknowledge signal to Si.

Synchronous Model: Clocked latches are used to interface between stages. The latches are made with master slave flip flops, which can detach inputs from outputs upon the arrival of a clock pulse, all latches transfer data to the next stage simultaneously.



Reservation Table in linear pipelining

The utilization pattern of successive stages in a synchronous pipeline is mentioned by reservation table. The table is essentially a space time diagram depicting the precedence relationship in using the pipeline stages. For a K- stage linear pipeline, 'K' clock cycles are needed to flow through the pipeline.