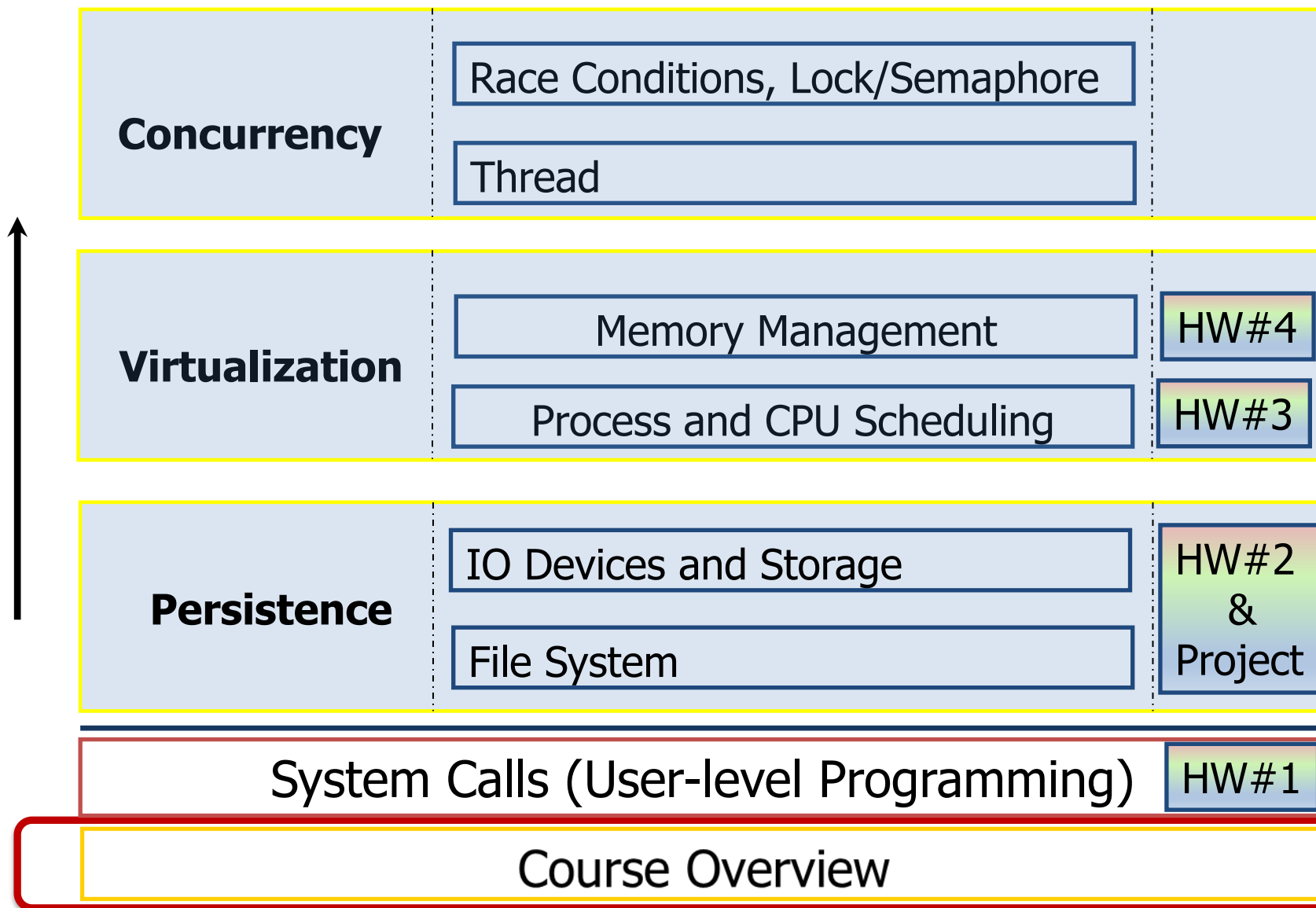


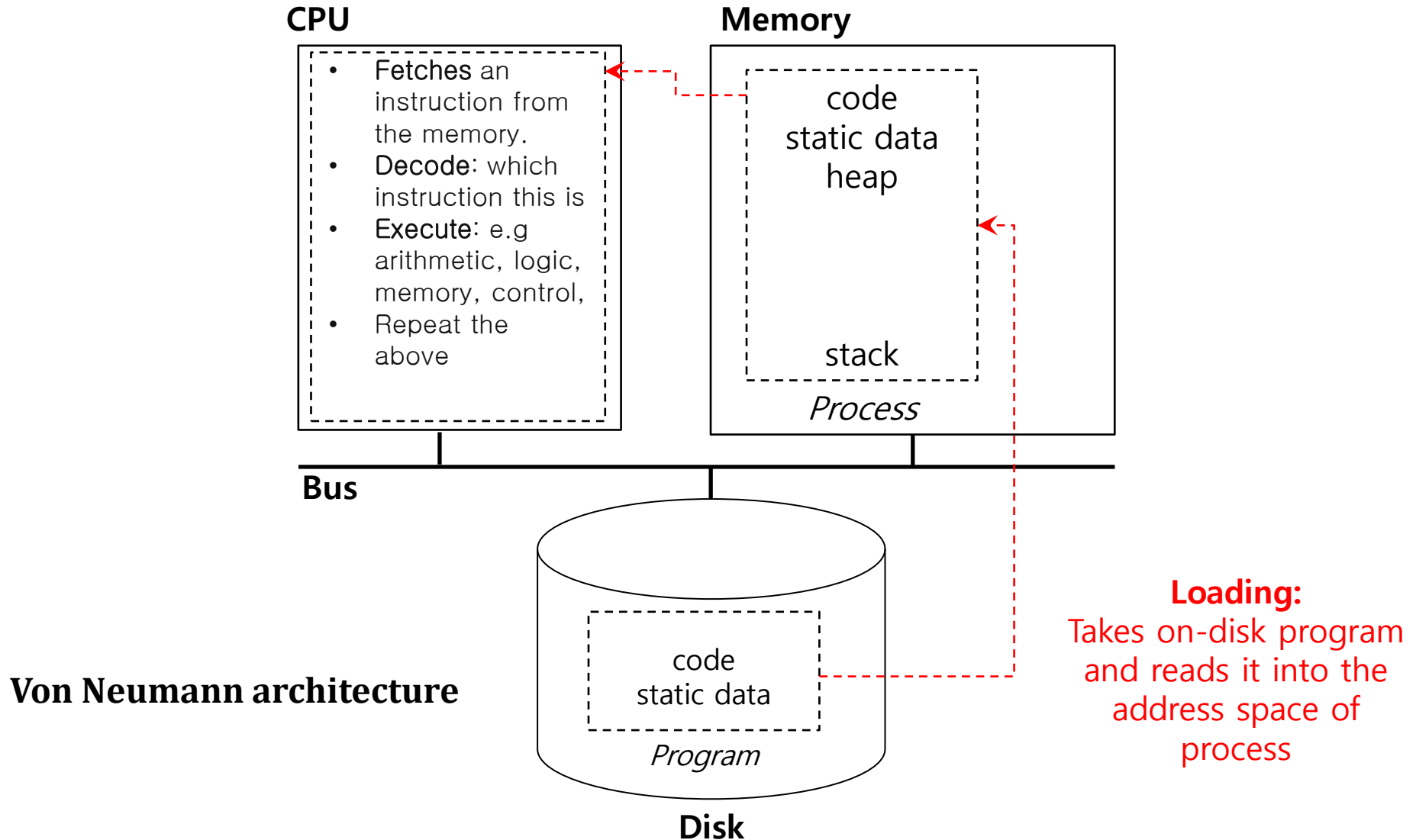
# **Lecture 1: Course Overview: Introduction to OS**

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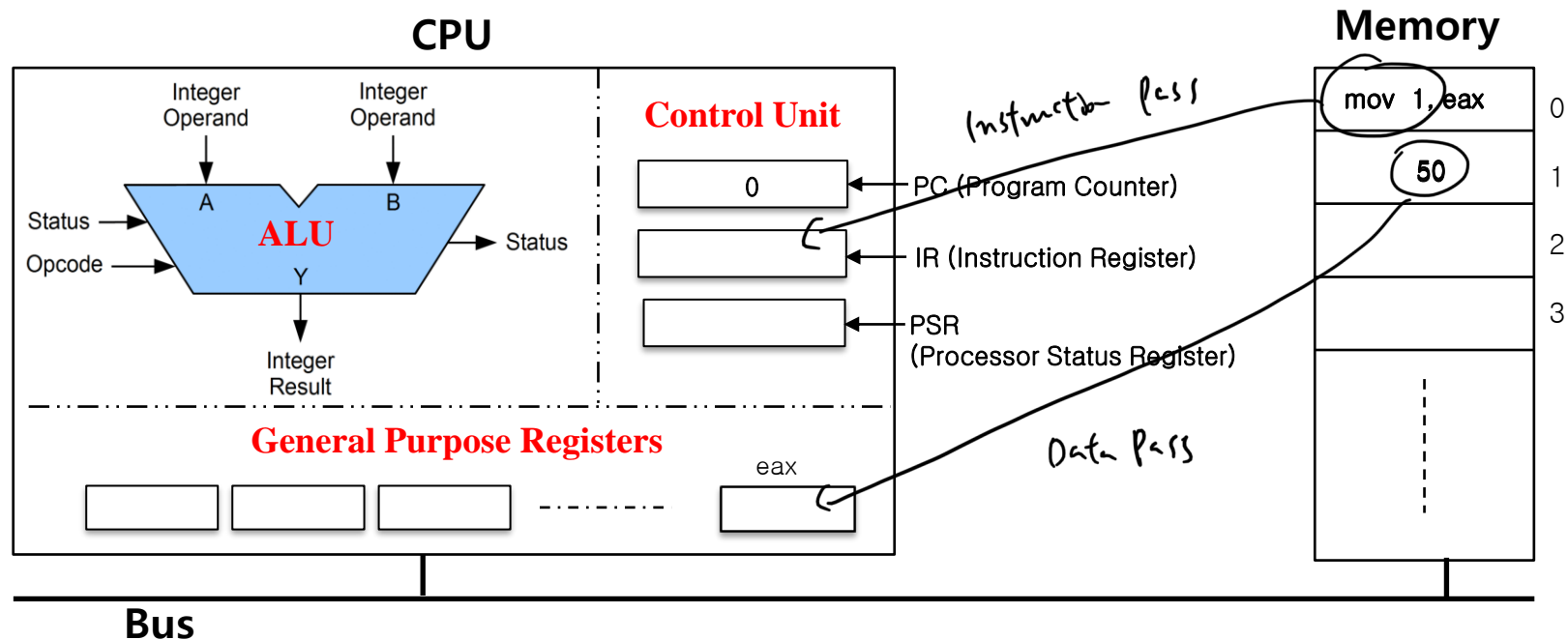
# The Course Organization (Bottom-up)



# What happens when a program runs?



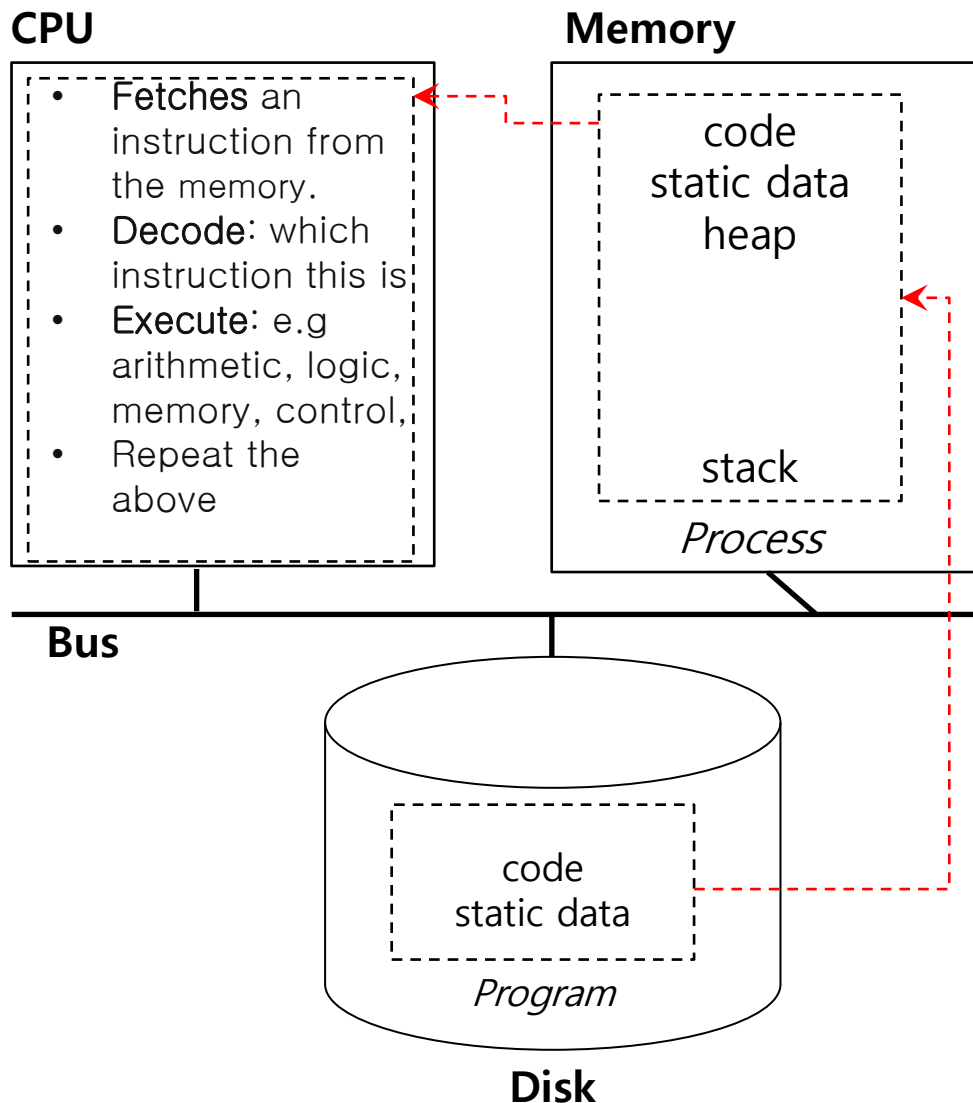
# How CPU works?



1. **Fetch** an instruction from memory.
2. **Decode:** Figure out which instruction this is
3. **Execute:** i.e., arithmetic/logic operations (e.g. add/and), memory, condition, branch, etc.

**Repeat the above steps**

# Operating System (OS)



## □ OS's major functions

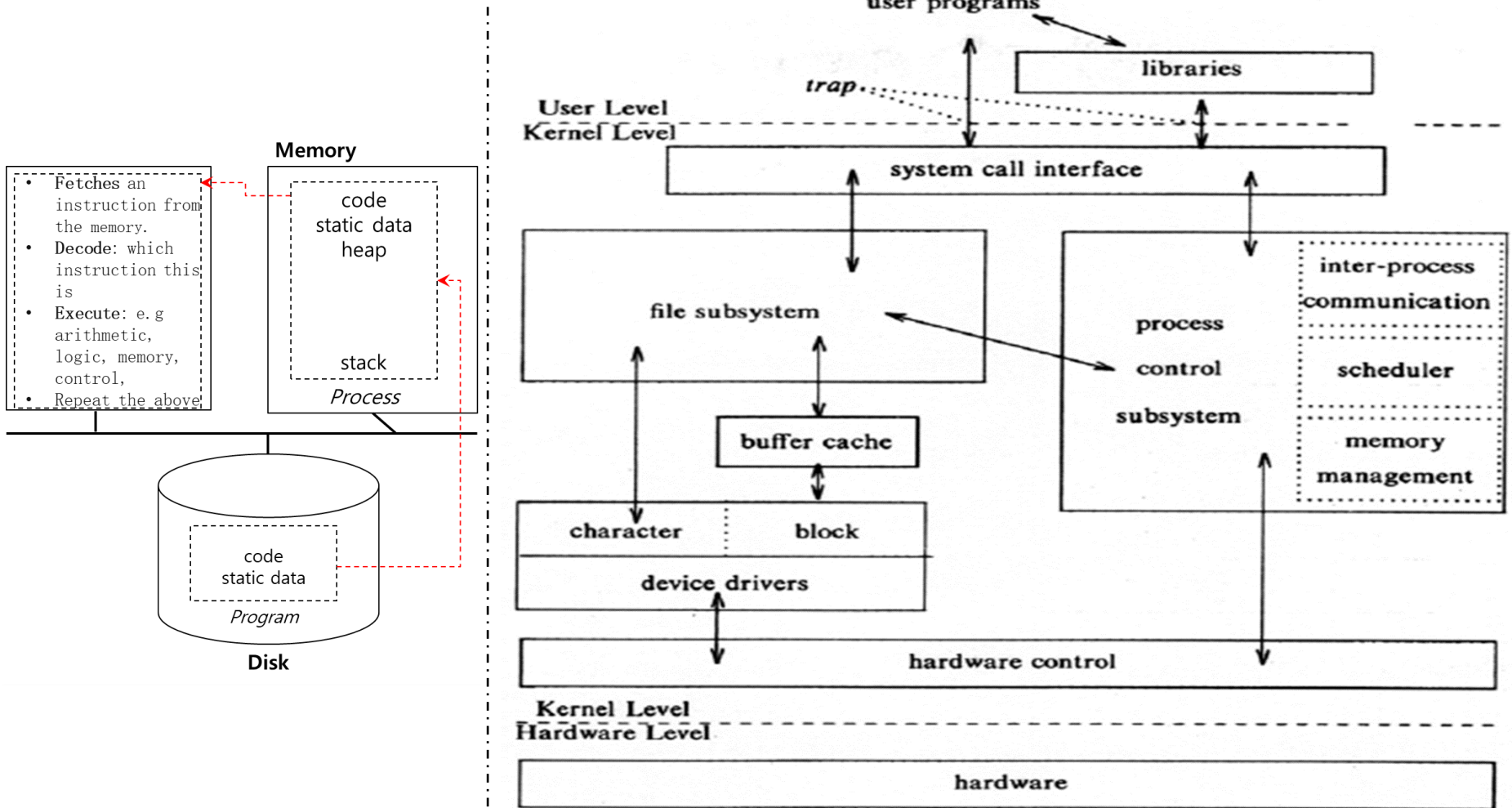
- ◆ Manage Resources (*virtualization*)
  - CPU, Memory, Disk, etc.
- ◆ Provide Services (*system call*)
  - **Process (running program)**: Easily **run** programs
  - **Memory**: **Share** memory among processes
  - **IO devices**: Enable processes to interact with or operate/utilize devices

# OS – Resource management via virtualization

- ❑ The OS **manages resources** such as *CPU*, *memory* and *disk*.
  - ◆ many programs to run (processes) → Sharing the CPU
  - ◆ many processes to *concurrently* access their own instructions and data → Sharing memory
  - ◆ many processes to access devices → Sharing disks
  - ◆ etc.
- ❑ How to achieve this – **Virtualization**
  - ◆ OS takes a **physical resource** and transforms it into a **virtual form** of itself.
    - **Physical resource**: Processor, Memory, Disk ...
  - ◆ The virtual form is more general, powerful and easy-to-use.
  - ◆ We can refer to the OS as a **virtual machine**.

# System call

- OS provides services (to utilize resources) via System Call (typically a few hundred) to run process, access memory/devices, etc.



# Virtualizing the CPU

- The system has a very large number of virtual CPUs.
  - ◆ Turn a single CPU into a seemingly infinite number of CPUs.
  - ◆ Allow many processes to seemingly run at the same time  
→ **Virtualizing the CPU**



# Virtualizing the CPU (Cont.)

```
1 #include <stdio.h>
2 #include <stdlib.h>
3 #include <sys/time.h>
4 #include <assert.h>
5 #include <unistd.h>
6
7 int main(int argc, char *argv[])
8 {
9     if (argc != 2) {
10         fprintf(stderr, "usage: cpu <string>\n");
11         exit(1);
12     }
13
14     char *str = argv[1];
15     int i=0;
16
17     while (i<100) {
18         sleep(1);
19         i++;
20         printf("%s\n", str);
21     }
22     return 0;
23 }
24
```

**Simple Example(cpu.c): Code that loops and prints**

# Virtualizing the CPU (Cont.)

## ▣ Execution result 1.

```
prompt> gcc -o cpu cpu.c swal  
prompt> ./cpu A  
A  
A  
A  
^C  
prompt>
```

**Pressing "Ctrl-c" to halt the program**

# Virtualizing the CPU (Cont.)

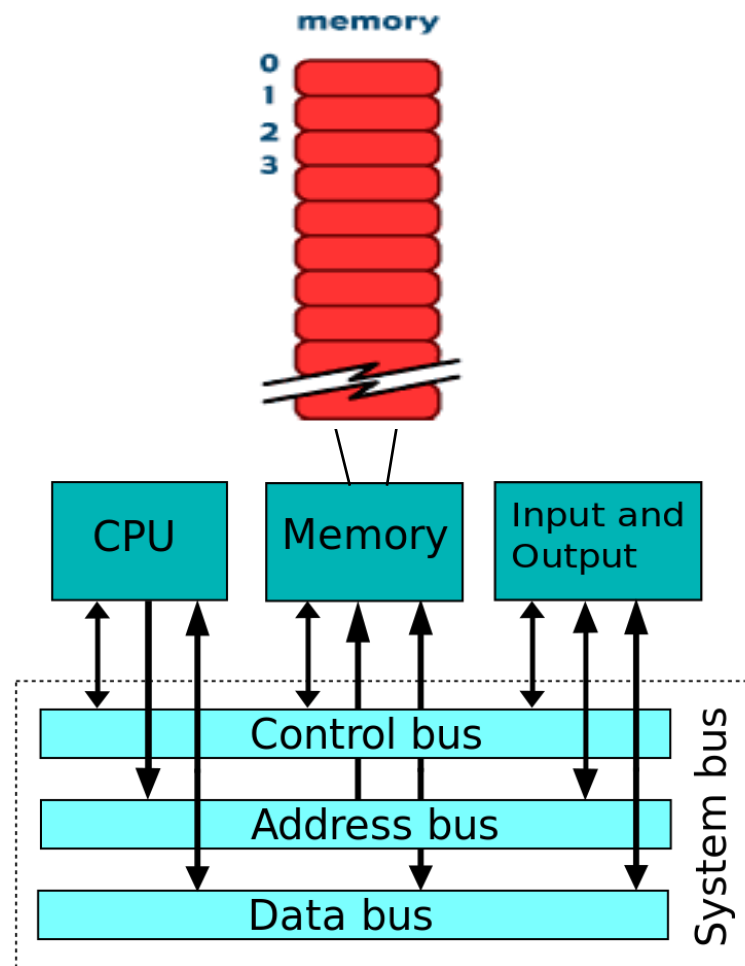
## ❑ Execution result 2.

```
prompt> ./cpu A &  ./cpu B &  ./cpu C &  ./cpu D &  
[1] 7353  
[2] 7354  
[3] 7355  
[4] 7356  
A  
B  
D  
C  
A  
B  
D  
C  
A  
C  
B  
D  
...
```

Even though we have only **one CPU**, the four processes  
seem to be running **at the same time!**

# Virtualizing Memory

- ❑ The physical memory is *an array of bytes*.
- ❑ A program keeps all of its data structures in memory.
  - ◆ **Read memory (load):**
    - Specify an address to be able to access the data
  - ◆ **Write memory (store):**
    - Specify the data to be written to the given address



# Virtualizing Memory (Cont.)

## ▣ A program that Accesses Memory (mem.c)

```
1      #include <unistd.h>
2      #include <stdio.h>
3      #include <stdlib.h>
4      #include <assert.h>
5      #define MAX 1000000000
6      int
7      main(int argc, char *argv[])
8      {
9          int *p = malloc(MAX*sizeof(int)); // a1: allocate memory
10         assert(p != NULL);
11         printf("(%d) Address Range: %08x %08x\n",getpid(),
12                (unsigned) p, (unsigned) (p+MAX-1));
13         *p = 0; // a3: put zero into the first slot of the memory
14         int i=0;
15         while (i<10) {
16             sleep(1);
17             *p = *p + 1; i=i+1;
18             printf("(%d) p: %d\n", getpid(), *p);
19         }
20         return 0;
21     }
```

# Virtualizing Memory (Cont.)

## □ The output of the program `mem.c`

```
prompt> ./mem
(25187) Address Range: 9f7eb008 - b7563404
(25187) p: 1
(25187) p: 2
(25187) p: 3
(25187) p: 4
(25187) p: 5
(25187) p: 6
(25187) p: 7
(25187) p: 8
(25187) p: 9
(25187) p: 10
```

- ◆ The newly allocated memory range is at 9f7eb008 - b7563404.
- ◆ It updates the value and prints out the results.

# Virtualizing Memory (Cont.)

## ❑ Running mem.c multiple times

```
prompt> ./mem & ./mem &  
(25274) Address Range: 9f7eb008 - b7563404  
(25275) Address Range: 9f8c0008 - b7638404  
(25274) p: 1  
(25275) p: 1  
(25274) p: 2  
(25275) p: 2  
(25274) p: 3  
(25275) p: 3  
(25274) p: 4  
(25275) p: 4  
...
```

- ◆ The memory ranges from two processes are overlapped – Each process has its own private memory.
  - Each running program has allocated memory at its own address space.
  - Each seems to be updating the value independently.

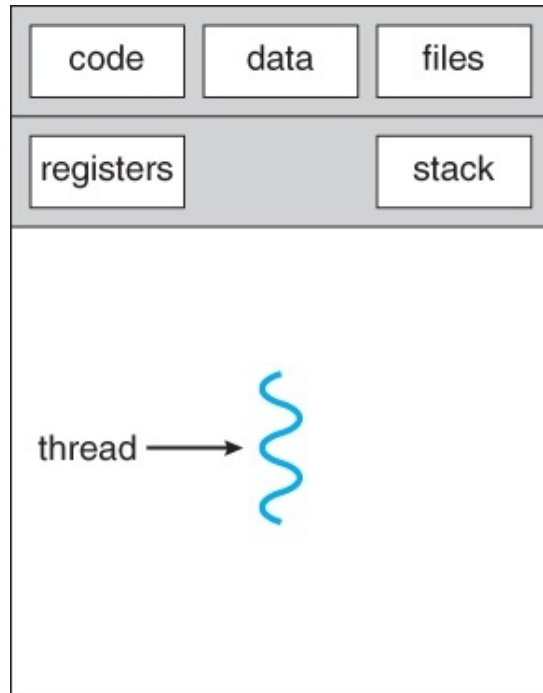
# Virtualizing Memory (Cont.)

- Each process accesses its own private **virtual address space**.
  - ◆ The OS maps **address space** onto the **physical memory**.
  - ◆ A memory reference within one running program does not affect the address space of other processes.
  - ◆ Physical memory is a shared resource, managed by the OS.

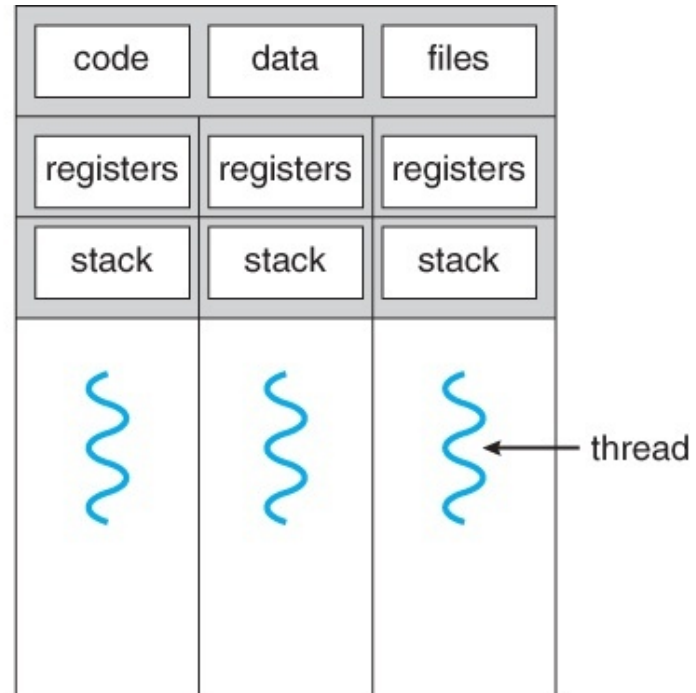


# Concurrency Problem

- ❑ The OS is juggling **many things at once**, first running one process, then another, and so forth.
- ❑ Modern **multi-threaded programs** also exhibit the concurrency problem.



single-threaded process



multithreaded process

# Concurrency Example

## ■ A Multi-threaded Program (thread.c)

```
1      #include <stdio.h>
2      #include <stdlib.h>
3      #include <pthread.h>
4
5      volatile int counter = 0;
6      int loops; ← 1000
7
8      void *worker(void *arg) {
9          int i;
10         for (i = 0; i < loops; i++) {
11             counter++;
12         }
13         return NULL;
14     }
```

2 workers : 2,000

# Concurrency Example (Cont.)

```
16     int
17     main(int argc, char *argv[])
18     {
19         if (argc != 2) {
20             fprintf(stderr, "usage: threads <value>\n");
21             exit(1);
22         }
23         loops = atoi(argv[1]);
24         pthread_t p1, p2;
25         printf("Initial value : %d\n", counter);
26
27         pthread_create(&p1, NULL, worker, NULL);
28         pthread_create(&p2, NULL, worker, NULL);
29         pthread_join(p1, NULL);
30         pthread_join(p2, NULL);
31         printf("Final value : %d\n", counter);
32         return 0;
33     }
```

- ◆ The main program creates **two threads**.
  - Thread: a function running within the same memory space. Each thread starts running in a routine called `worker()`.
  - `worker()`: increments a counter

## Concurrency Example (Cont.)

- ▣ `loops` determines how many times each of the two workers will **increment the shared counter** in a loop.

- ◆ `loops: 1000.`

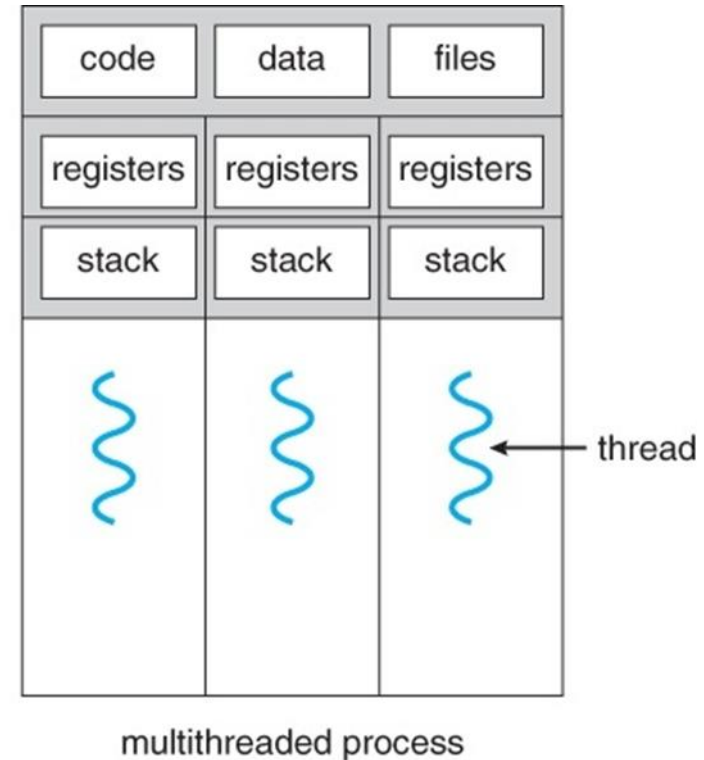
```
prompt> gcc -o thread thread.c -Wall -pthread
prompt> ./thread 1000
Initial value : 0
Final value : 2000
```

- ◆ `loops: 1000000000`

```
prompt> ./thread 1000000000
Initial value : 0
Final value : 1997974414 // huh??
prompt> ./thread 1000000000
Initial value : 0
Final value : 1997940107 // what the??
```

# Why is this happening?

- ▣ Increment a shared counter → take three instructions.
  1. Load the value of the counter from the memory into a register.
  2. Increment it
  3. Store it back into the memory
  
- ▣ These three instructions do not execute **atomically**. → Problem of **concurrency** happen.



# What happened?

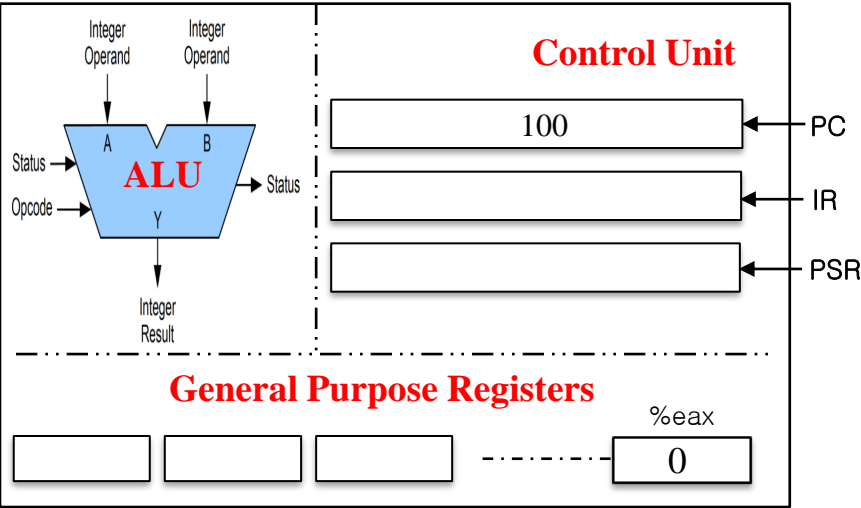
## □ Example with two threads

- ♦  $\text{counter} = \text{counter} + 1$  (**initial value: 50**)
- ♦ We expect the result is **52**. However,

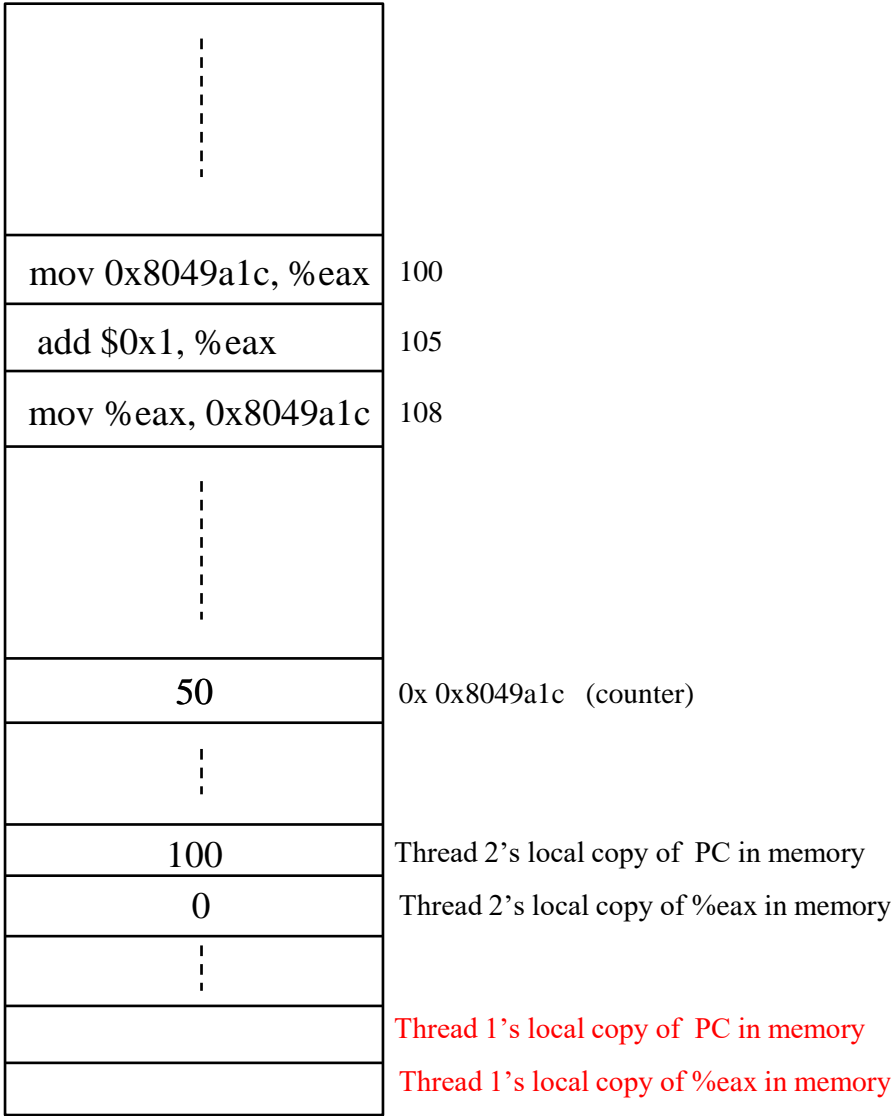
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	mov 0x8049a1c, %eax		105	50	50
	add \$0x1, %eax		108	51	50
interrupt	save T1's state				
	restore T2's state		100	0	50
		mov 0x8049a1c, %eax	105	50	50
		add \$0x1, %eax	108	51	50
		mov %eax, 0x8049a1c	113	51	51
interrupt	save T2's state				
	restore T1's state		108	51	51
	mov %eax, 0x8049a1c		113	51	<b>51</b>

# Step 0: Initial Value (PC=100)

## CPU



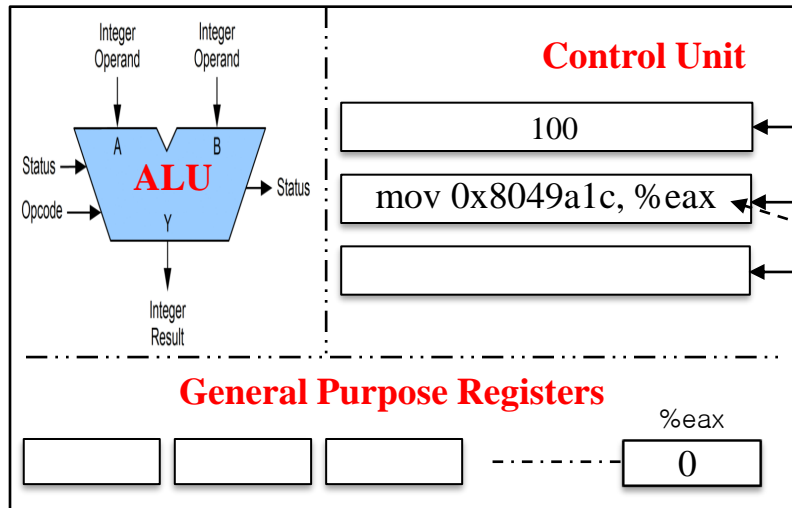
## Memory



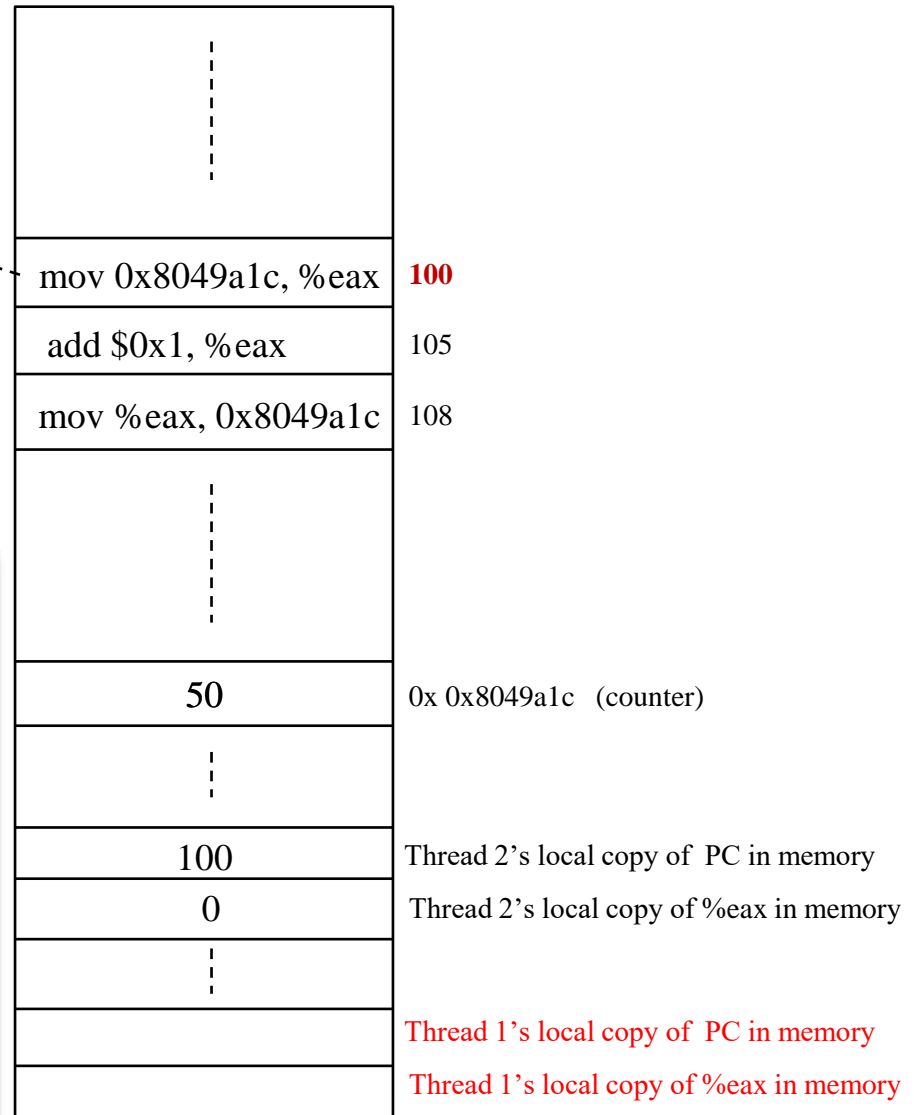
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
	<u>mov</u> <u>%eax</u> , 0x8049a1c		113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
	<u>mov</u> <u>%eax</u> , 0x8049a1c		113	51	51

# Step 1: Fetch instruction from the memory (PC->Address=100)

## CPU



## Memory

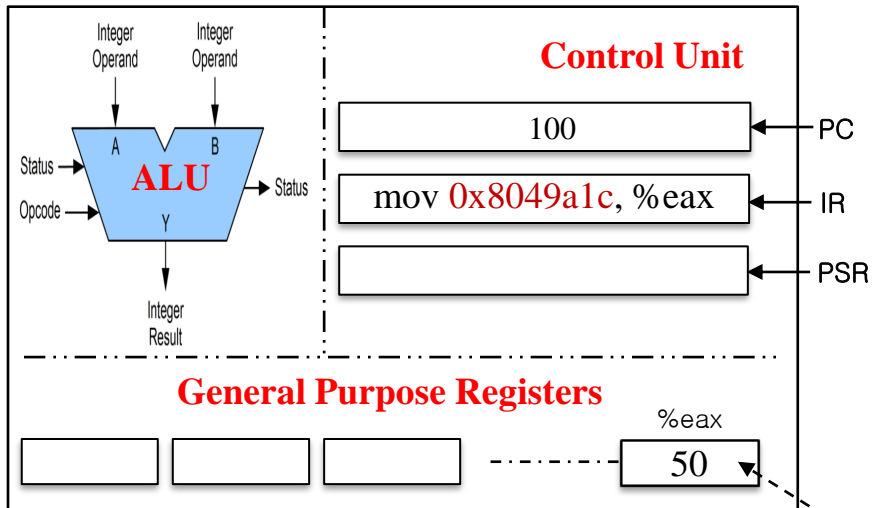


OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<u>mov 0x8049a1c, %eax</u>		105	50	50
	<u>add \$0x1, %eax</u>		108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
	<u>mov 0x8049a1c, %eax</u>		105	50	50
	<u>add \$0x1, %eax</u>		108	51	50
	<u>mov %eax, 0x8049a1c</u>		113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
	<u>mov %eax, 0x8049a1c</u>		113	51	51

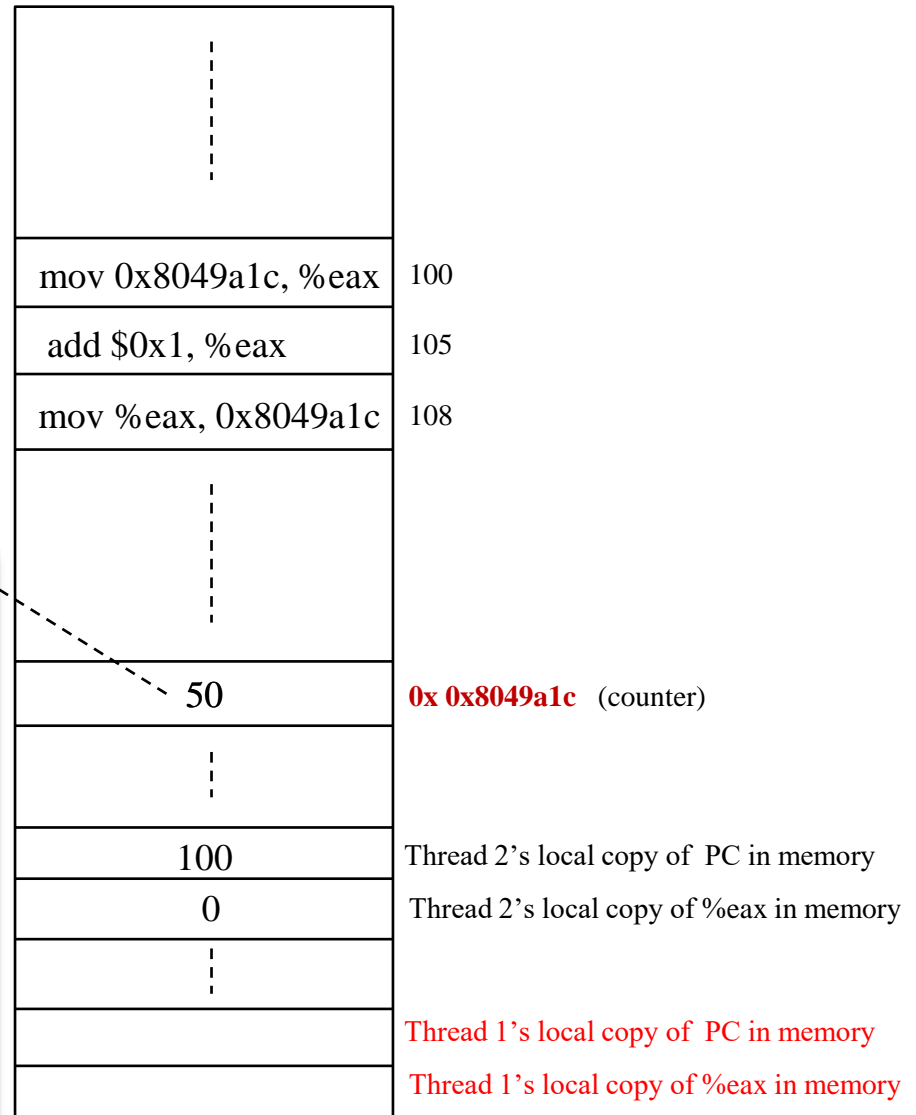


# Steps 2 & 3: Decode & Execution

## CPU



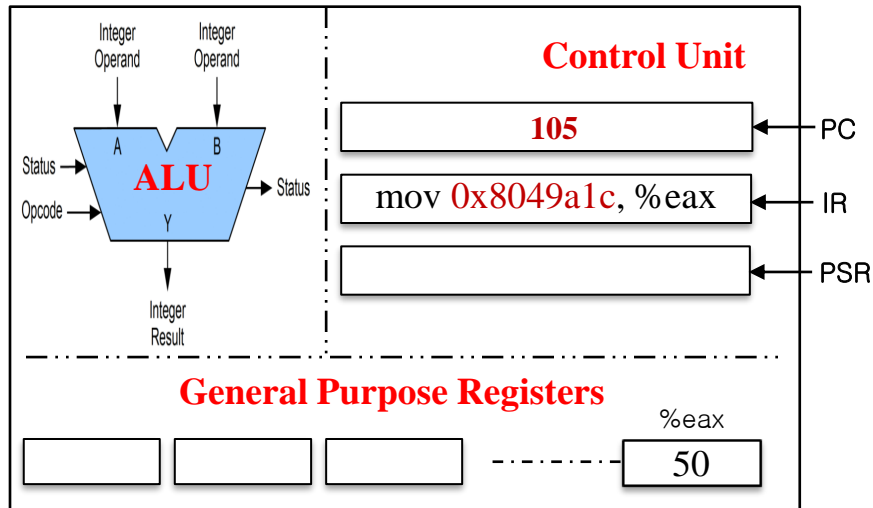
## Memory



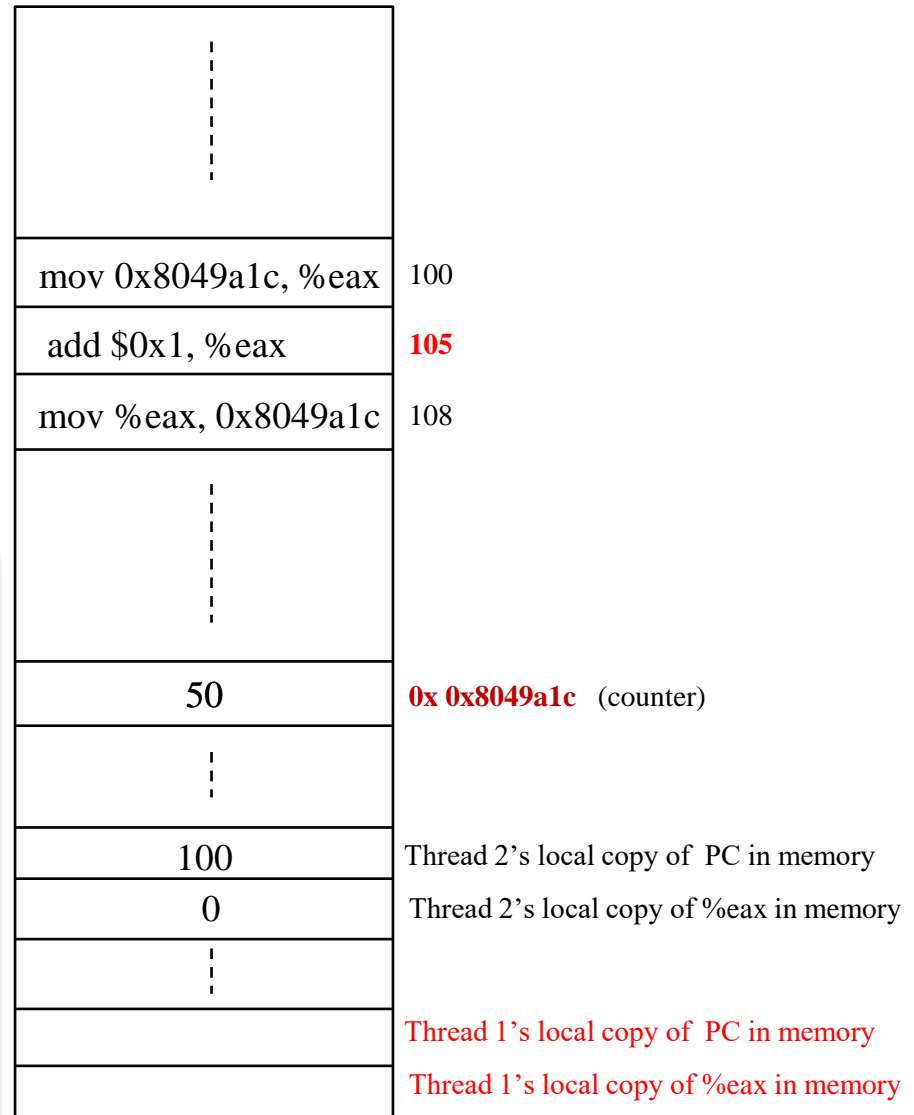
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
	<code>mov %eax, 0x8049a1c</code>		113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
	<code>mov %eax, 0x8049a1c</code>		113	51	51

# Step 4: Increase PC (pointed to the next instruction in the memory)

## CPU



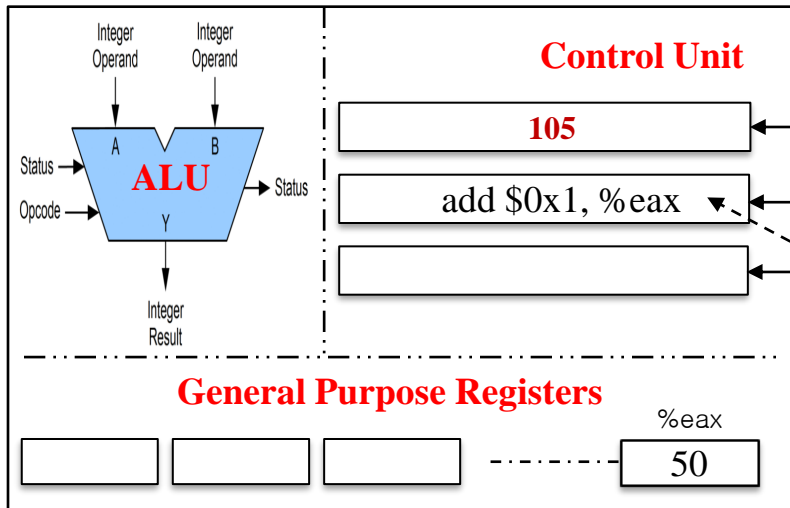
## Memory



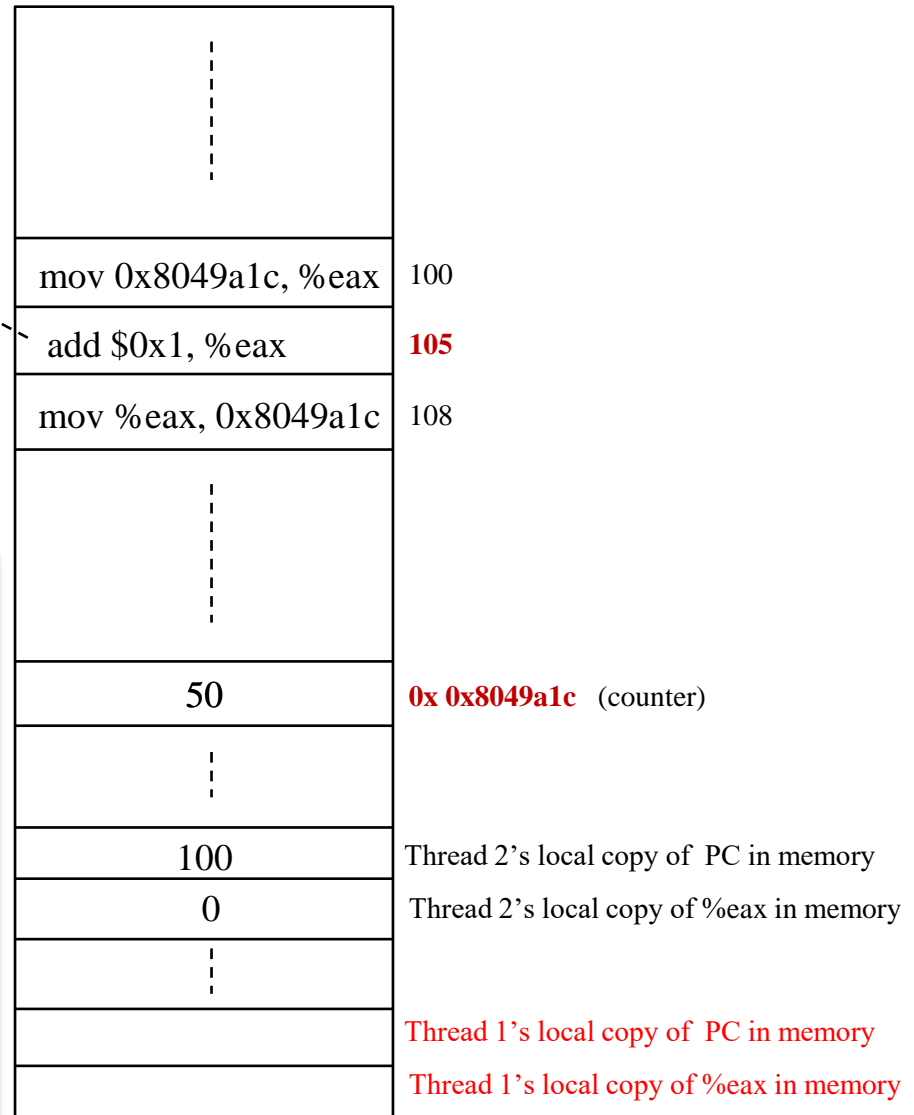
OS	Thread1	Thread2	(after instruction)		
			PC	<u>%eax</u>	counter
	<b>Initial value</b>		100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
	<code>mov %eax, 0x8049a1c</code>		113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
	<code>mov %eax, 0x8049a1c</code>		113	51	51

# Step 1: Fetch instruction from the memory (PC->Address=105)

## CPU



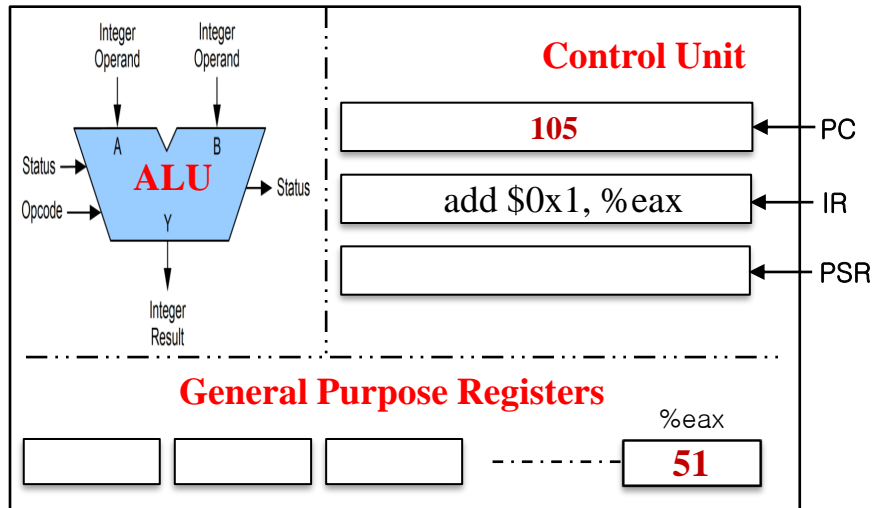
## Memory



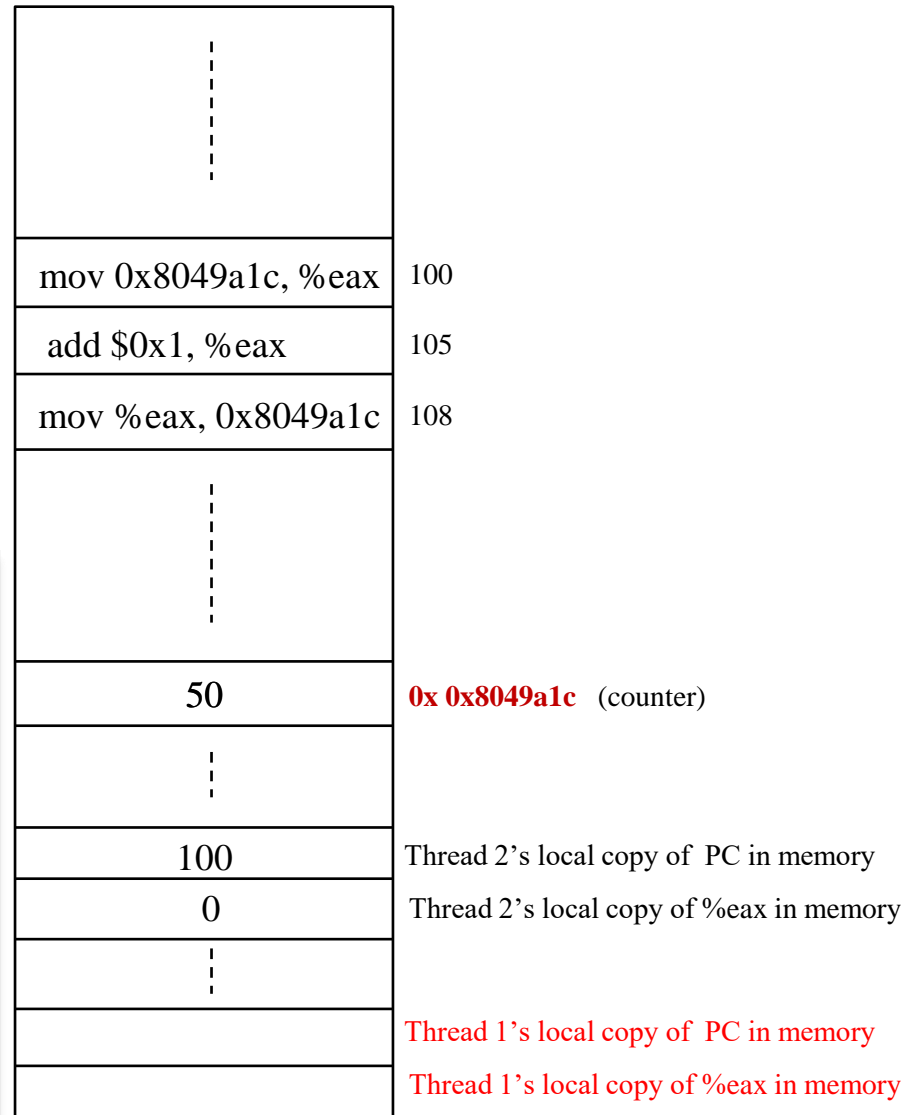
OS	Thread1	Thread2	(after instruction)		
			PC	% <u>eax</u>	counter
	<b>Initial value</b>		100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
interrupt	save T1's state				
	restore T2's state		100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
	<code>mov %eax, 0x8049a1c</code>		113	51	51
interrupt	save T2's state				
	restore T1's state		108	51	<b>51</b>
	<code>mov %eax, 0x8049a1c</code>		113	51	<b>51</b>

# Steps 2 & 3: Decode & Execution

## CPU



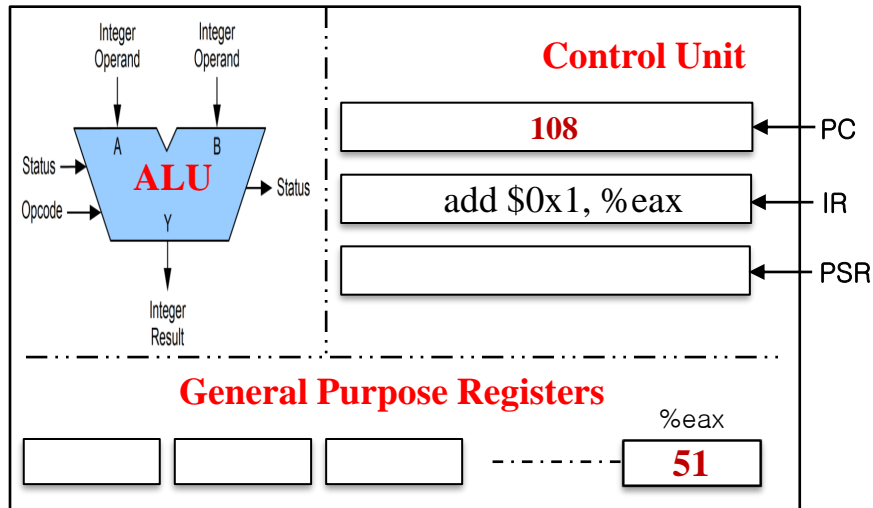
## Memory



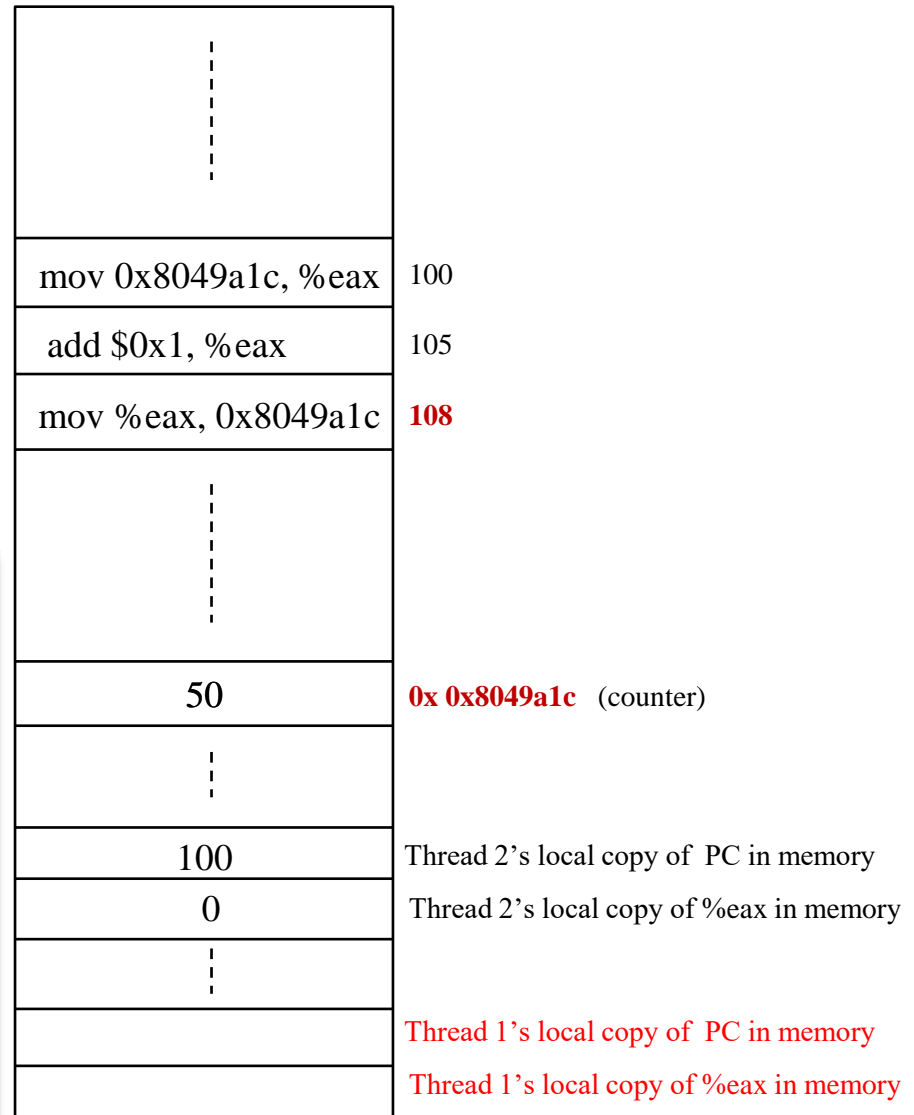
OS	Thread1	Thread2	PC	<u>%eax</u>	(after instruction) counter
	<b>Initial value</b>		100	0	50
	mov 0x8049a1c, %eax		105	50	50
	add \$0x1, %eax		108	51	50
interrupt	save T1's state				
	restore T2's state		100	0	50
	mov 0x8049a1c, %eax		105	50	50
	add \$0x1, %eax		108	51	50
	mov %eax, 0x8049a1c		113	51	51
interrupt	save T2's state				
	restore T1's state		108	51	51
	mov %eax, 0x8049a1c		113	51	51

# Step 3: Increase PC (pointed to the next instruction in the memory)

## CPU



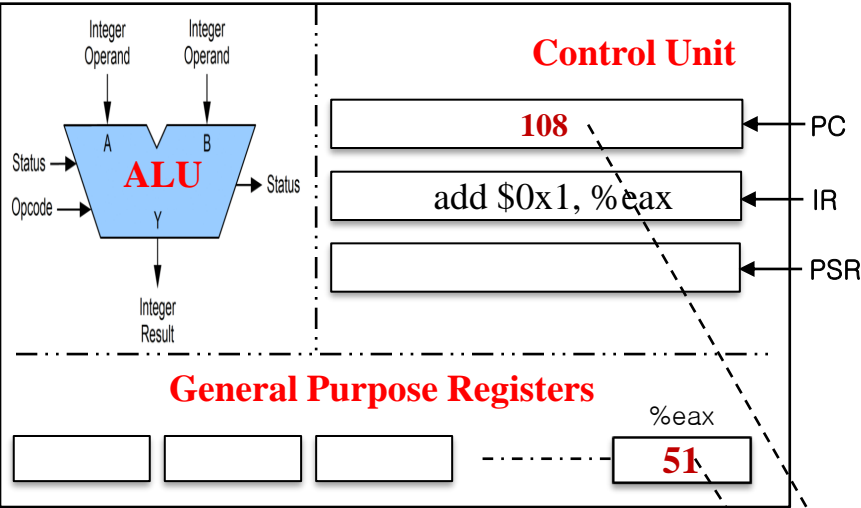
## Memory



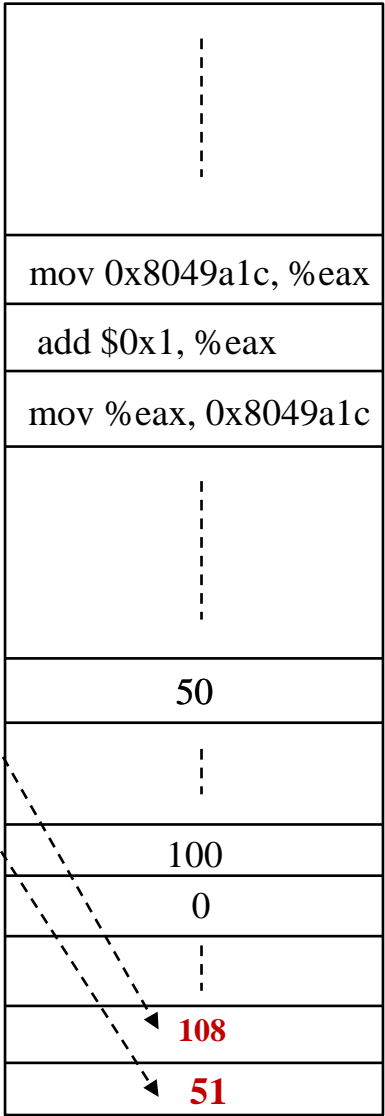
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	Initial value		100	0	50
	mov 0x8049a1c, %eax		105	50	50
	add \$0x1, %eax		108	51	50
interrupt	save T1's state				
	restore T2's state		100	0	50
	mov 0x8049a1c, %eax		105	50	50
	add \$0x1, %eax		108	51	50
	mov %eax, 0x8049a1c		113	51	51
interrupt	save T2's state				
	restore T1's state		108	51	51
	mov %eax, 0x8049a1c		113	51	51

# Interrupt occurred; Save Thread 1's state

## CPU



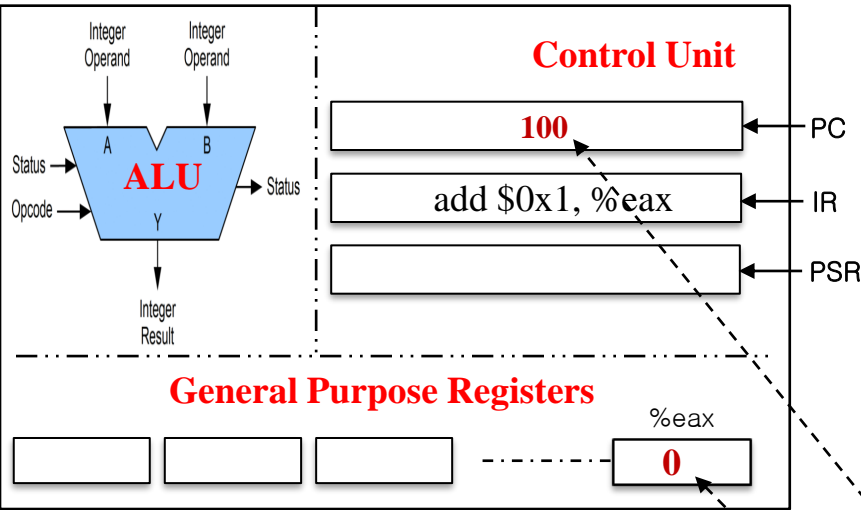
## Memory



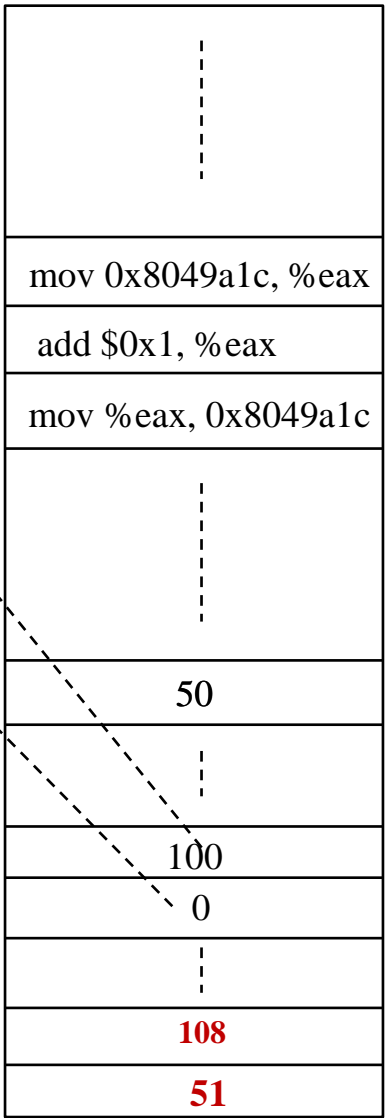
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
interrupt					
save T1's state					
restore T2's state					
			100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
	<u>mov</u> %eax, 0x8049a1c		113	51	51
interrupt					
save T2's state					
restore T1's state					
			108	51	51
	<u>mov</u> %eax, 0x8049a1c		113	51	51

# Restore Thread 2's state

## CPU



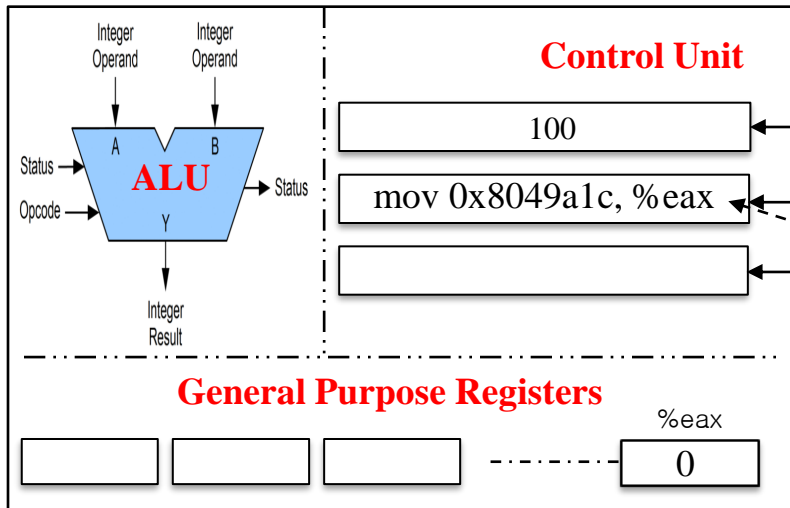
## Memory



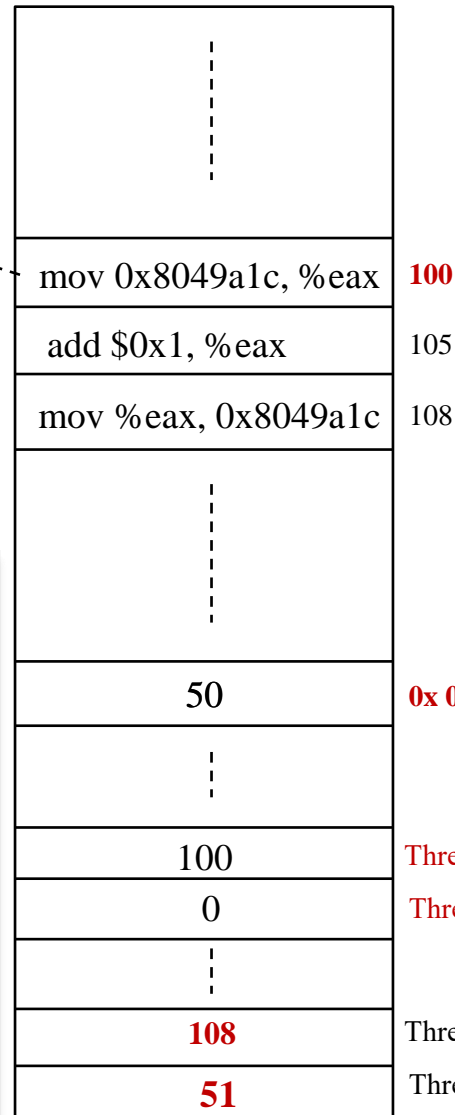
OS	Thread1	Thread2	PC	<u>%eax</u>	(after instruction) counter
	<b>Initial value</b>		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
interrupt					
	save T1's state				
	<b>restore T2's state</b>		100	0	50
		<u>mov</u> 0x8049a1c, <u>%eax</u>	105	50	50
		<u>add</u> \$0x1, <u>%eax</u>	108	51	50
		<u>mov</u> <u>%eax</u> , 0x8049a1c	113	51	51
interrupt					
	save T2's state				
	restore T1's state		108	51	51
		<u>mov</u> <u>%eax</u> , 0x8049a1c	113	51	51

# Step 1: Fetch instruction from the memory (PC->Address=100)

## CPU



## Memory

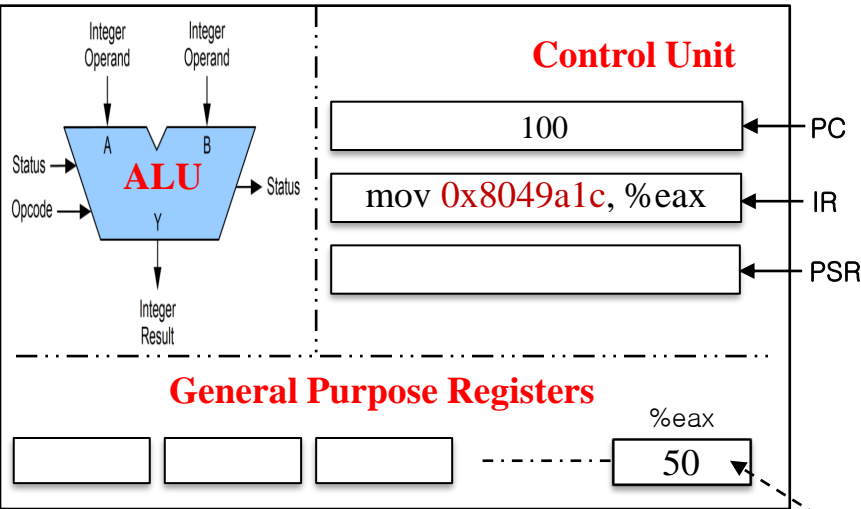


OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
interrupt	save T1's state				
	restore T2's state		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
	<u>mov</u> %eax, 0x8049a1c		113	51	51
interrupt	save T2's state				
	restore T1's state		108	51	51
	<u>mov</u> %eax, 0x8049a1c		113	51	51

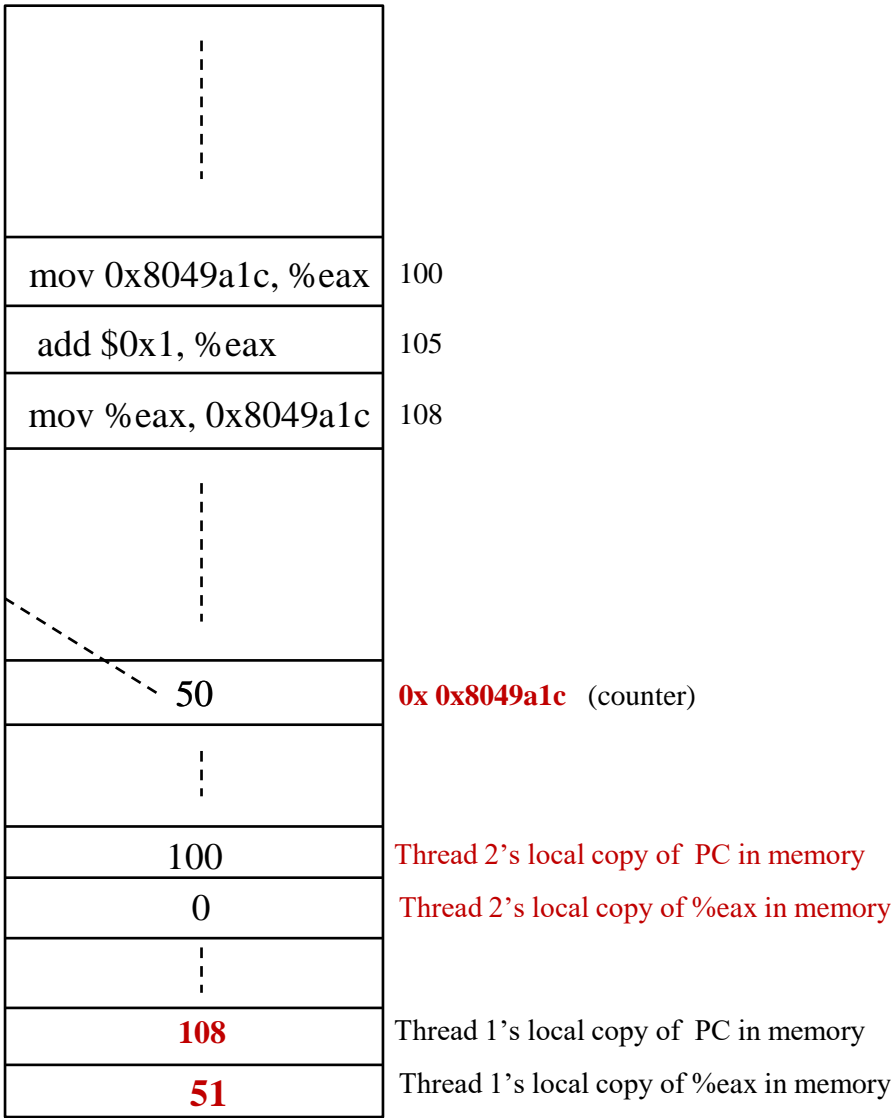


# Steps 2 & 3: Decode & Execution

## CPU



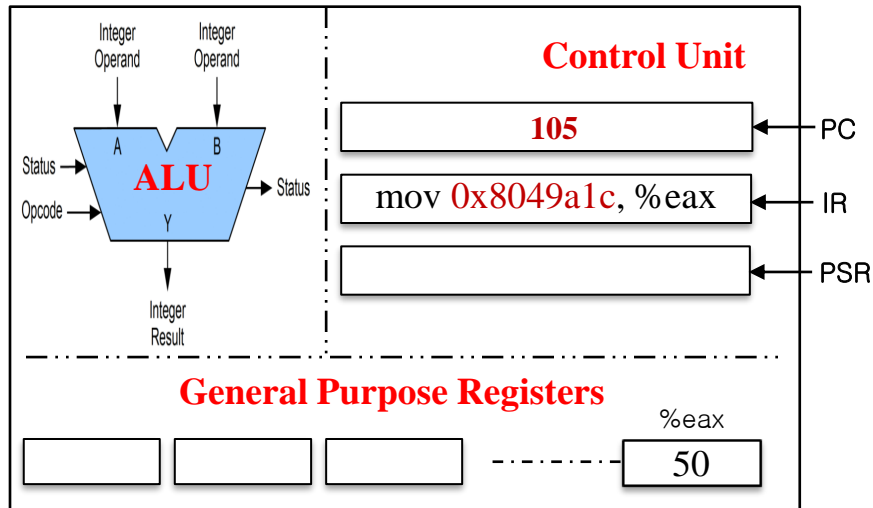
## Memory



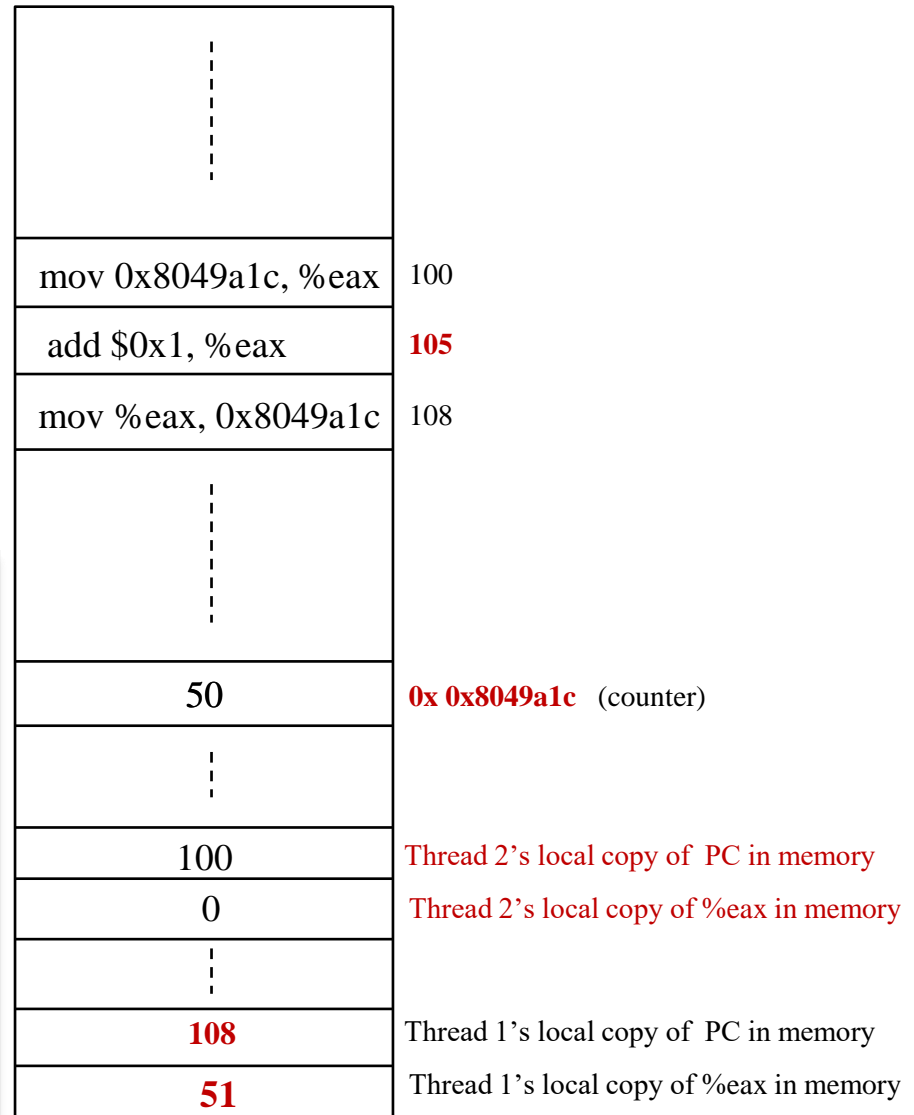
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
Initial value			100	0	50
mov 0x8049a1c, %eax			105	50	50
add \$0x1, %eax			108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
		mov 0x8049a1c, %eax	105	50	50
		add \$0x1, %eax	108	51	50
		mov %eax, 0x8049a1c	113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
		mov %eax, 0x8049a1c	113	51	51

# Step 4: Increase PC (pointed to the next instruction in the memory)

## CPU

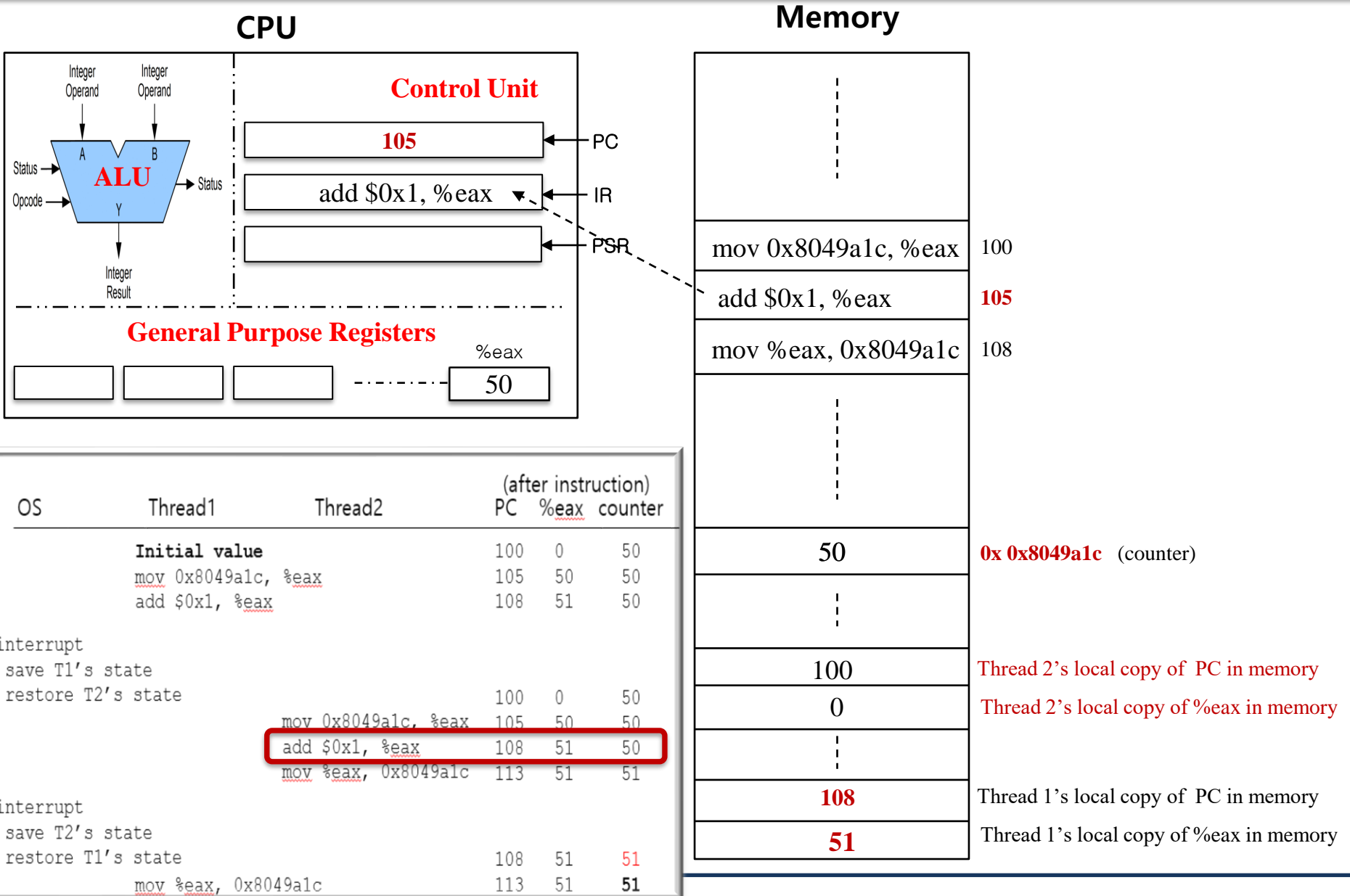


## Memory



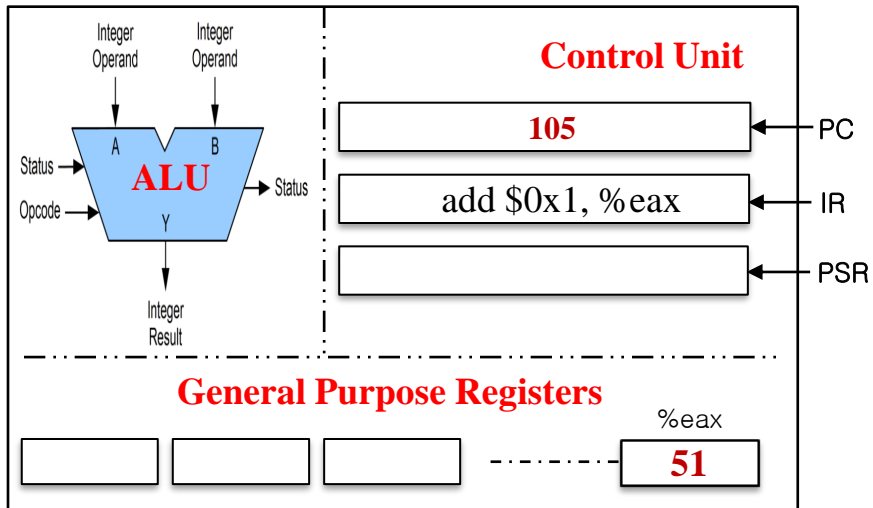
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
interrupt	save T1's state				
	restore T2's state		100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
	<code>mov %eax, 0x8049a1c</code>		113	51	51
interrupt	save T2's state				
	restore T1's state		108	51	51
	<code>mov %eax, 0x8049a1c</code>		113	51	51

## Step 1: Fetch instruction from the memory (PC->Address=105)

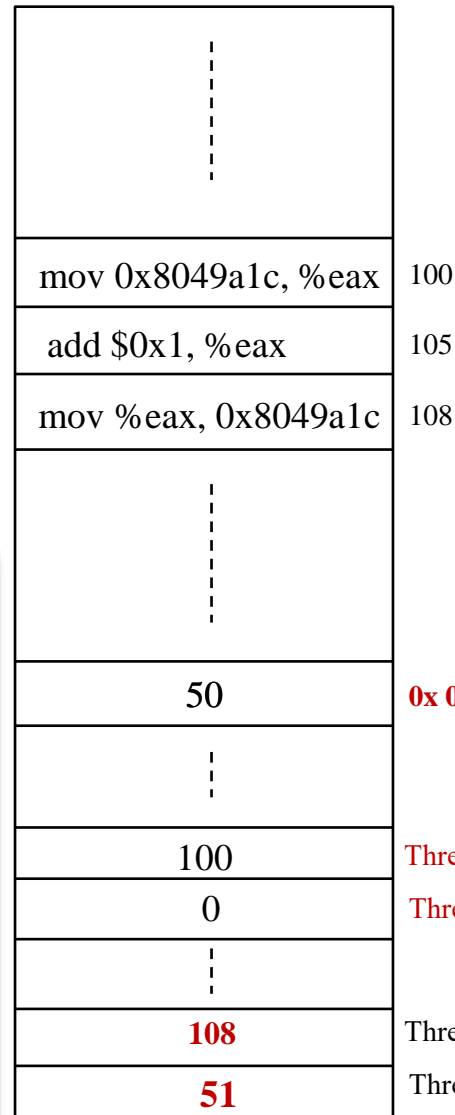


# Steps 2 & 3: Decode & Execution

## CPU



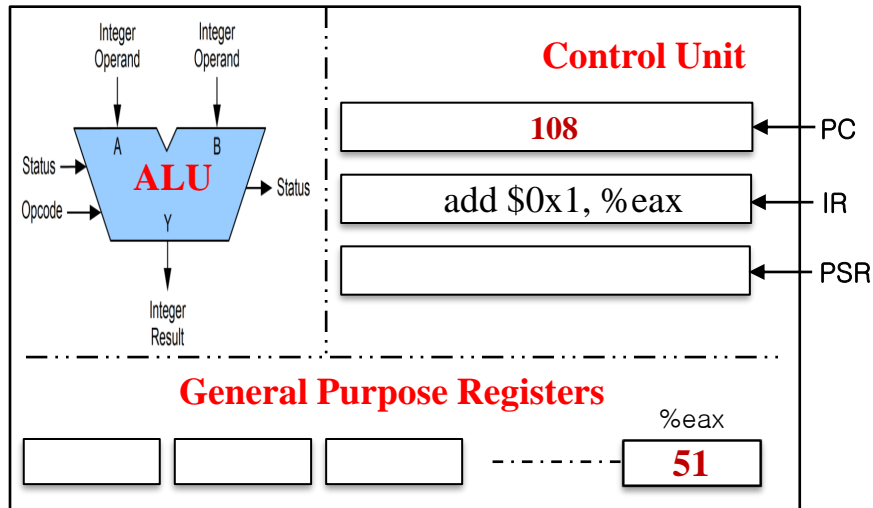
## Memory



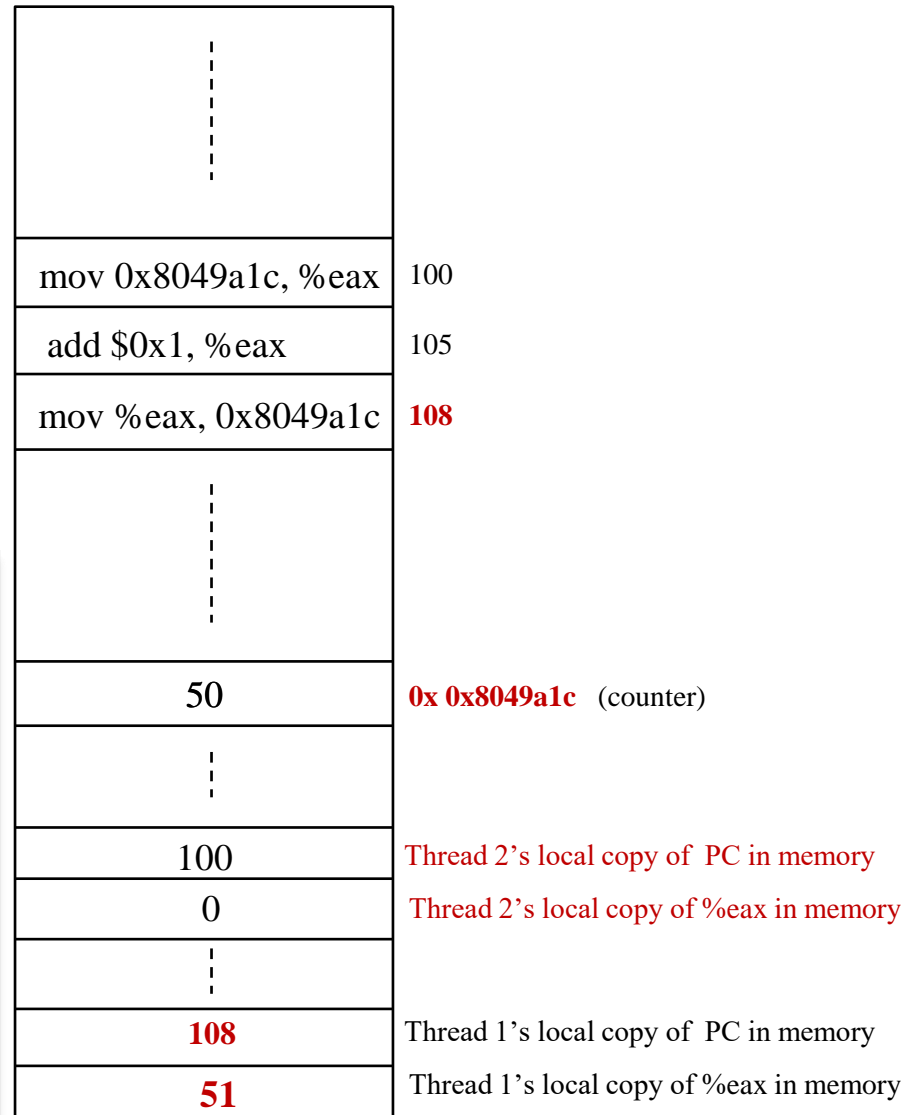
OS	Thread1	Thread2	(after instruction)		
			PC	% <u>eax</u>	counter
	<b>Initial value</b>		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
interrupt	save T1's state				
	restore T2's state		100	0	50
		<u>mov</u> 0x8049a1c, <u>%eax</u>	105	50	50
		<u>add</u> \$0x1, <u>%eax</u>	108	51	50
		<u>mov</u> <u>%eax</u> , 0x8049a1c	113	51	51
interrupt	save T2's state				
	restore T1's state		108	51	51
		<u>mov</u> <u>%eax</u> , 0x8049a1c	113	51	51

# Step 4: Increase PC (pointed to the next instruction in the memory)

## CPU



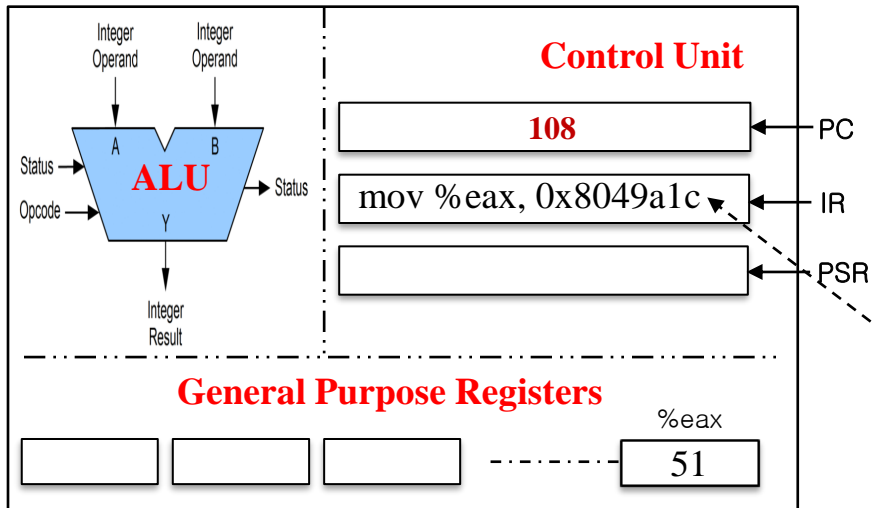
## Memory



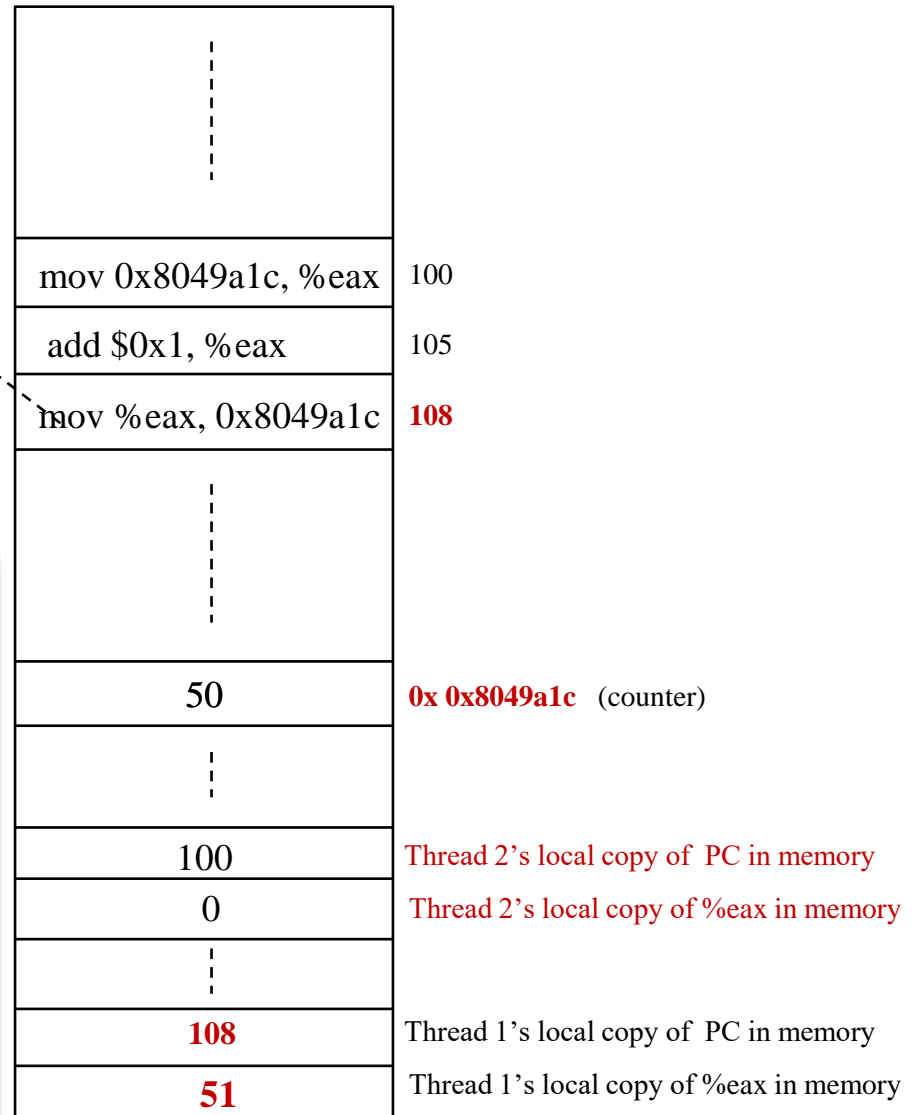
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
interrupt	save T1's state				
	restore T2's state				
			100	0	50
		<u>mov</u> 0x8049a1c, <u>%eax</u>	105	50	50
		<u>add</u> \$0x1, <u>%eax</u>	108	51	50
		<u>mov</u> <u>%eax</u> , 0x8049a1c	113	51	51
interrupt	save T2's state				
	restore T1's state				
			108	51	51
	<u>mov</u> <u>%eax</u> , 0x8049a1c		113	51	51

# Step 1: Fetch instruction from the memory (PC->Address=108)

## CPU



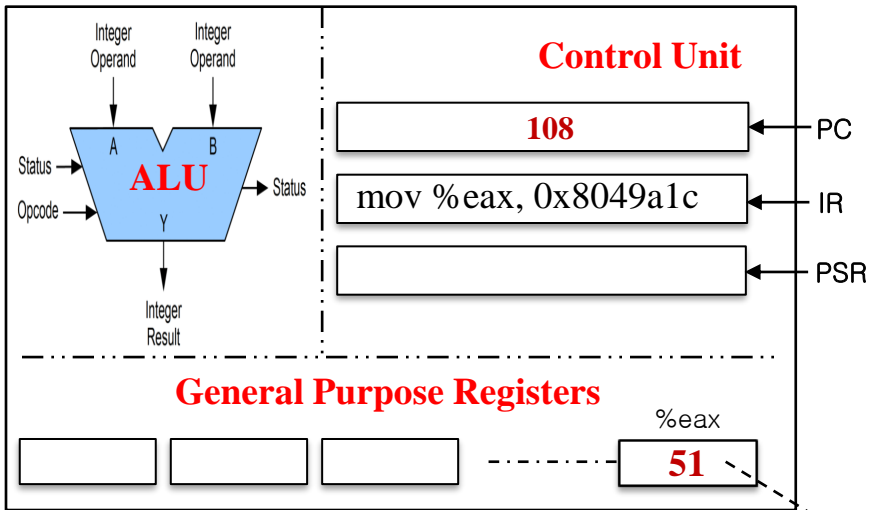
## Memory



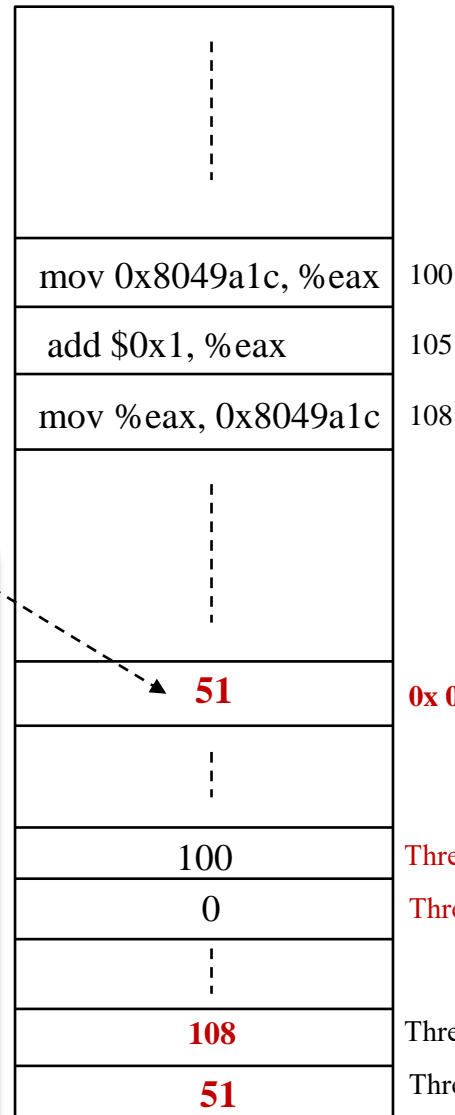
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
interrupt	Initial value		100	0	50
	mov 0x8049a1c, %eax		105	50	50
	add \$0x1, %eax		108	51	50
interrupt	save T1's state				
	restore T2's state		100	0	50
		mov 0x8049a1c, %eax	105	50	50
		add \$0x1, %eax	108	51	50
interrupt		mov %eax, 0x8049a1c	113	51	51
	save T2's state				
	restore T1's state		108	51	51
		mov %eax, 0x8049a1c	113	51	51

# Steps 2 & 3: Decode & Execution

## CPU



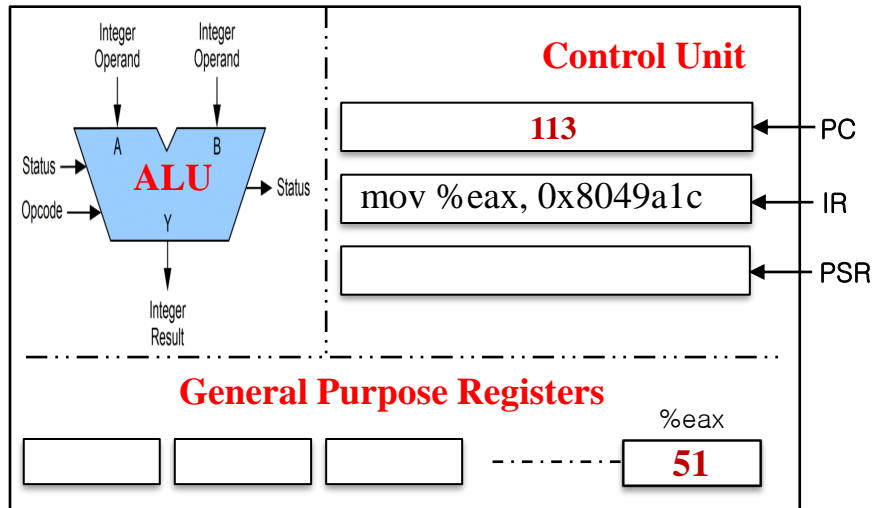
## Memory



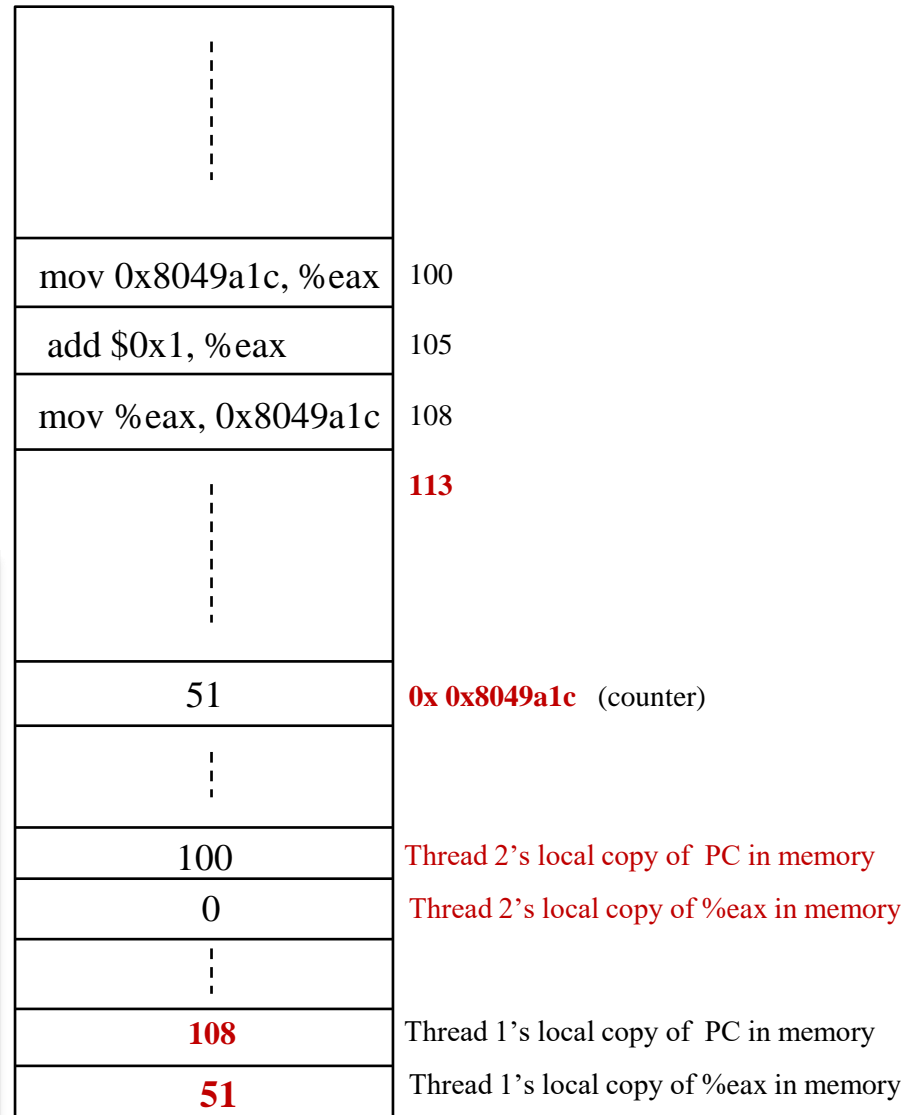
OS	Thread1	Thread2	(after instruction)		
			PC	<u>%eax</u>	counter
	<b>Initial value</b>		100	0	50
	<code>mov 0x8049a1c, <u>%eax</u></code>		105	50	50
	<code>add \$0x1, <u>%eax</u></code>		108	51	50
interrupt					
save T1's state					
restore T2's state					
			100	0	50
		<code>mov 0x8049a1c, <u>%eax</u></code>	105	50	50
		<code>add \$0x1, <u>%eax</u></code>	108	51	50
		<code><u>mov %eax, 0x8049a1c</u></code>	113	51	51
interrupt					
save T2's state					
restore T1's state					
			108	51	51
		<code><u>mov %eax, 0x8049a1c</u></code>	113	51	51

# Step 4: Increase PC (pointed to the next instruction in the memory)

## CPU



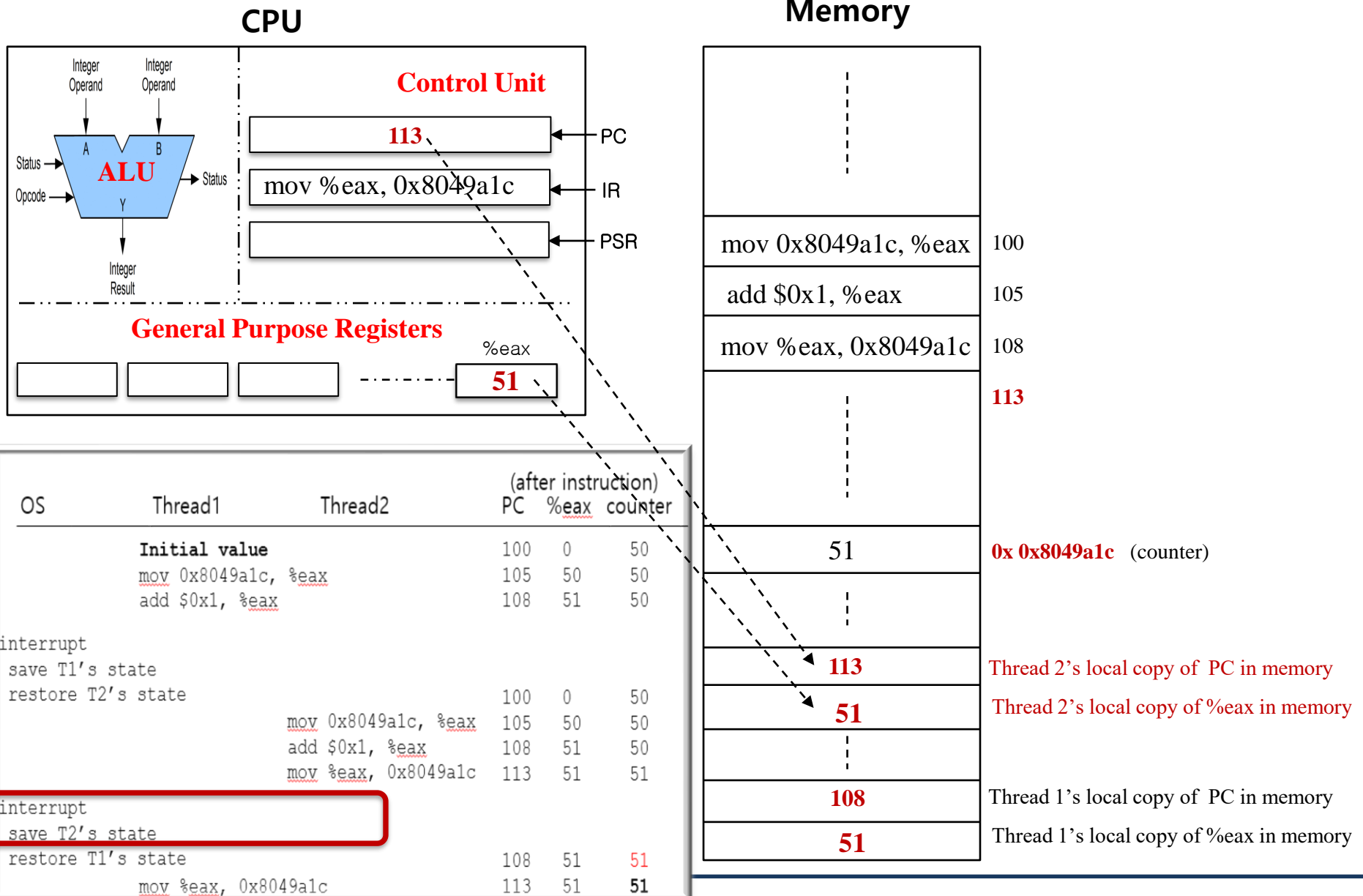
## Memory



OS	Thread1	Thread2	(after instruction)		
			PC	<u>%eax</u>	counter
	<b>Initial value</b>		100	0	50
	<code>mov 0x8049a1c, <u>%eax</u></code>		105	50	50
	<code>add \$0x1, <u>%eax</u></code>		108	51	50
interrupt	save T1's state				
	restore T2's state				
			100	0	50
	<code>mov 0x8049a1c, <u>%eax</u></code>		105	50	50
	<code>add \$0x1, <u>%eax</u></code>		108	51	50
	<code>mov <u>%eax</u>, 0x8049a1c</code>		113	51	51
interrupt	save T2's state				
	restore T1's state				
			108	51	51
	<code>mov <u>%eax</u>, 0x8049a1c</code>		113	51	51

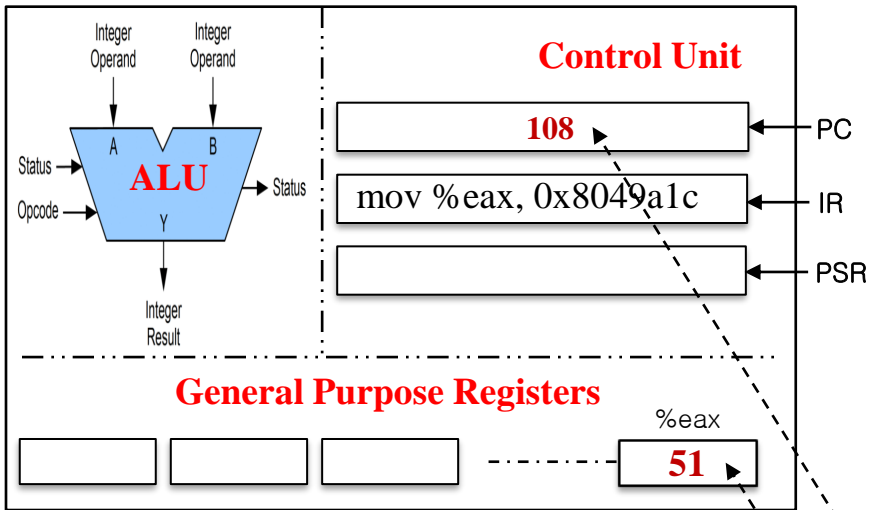


## Interrupt occurred; Save Thread 2's state

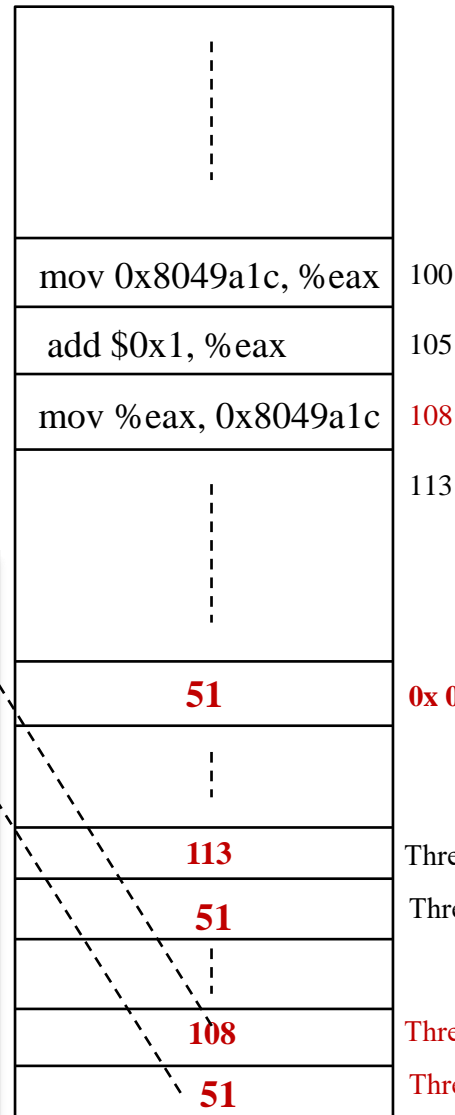


# Restore Thread 1's state

## CPU



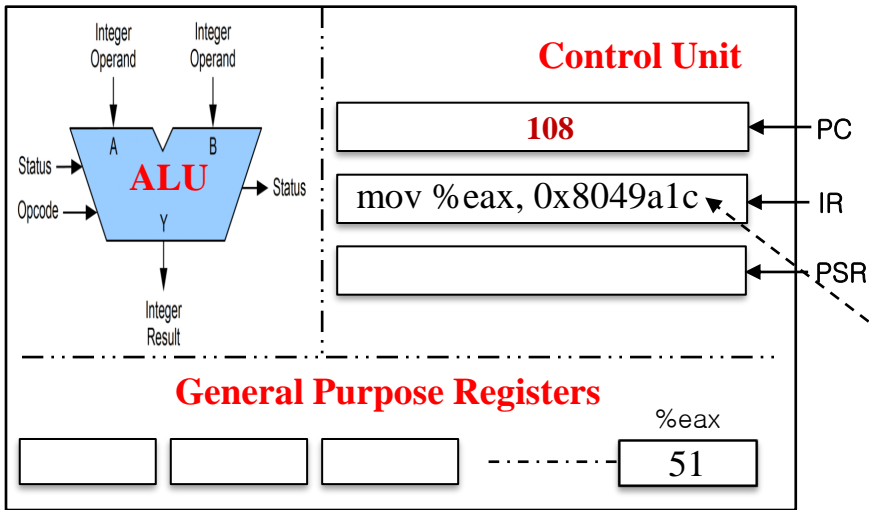
## Memory



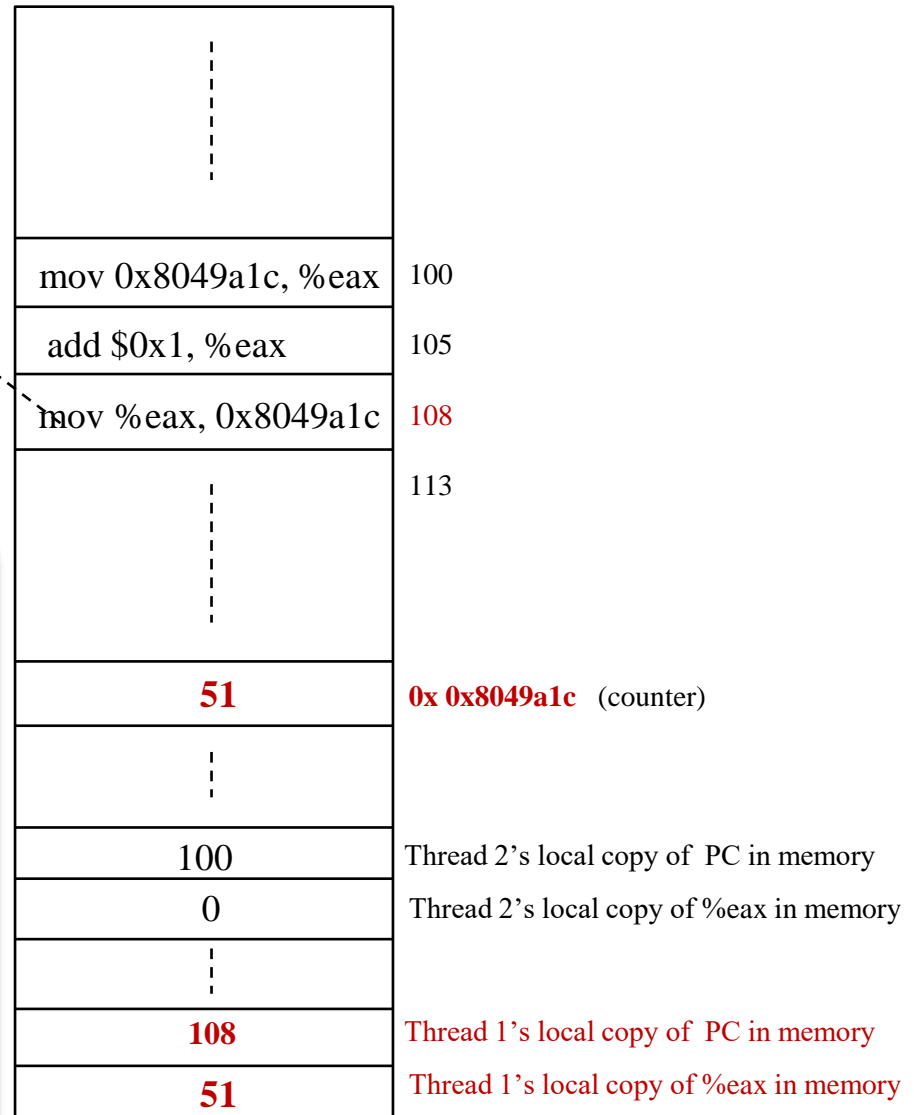
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
	<code>mov %eax, 0x8049a1c</code>		113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
	<code>mov %eax, 0x8049a1c</code>		113	51	51

# Step 1: Fetch instruction from the memory (PC->Address=108)

## CPU



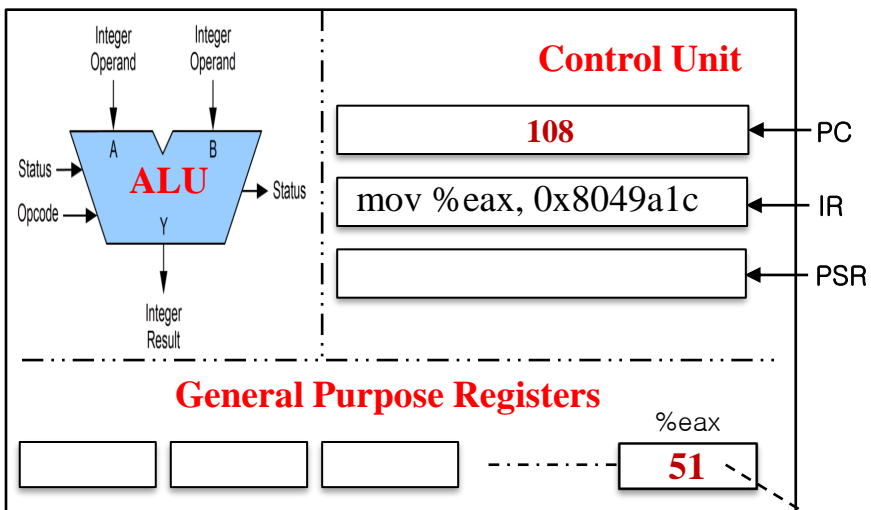
## Memory



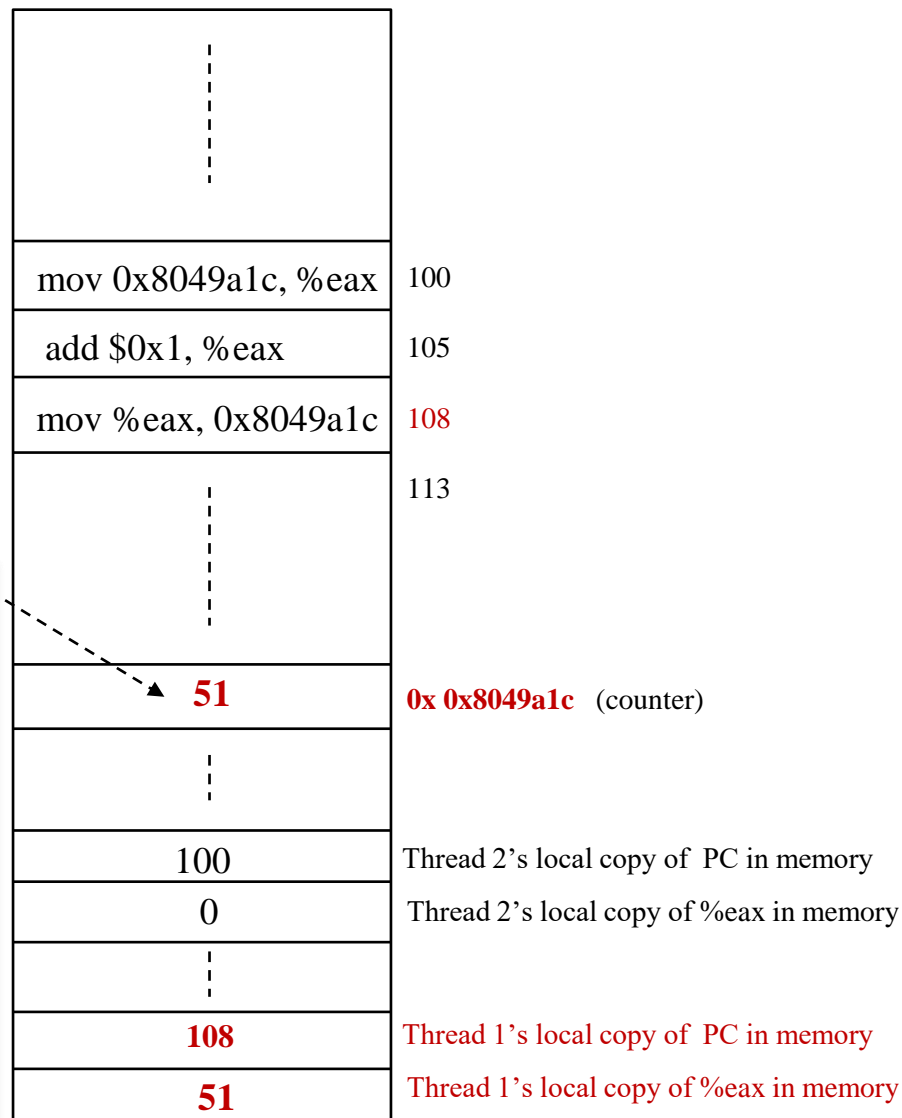
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
	<u>mov</u> <u>%eax</u> , 0x8049a1c		113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
	<u>mov</u> <u>%eax</u> , 0x8049a1c		113	51	51

# Step 2 & 3: Decode & Execution

## CPU



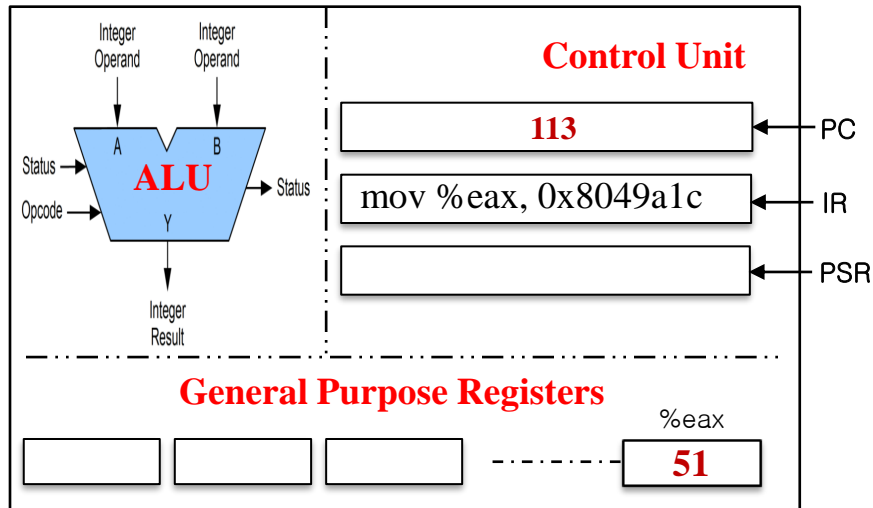
## Memory



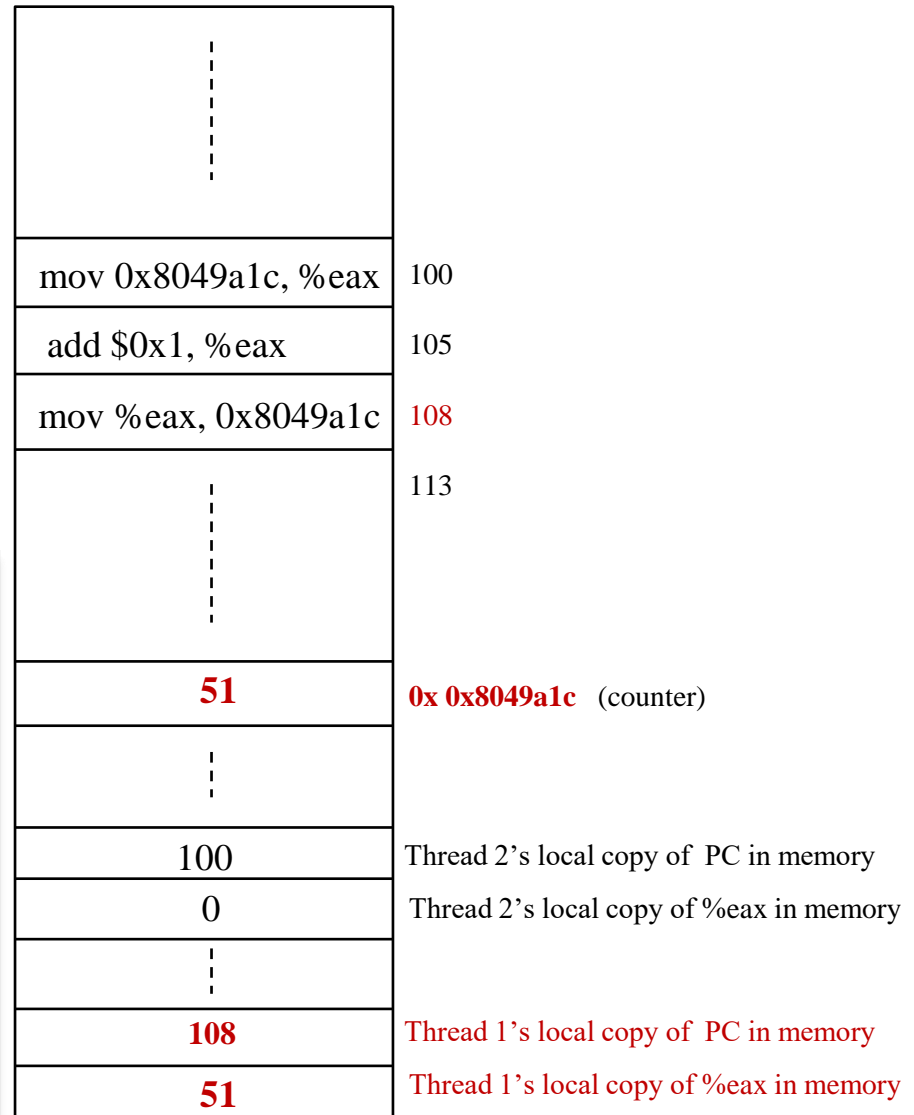
OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
	<code>mov 0x8049a1c, %eax</code>		105	50	50
	<code>add \$0x1, %eax</code>		108	51	50
	<code>mov %eax, 0x8049a1c</code>		113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
	<code>mov %eax, 0x8049a1c</code>		113	51	51

# Step 4: Increase PC (pointed to the next instruction in the memory)

## CPU



## Memory



OS	Thread1	Thread2	(after instruction)		
			PC	%eax	counter
	<b>Initial value</b>		100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
interrupt					
save T1's state					
restore T2's state			100	0	50
	<u>mov</u> 0x8049a1c, <u>%eax</u>		105	50	50
	<u>add</u> \$0x1, <u>%eax</u>		108	51	50
	<u>mov</u> <u>%eax</u> , 0x8049a1c		113	51	51
interrupt					
save T2's state					
restore T1's state			108	51	51
	<u>mov</u> <u>%eax</u> , 0x8049a1c		113	51	51

# Persistence

- ❑ Devices such as DRAM store values in a volatile.
- ❑ *Hardware* and *software* are needed to store data **persistently**.
  - ◆ **Hardware:** I/O device such as a hard drive, solid-state drives(SSDs)
  - ◆ **Software:**
    - File system manages storage devices (hard drives, SSDs, etc.).
    - File system is responsible for storing any files that users create.
      - Regular files
      - Directory files
      - Special files (e.g. devices – keyboards, monitors, etc.)
      - etc.

## Persistence (Cont.)

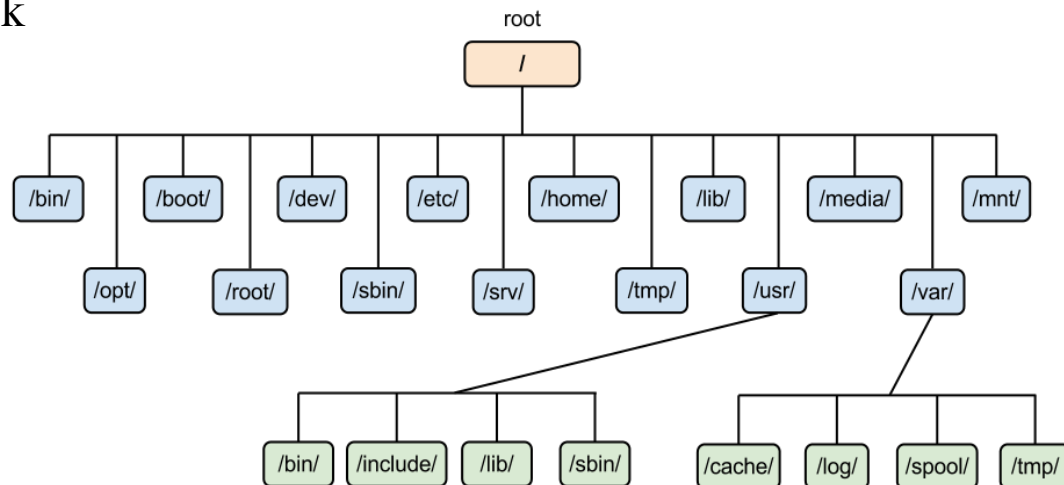
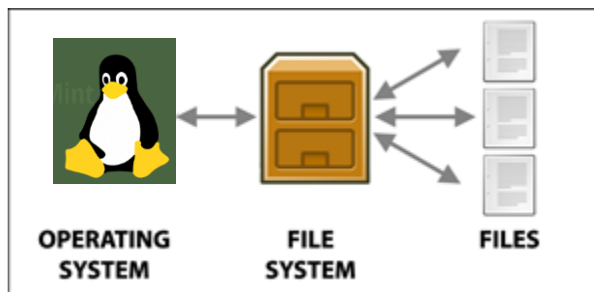
- Create a file (myfile) that contains the string “hello world” (fs.c)

```
1      #include <stdio.h>
2      #include <unistd.h>
3      #include <assert.h>
4      #include <fcntl.h>
5      #include <sys/types.h>
6
7      int
8      main(int argc, char *argv[])
9      {
10         int fd = open("myfile", O_WRONLY | O_CREAT
                        | O_TRUNC, S_IRWXU);
11         assert(fd > -1);
12         int rc = write(fd, "hello world\n", 13);
13         assert(rc == 13);
14         close(fd);
15         return 0;
16     }
```

`open()`, `write()`, and `close()` system calls are routed to the part of OS called the file system, which handles the requests

# Persistence (Cont.)

- ❑ What OS does in order to write data to the disk?
  - ◆ Store file meta data in the disk (file name, creation time, etc.)
  - ◆ Figure out **where** on the disk this new data will reside
  - ◆ **Issue I/O** requests to the underlying storage device
- ❑ File system handles system crashes during write.
  - ◆ **Journaling** or **copy-on-write**
  - ◆ Carefully ordering writes to disk





# Design Goals

- ❑ Build up **abstraction**
  - ◆ Make the system convenient and easy to use.
- ❑ Provide **high performance**
  - ◆ Minimize the overhead of the OS.
  - ◆ OS must strive to provide virtualization without excessive overhead.
- ❑ **Protection** between applications
  - ◆ Isolation: Bad behavior of one does not harm other and the OS itself.
- ❑ High degree of **reliability**
  - ◆ The OS must also run non-stop.
- ❑ Other issues: Energy-efficiency, Security, Mobility

# Summary

- ❑ Computer architecture (Von Neumann): CPU, Memory, and IO devices
- ❑ OS main functions
  - ◆ **Manage resources via virtualization**
    - CPU, Memory, IO devices (e.g. storage (e.g. hard drives), keyboard, etc.)
  - ◆ **Provide services via system calls**
    - Process (run programs), memory management, file, etc.
- ❑ Design goals
  - ◆ Abstraction, high performance, protection, reliability etc.
- ❑ Related Chapter: [Chapter 2](#) (2.1 – 2.5)
- ❑ Next: User-level programming using system calls (process, memory, file)
  - ◆ [Chapter 5 \(Process\)](#), [Chapter 14 \(Memory\)](#), [Chapter 39 \(Files\)](#)
  - ◆ Self study: [Lab tutorial](#)