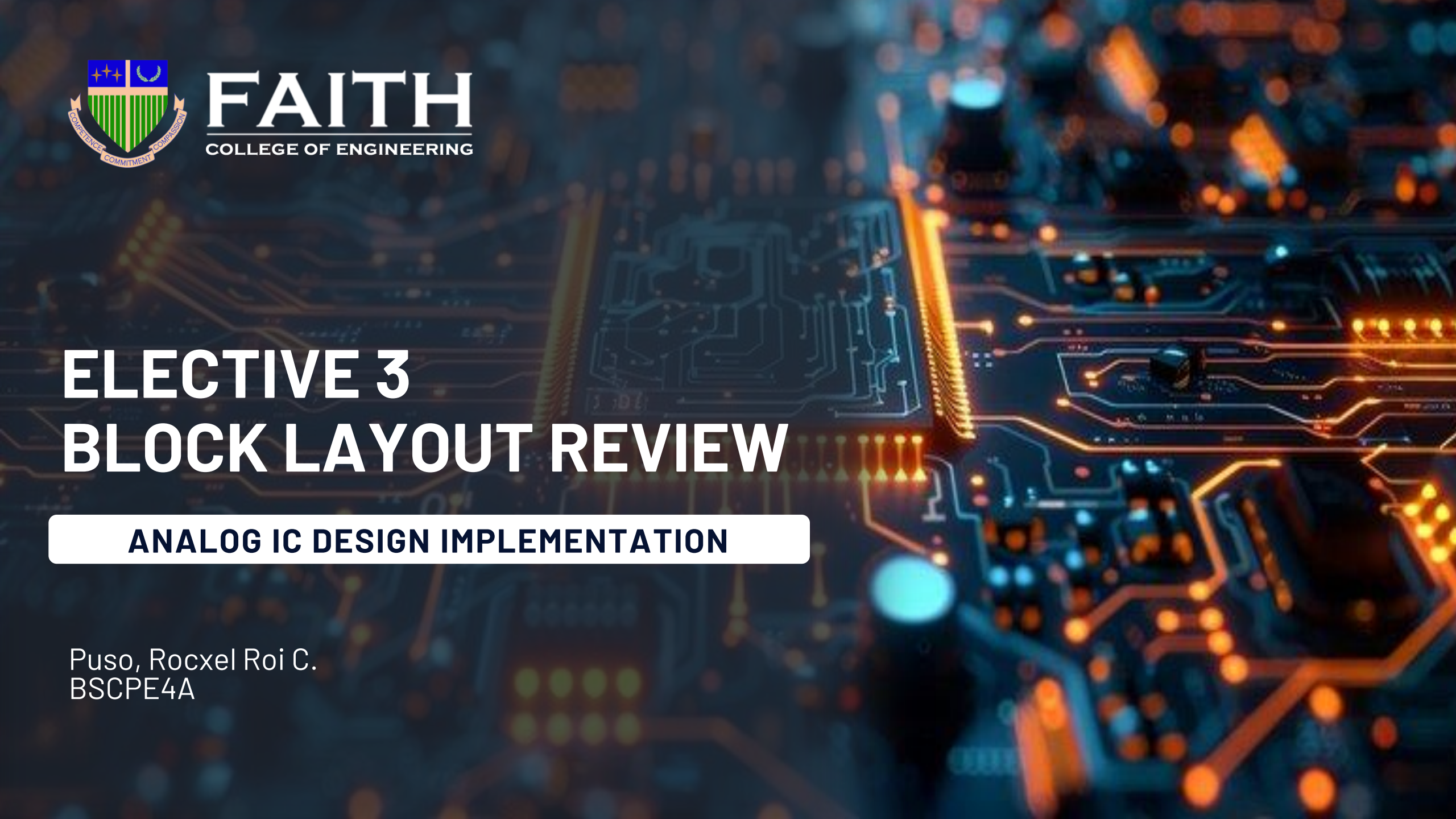

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ELECTIVE 3
BLOCK LAYOUT REVIEW

ANALOG IC DESIGN IMPLEMENTATION

Puso, Rocxel Roi C.
BSCPE4A

OUTLINE

- General Block Layout Guidelines
- Block Details
- General Layout Implementation
- Layout Takeaways
- Question and Answers

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General Block Layout Guidelines

ANALOG IC DESIGN IMPLEMENTATION – LAYOUT REVIEW

GENERAL BLOCK LAYOUT GUIDELINES

- Allotted Area: X = 750λ (Maximum) , Y = variable
- Use 24λ for main power and Ground line widths.
- Match devices properly.
- Avoid routing on active devices.
- Do not use poly when routing.
- Place pins at block edges.
- Keep the layout compact and the shape as regular as possible.
- Implement double via when routing.
- Implement double contact rows for Back gate.
- Use side shield.
- Create Dummies if applicable.
- Layout should be verified. (DRC and LVS).

OTHER LAYOUT CONSIDERATIONS

- Uniform Metal Orientation
- Avoid intersecting input and output lines
- Instances Label
- Same Size, Shape, Structure, Temperature, Orientation and Surroundings
- Close to minimum distances/Abutment
- Common Centroid Geometry: Cross-Quad/Interdigitation
- Non-Minimum Size Device

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Block Details

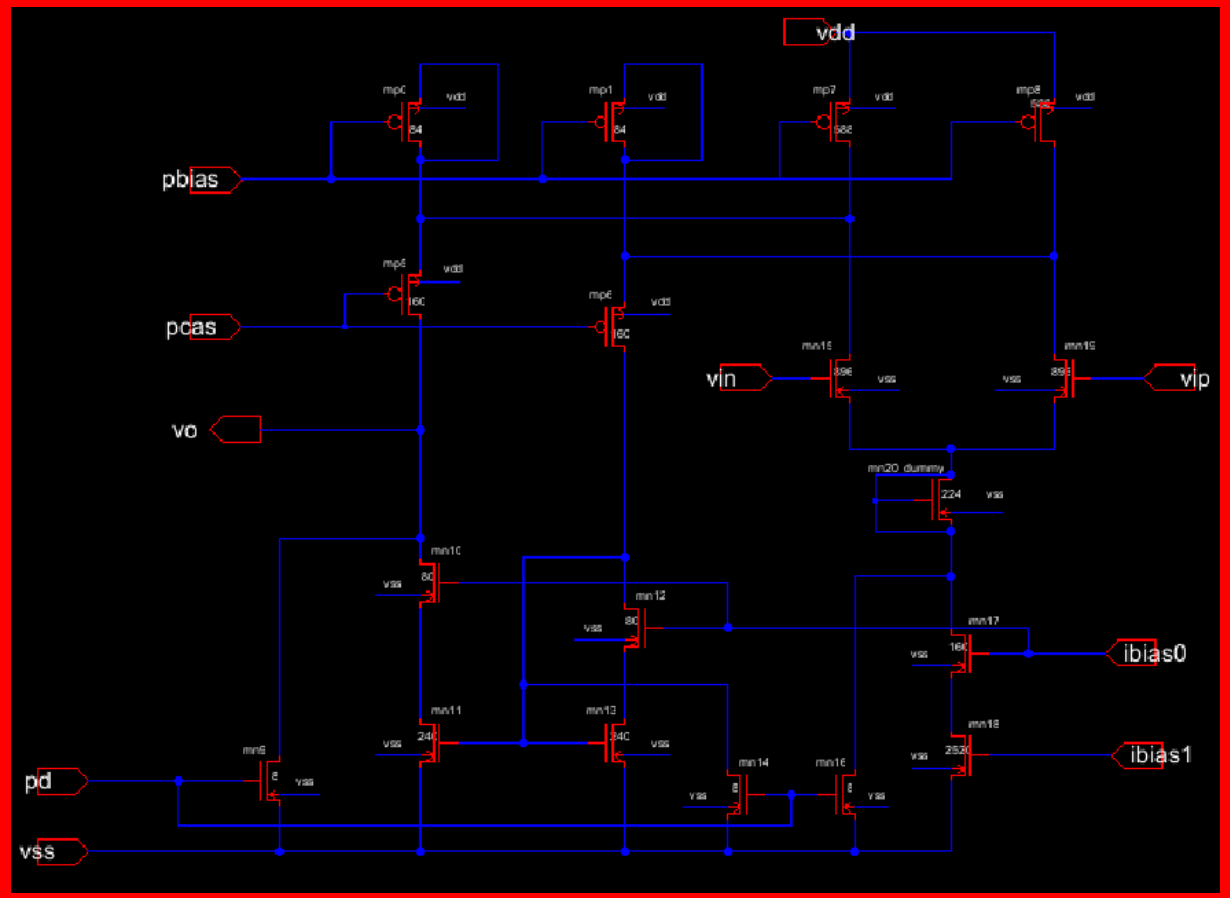
ANALOG IC DESIGN IMPLEMENTATION – LAYOUT REVIEW

BLOCK DETAILS

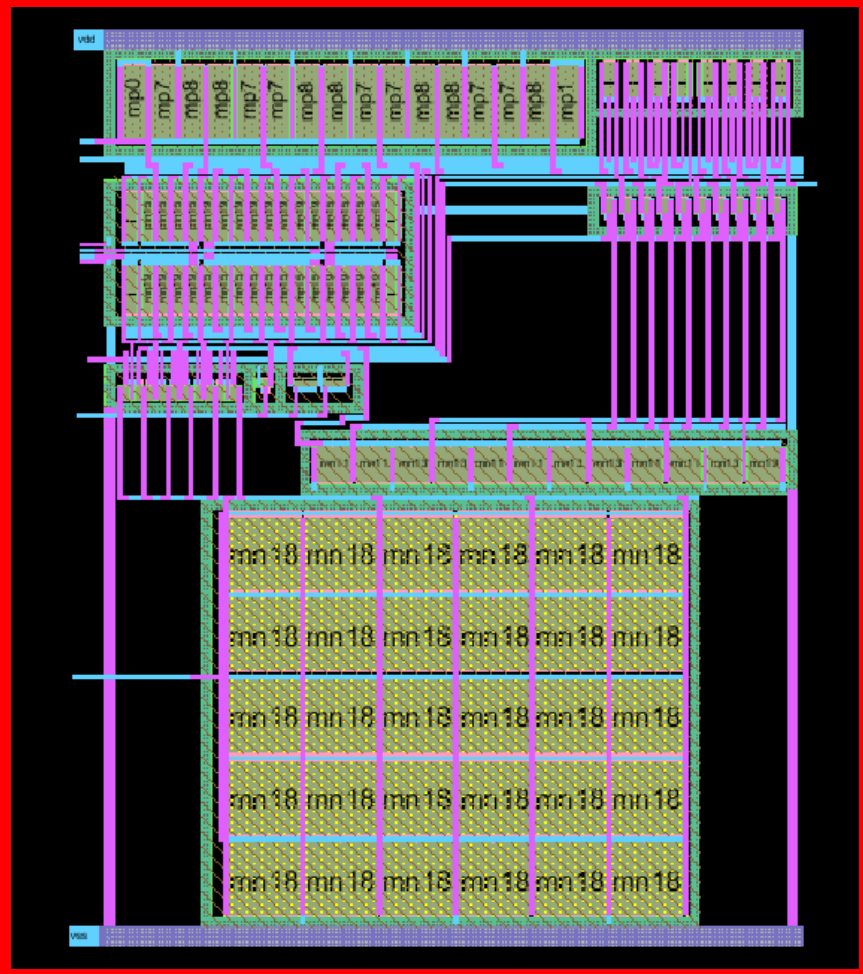
Block Name	**hfrcosc_comp_folded_Puso**
Circuit Name	*Comparator using Folded Cascode Amplifier*
Actual Area	X = 880λ , Y = 1080.5λ
Verifications	*DRC, NCC, ERC(ANTENNA, WELLS)*

Schedule (3 hrs per ECEMIC3 Schedule)						
10 Nov 2023	17 Nov 2023	24 Nov 2023	28 Nov 2023	1 Dec 2023	5 Dec 2023	12 Dec 2023
Placement	Placement	Placement	Placement	Placement	Placement/Routing	PPT

BLOCK DETAILS

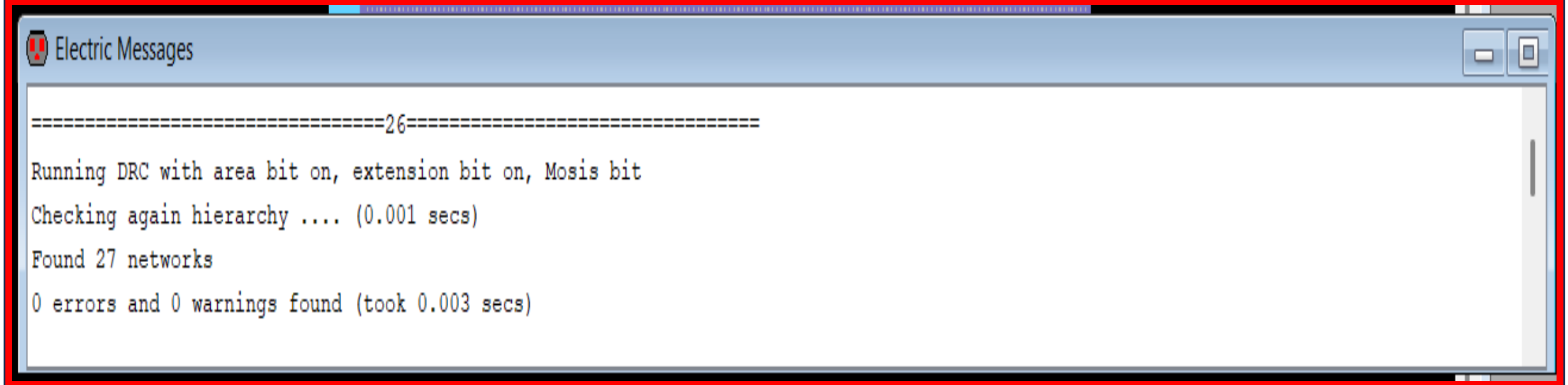


Schematic View



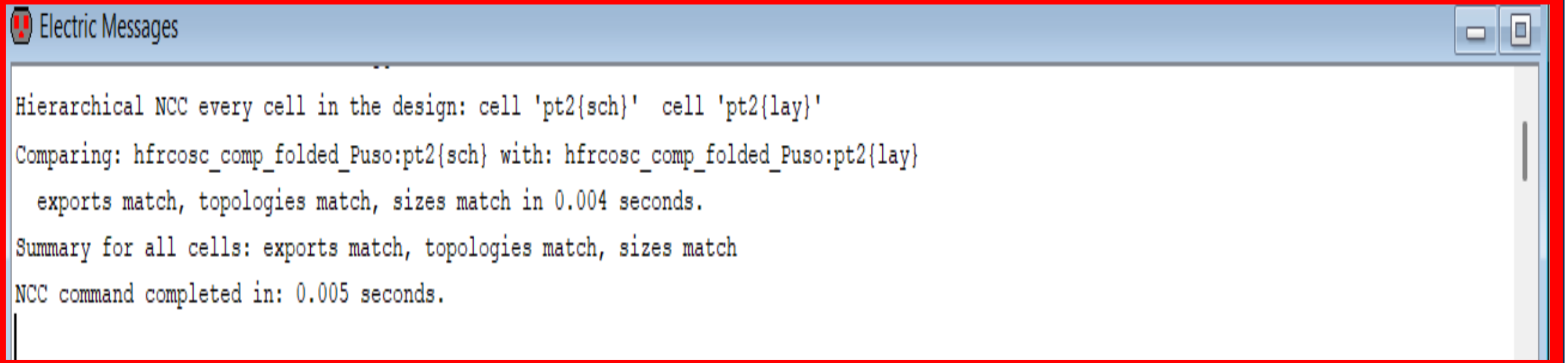
Layout View

Verification Job : DRC



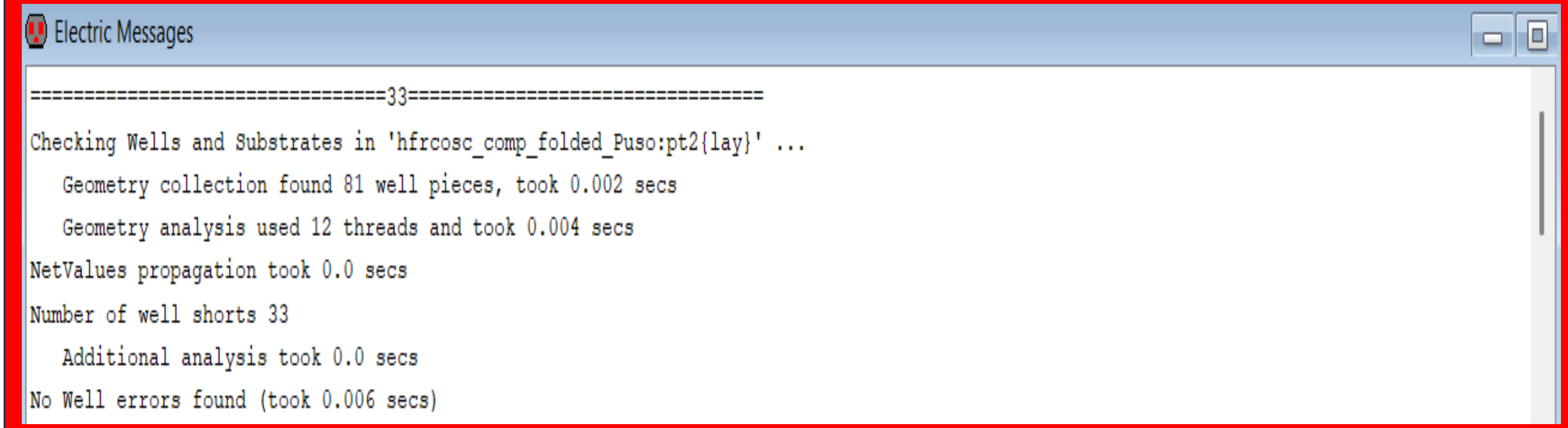
DRC RESULTS

Verification Job : NCC(LVS)



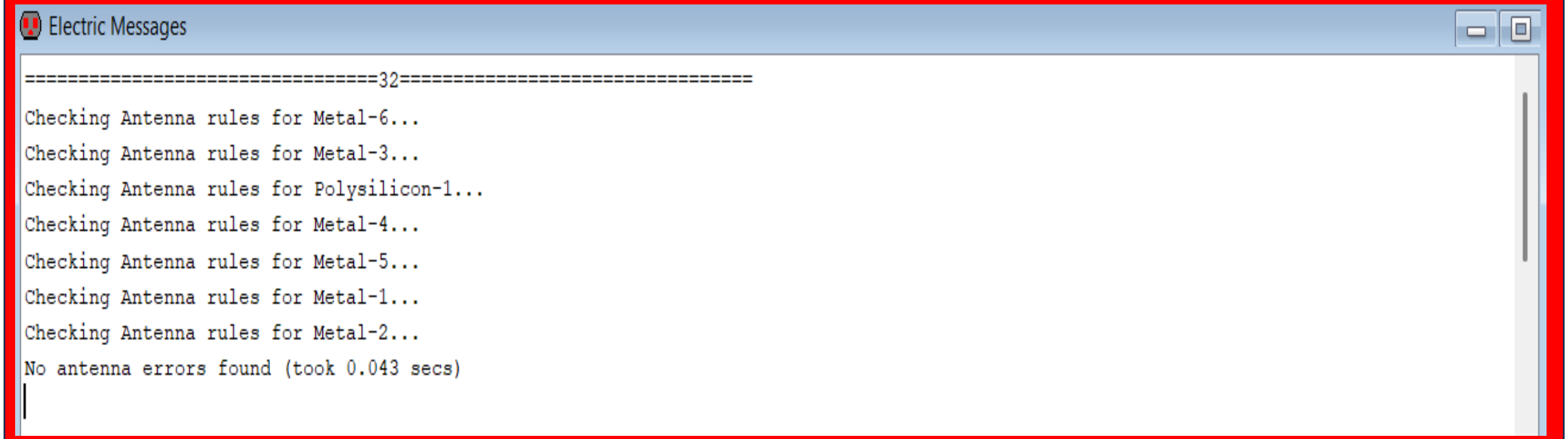
NCC RESULTS

Verification Job : ERC



ERC RESULTS

Verification Job : ANTENNA CHECK



ANTENNA CHECK RESULTS

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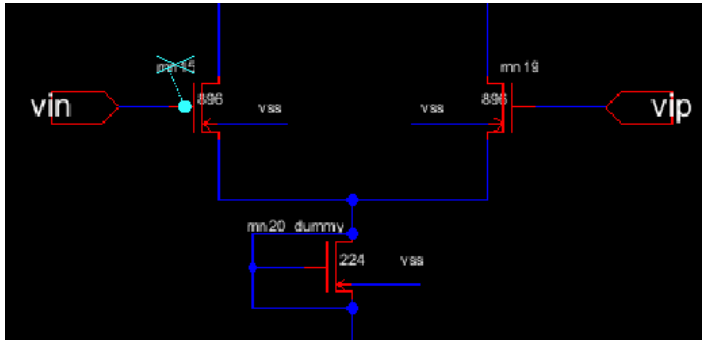
General Layout Implementation

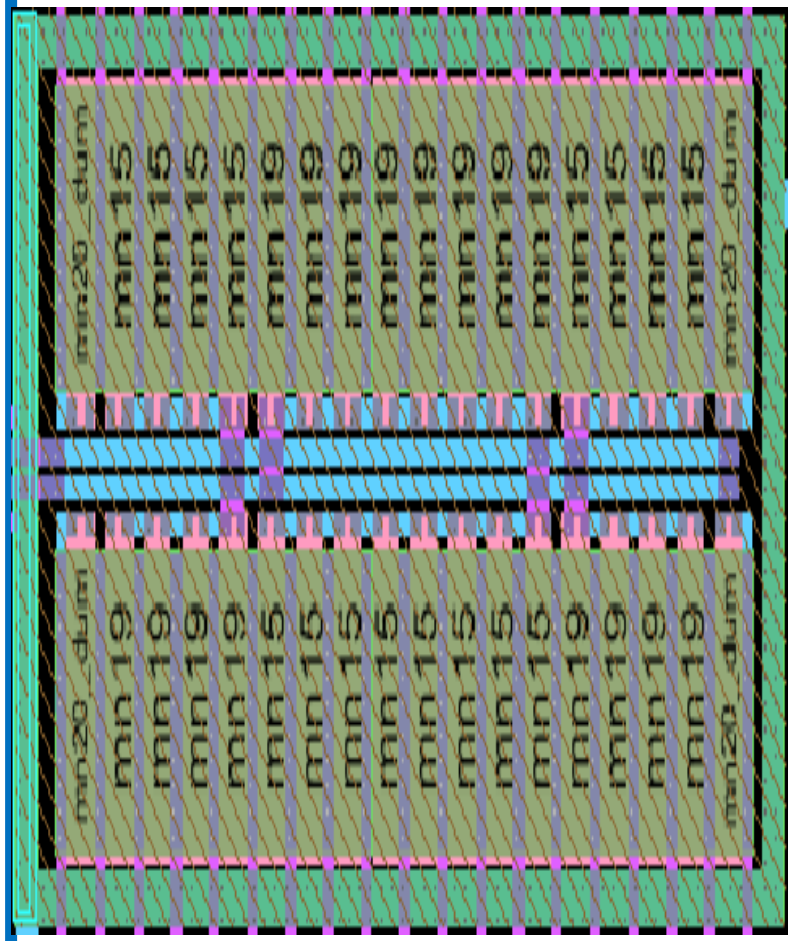
ANALOG IC DESIGN IMPLEMENTATION – LAYOUT REVIEW

How I Layout my Differential Pairs : PLACEMENT

Matching Guidelines:
Cross Quad
Shared Diffusion
Surround Dummies
Enclosed Guardring



Schematic View



Layout View

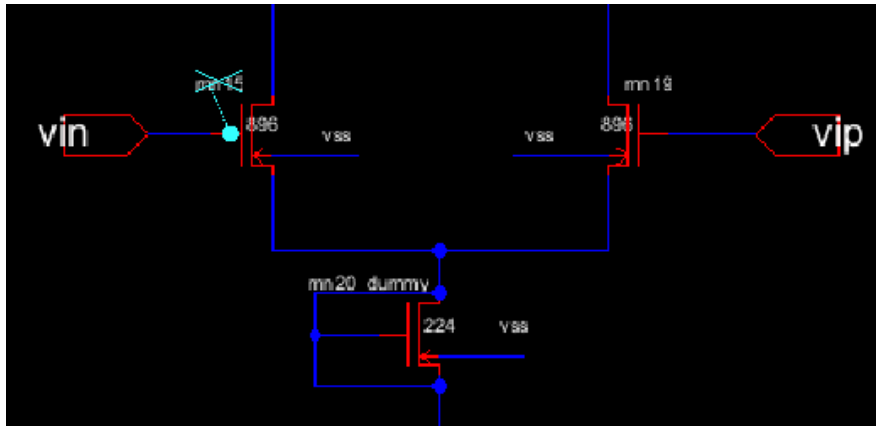
Floorplan

THIS TYPE OF PLACEMENT APPLIES IN (**mn19,mn15,mn20_dum**)

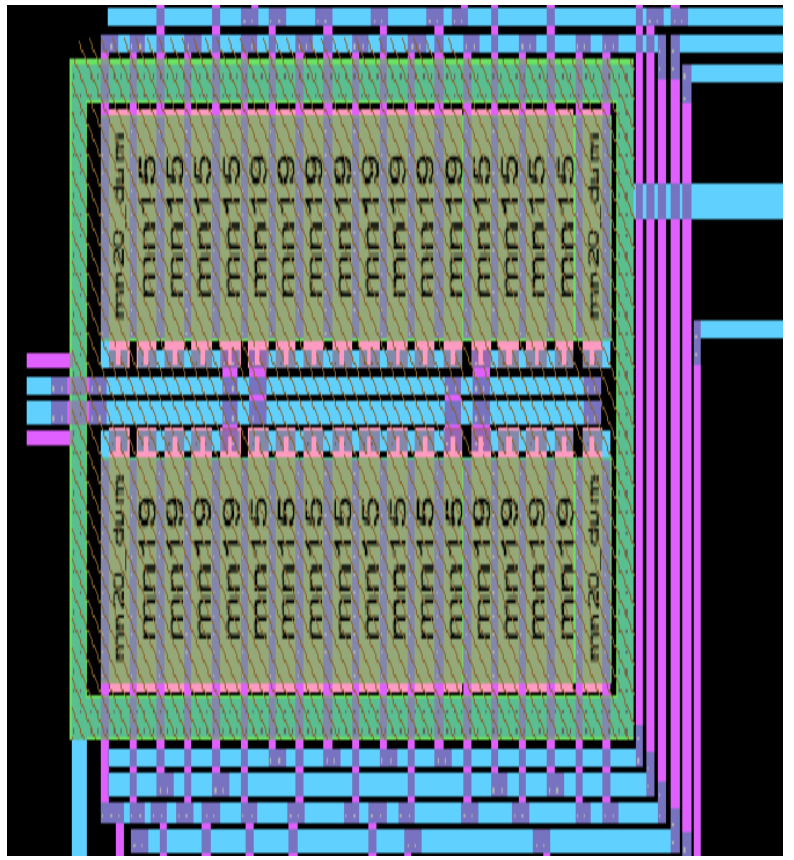
How I Layout my Differential Pairs : ROUTING

Matching Guidelines:

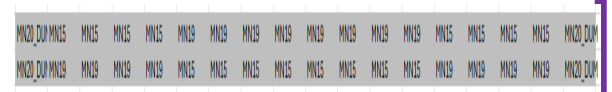
Match the length of wires
Consider shielding input signals
Match the parasitics, both resistance and capacitance
Keep aggressors away from the differential pair



Schematic View



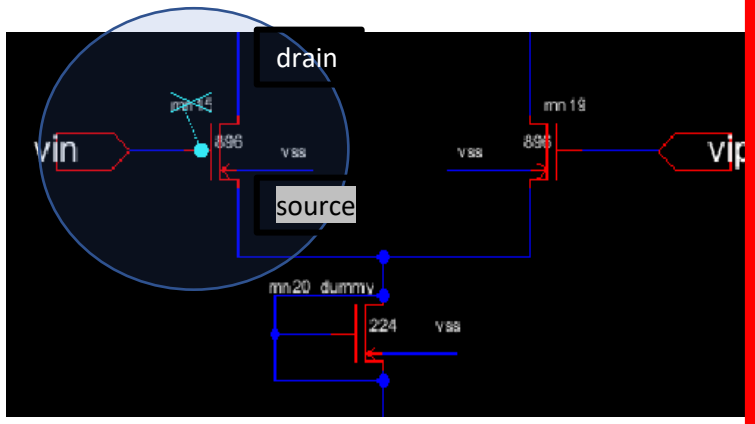
Layout View



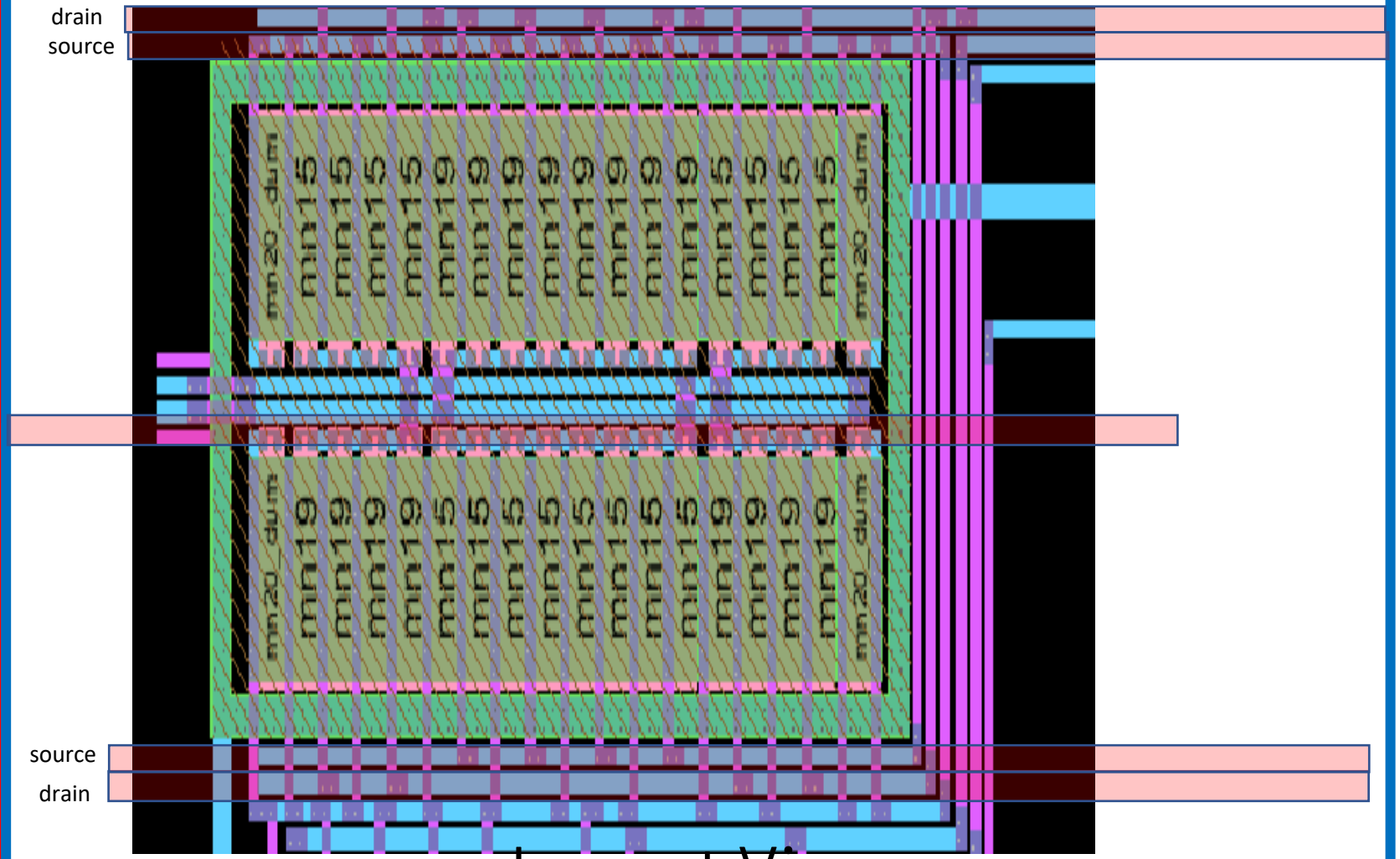
Floorplan

THIS TYPE OF ROUTING APPLIES IN (**mn19,mn15,mn20_dum**)

How I Layout my Differential Pairs : ROUTING



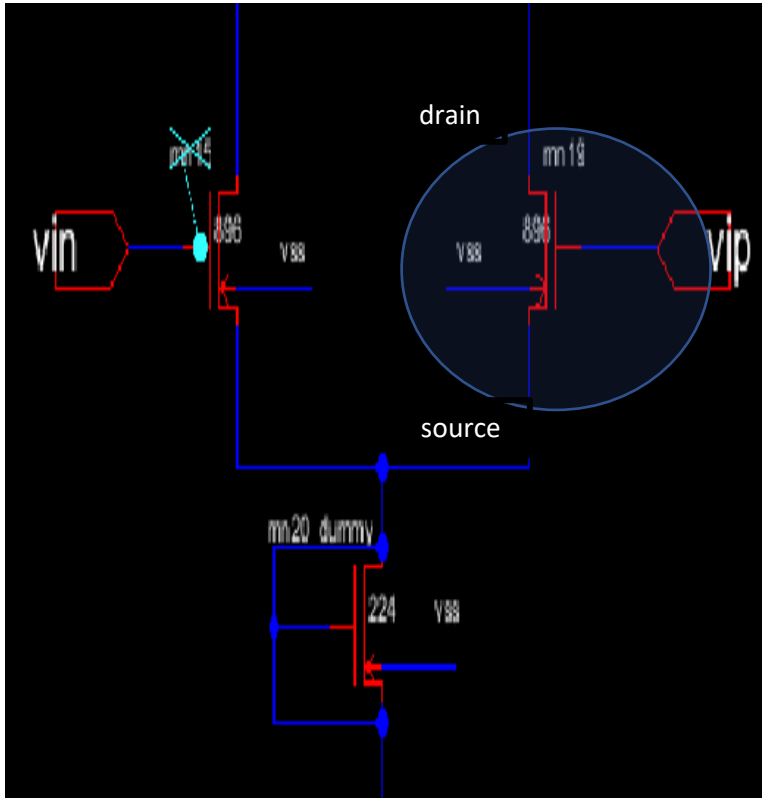
Schematic View



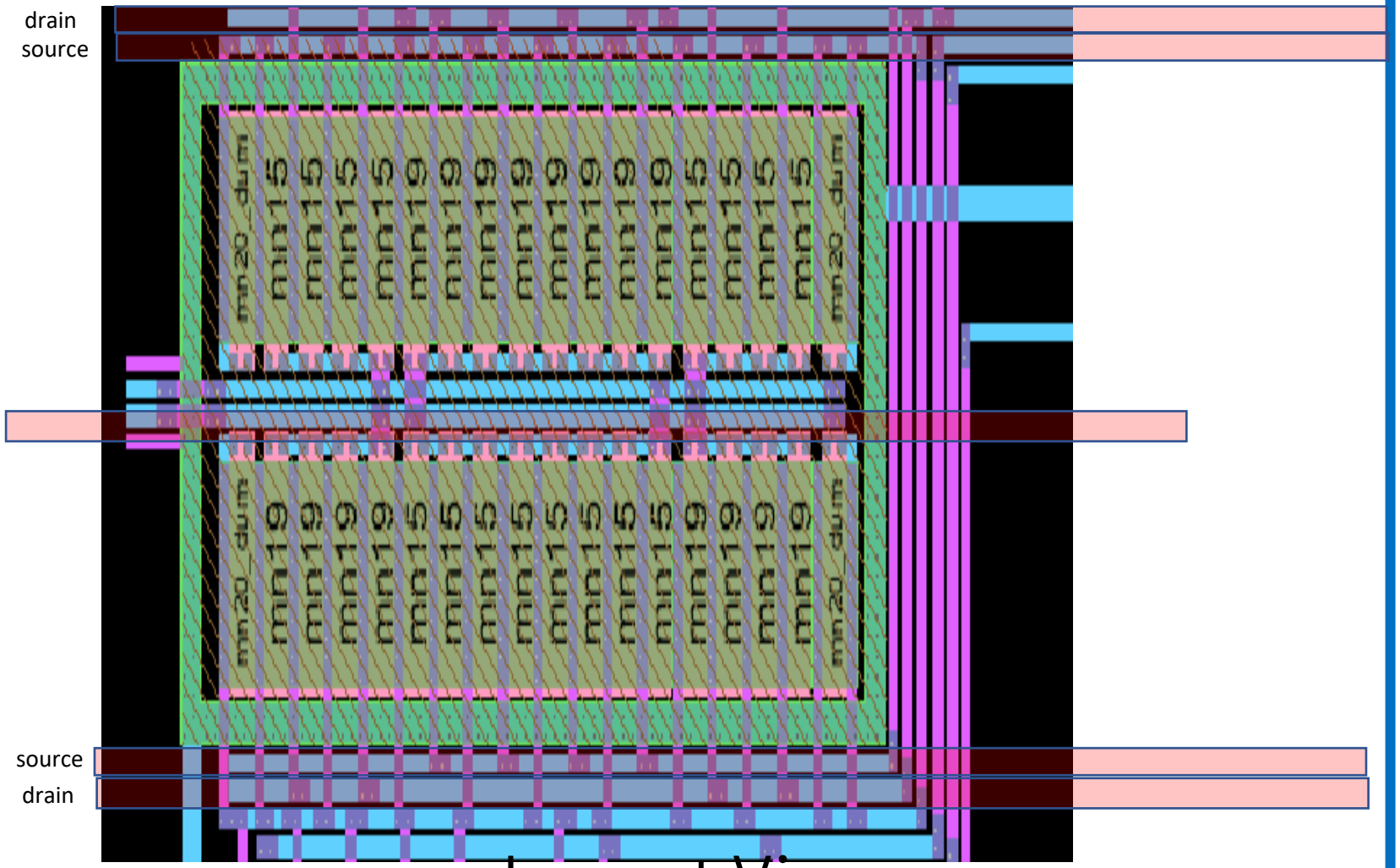
Layout View

THIS TYPE OF ROUTING APPLIES IN (**mn19,mn15,mn20_dum**)

How I Layout my Differential Pairs : ROUTING



Schematic View



Layout View

THIS TYPE OF ROUTING APPLIES IN (**mn19,mn15,mn20_dum**)

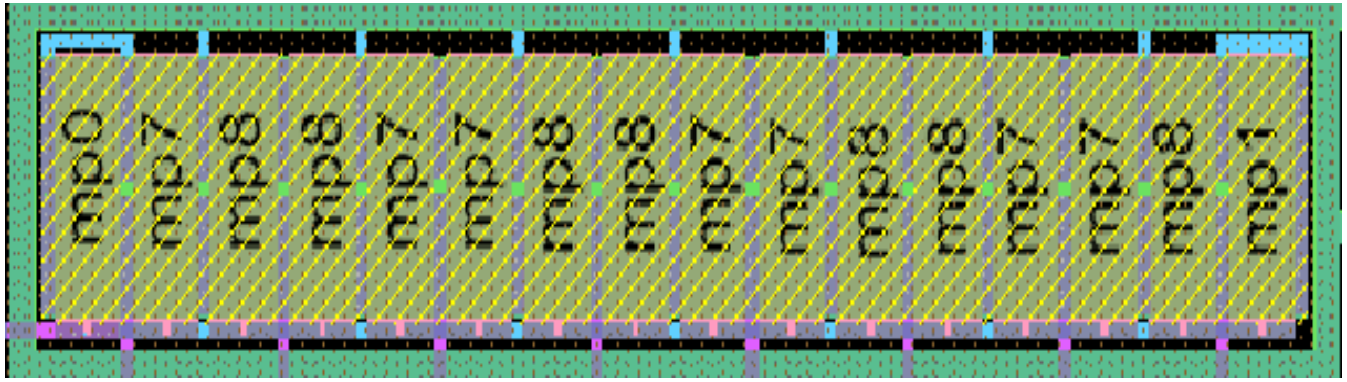
How I Layout my Current Mirrors : PLACEMENT

Matching Guidelines:

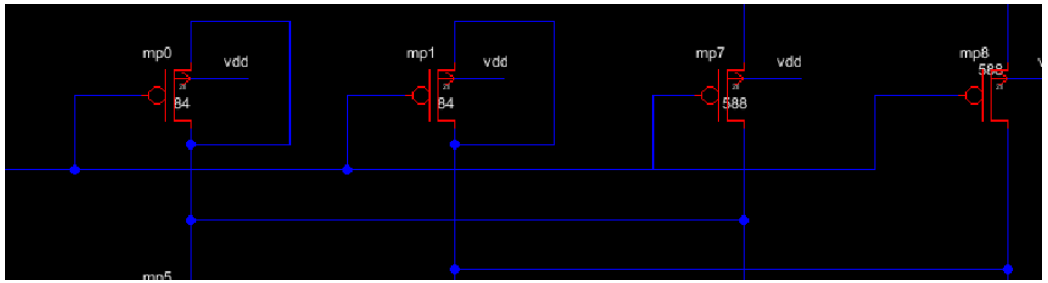
Place the current mirrors around the current reference

Surround dummies

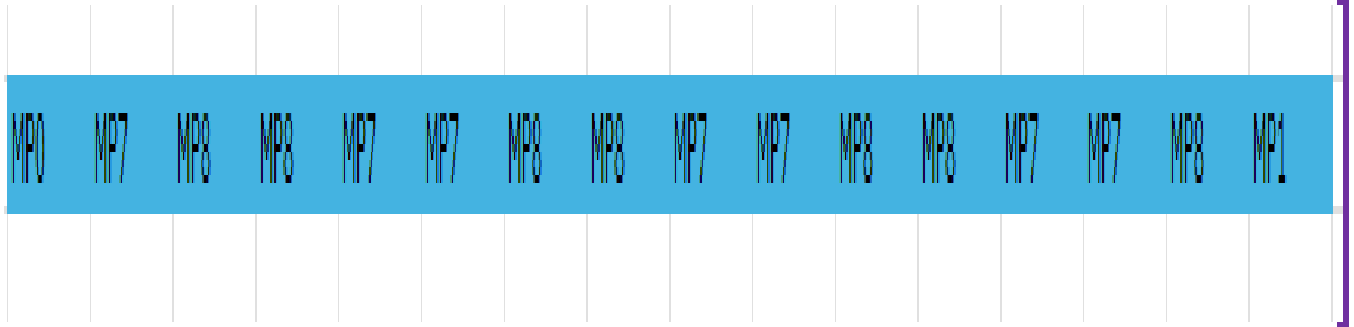
Enclose with guardring



Layout View



Schematic View



Floorplan

THIS TYPE OF PLACEMENT APPLIES IN (**mp0,mp1,mp7,mp8**)

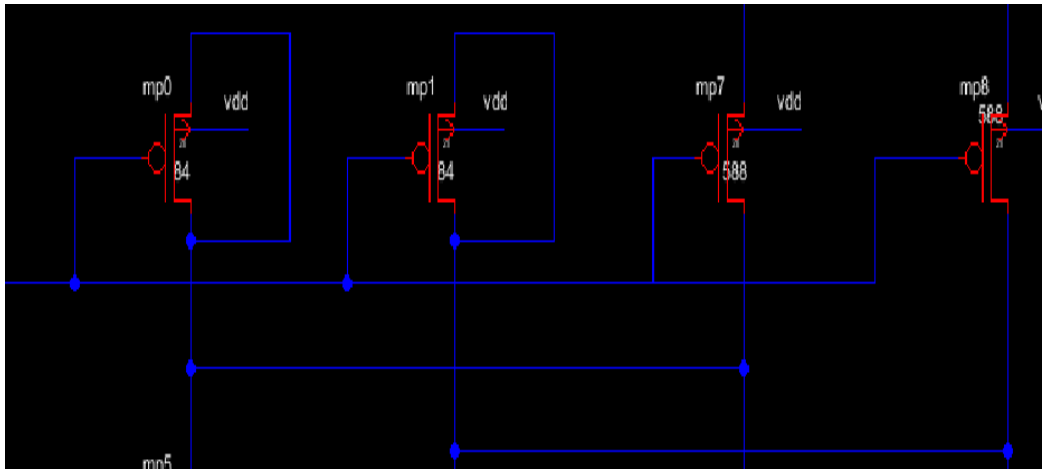
How I Layout my Current Mirrors : ROUTING

Matching Guidelines:

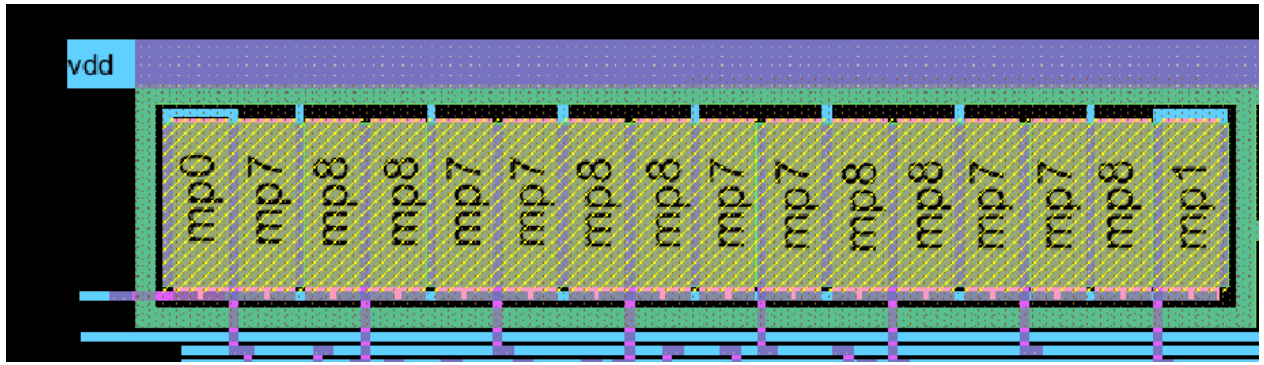
Connect all gate terminals

Connect the source terminals to BG

Connect the drain of each segment



Schematic View



Layout View

Floorplan

THIS TYPE OF ROUTING APPLIES IN (**mp0,mp1,mp7,mp8**)

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Layout Takeaways

ANALOG IC DESIGN IMPLEMENTATION – LAYOUT REVIEW

LAYOUT TAKEAWAYS

- Proper Layout Structure
- Correct sizing of metals and Transistors
- General Layout Rules
- Proper implementation of Layout design

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Question and Answer

ANALOG IC DESIGN IMPLEMENTATION – LAYOUT REVIEW

END OF PRESENTATION

THANK YOU

Elective 3 Block Layout Review

Analog IC Design Implementation