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ELECTIVE 3 BLOCK LAYOUT REVIEW

ANALOG IC DESIGN IMPLEMENTATION

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BSCPE4A

OUTLINE

- General Block Layout Guidelines
- Block Details
- General Layout Implementation
- Layout Takeaways
- Question and Answers



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General Block Layout Guidelines

ANALOG IC DESIGN IMPLEMENTATION - LAYOUT REVIEW

GENERAL BLOCK LAYOUT GUIDELINES

- Allotted Area: $X = 750\lambda$ (Maximum) , $Y = \text{variable}$
- Use 24λ for main power and Ground line widths.
- Match devices properly.
- Avoid routing on active devices.
- Do not use poly when routing.
- Place pins at block edges.
- Keep the layout compact and the shape as regular as possible.
- Implement double via when routing.
- Implement double contact rows for Back gate.
- Use side shield.
- Create Dummies if applicable.
- Layout should be verified. (DRC and LVS).

OTHER LAYOUT CONSIDERATIONS

- Uniform Metal Orientation
- Avoid intersecting input and output lines
- Instances Label
- Same Size, Shape, Structure, Temperature, Orientation and Surroundings
- Close to minimum distances/Abutment
- Common Centroid Geometry: Cross-Quad/Interdigitation
- Non-Minimum Size Device



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Block Details

ANALOG IC DESIGN IMPLEMENTATION - LAYOUT REVIEW

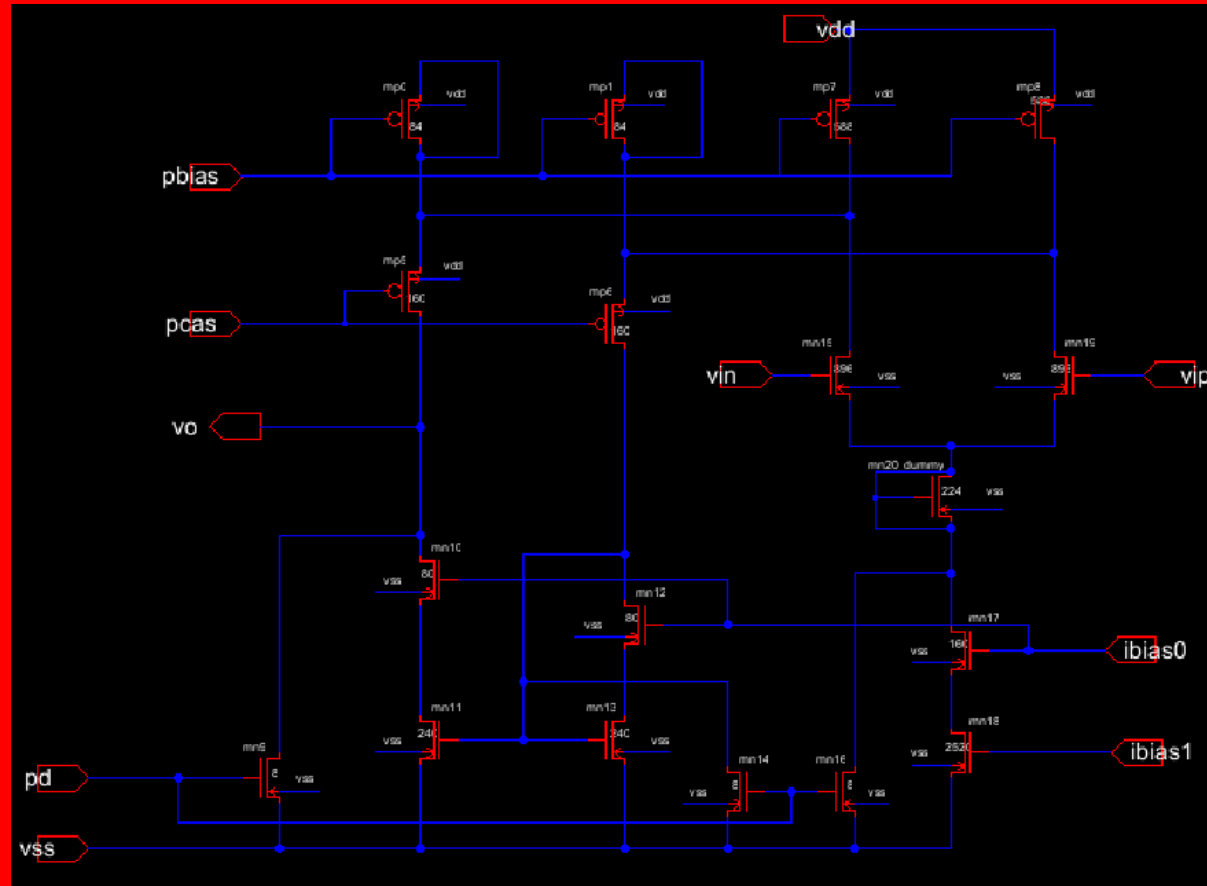
BLOCK DETAILS

Block Name	hfrcosc_comp_folded_Puso
Circuit Name	<i>Comparator using Folded Cascode Amplifier</i>
Actual Area	$X = 880\lambda$, $Y = 1080.5\lambda$
Verifications	<i>DRC, NCC, ERC(ANTENNA, WELLS)</i>

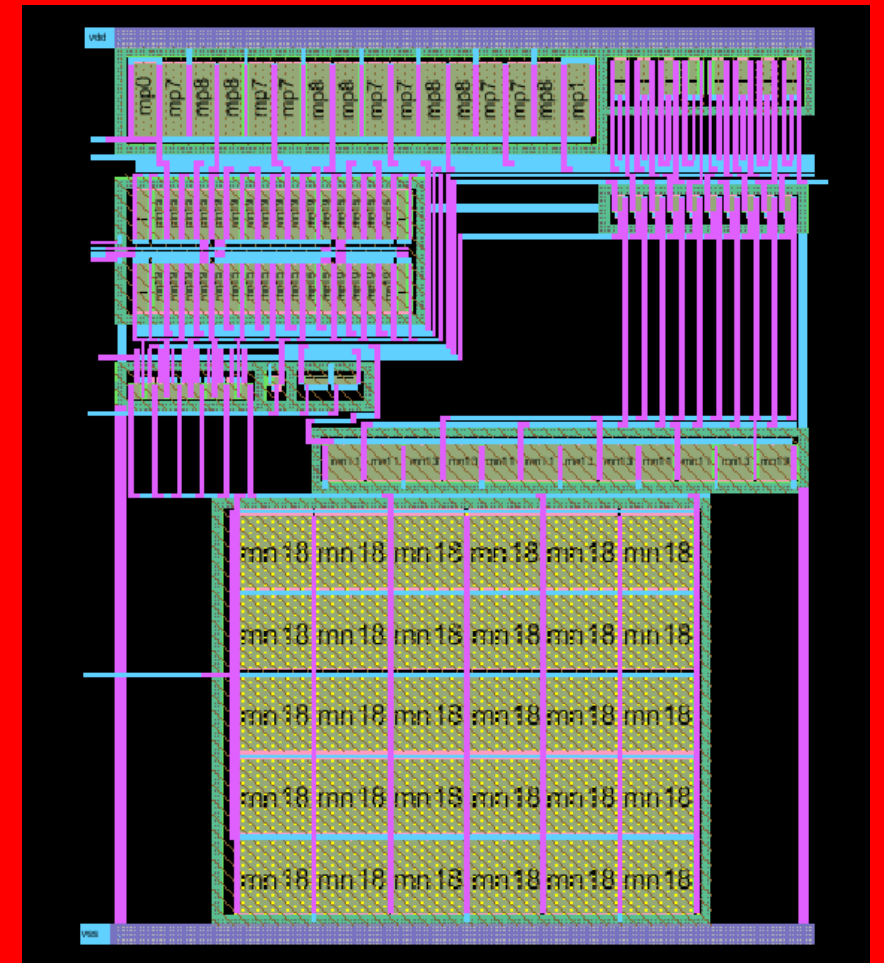
Schedule (3 hrs per ECEMIC3 Schedule)

10 Nov 2023	17 Nov 2023	24 Nov 2023	28 Nov 2023	1 Dec 2023	5 Dec 2023	12 Dec 2023
Placement	Placement	Placement	Placement	Placement	Placement/Routing	PPT

BLOCK DETAILS



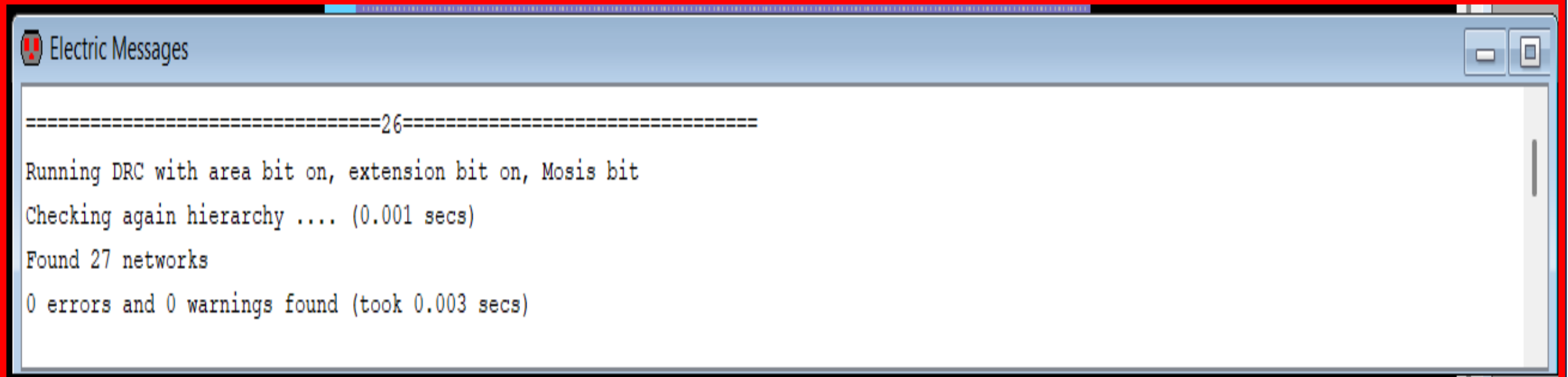
Schematic View



Layout View

BLOCK DETAILS

Verification Job : DRC

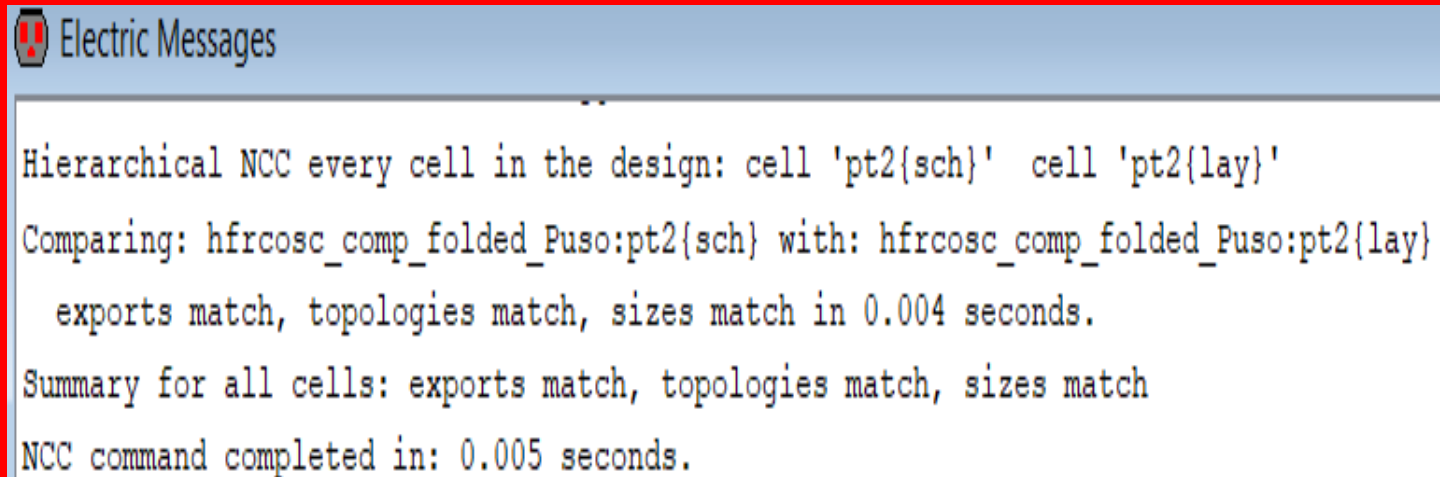
A screenshot of a software window titled 'Electric Messages'. The window has a light blue header bar with the title and standard window controls (minimize, maximize, close). The main area is white and contains text in a monospaced font. The text is as follows:

```
=====26=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 27 networks
0 errors and 0 warnings found (took 0.003 secs)
```

DRC RESULTS

BLOCK DETAILS

Verification Job : NCC(LVS)

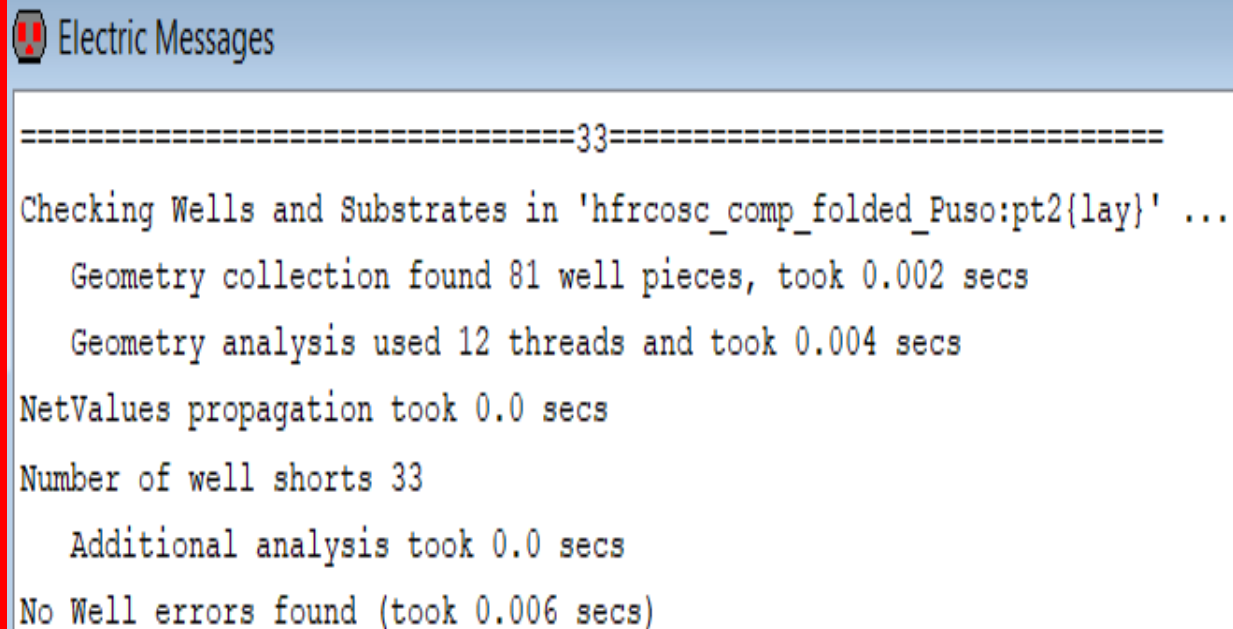


The screenshot shows a window titled "Electric Messages" with a standard Windows-style title bar (minimize, maximize, close buttons). The window contains a text area with the following content:

```
Hierarchical NCC every cell in the design: cell 'pt2{sch}'  cell 'pt2{lay}'  
Comparing: hfrcosc_comp_folded_Puso:pt2{sch} with: hfrcosc_comp_folded_Puso:pt2{lay}  
  exports match, topologies match, sizes match in 0.004 seconds.  
Summary for all cells: exports match, topologies match, sizes match  
NCC command completed in: 0.005 seconds.
```

NCC RESULTS

Verification Job : ERC

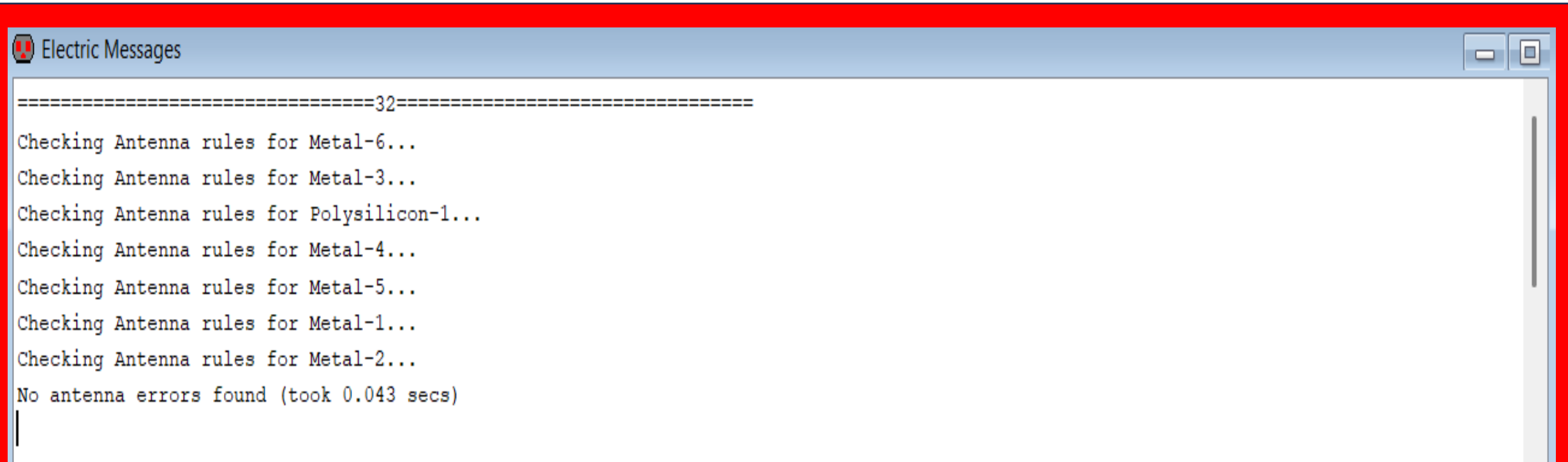


The screenshot shows a window titled 'Electric Messages' with a standard Windows-style title bar. The window contains a text area with the following content:

```
=====33=====
Checking Wells and Substrates in 'hfrcosc_comp_folded_Puso:pt2{lay}' ...
  Geometry collection found 81 well pieces, took 0.002 secs
  Geometry analysis used 12 threads and took 0.004 secs
NetValues propagation took 0.0 secs
Number of well shorts 33
  Additional analysis took 0.0 secs
No Well errors found (took 0.006 secs)
```

ERC RESULTS

Verification Job : ANTENNA CHECK

A screenshot of a software window titled "Electric Messages". The window has a light blue title bar with standard minimize, maximize, and close buttons. The main content area is white and displays a series of text messages in a monospaced font. The messages are: "=====-32====", "Checking Antenna rules for Metal-6...", "Checking Antenna rules for Metal-3...", "Checking Antenna rules for Polysilicon-1...", "Checking Antenna rules for Metal-4...", "Checking Antenna rules for Metal-5...", "Checking Antenna rules for Metal-1...", "Checking Antenna rules for Metal-2...", and "No antenna errors found (took 0.043 secs)". A vertical scrollbar is visible on the right side of the message area.

```
=====-32====  
Checking Antenna rules for Metal-6...  
Checking Antenna rules for Metal-3...  
Checking Antenna rules for Polysilicon-1...  
Checking Antenna rules for Metal-4...  
Checking Antenna rules for Metal-5...  
Checking Antenna rules for Metal-1...  
Checking Antenna rules for Metal-2...  
No antenna errors found (took 0.043 secs)
```

ANTENNA CHECK RESULTS



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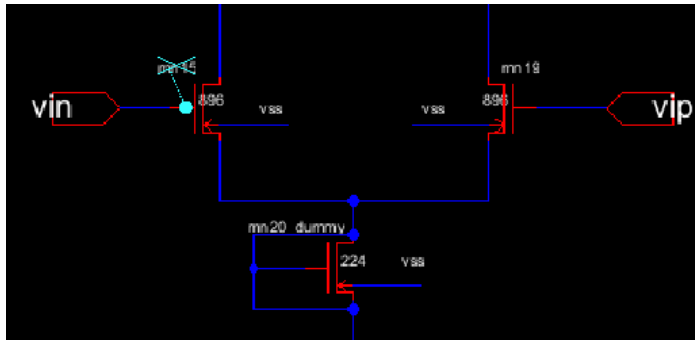
General Layout Implementation

ANALOG IC DESIGN IMPLEMENTATION - LAYOUT REVIEW

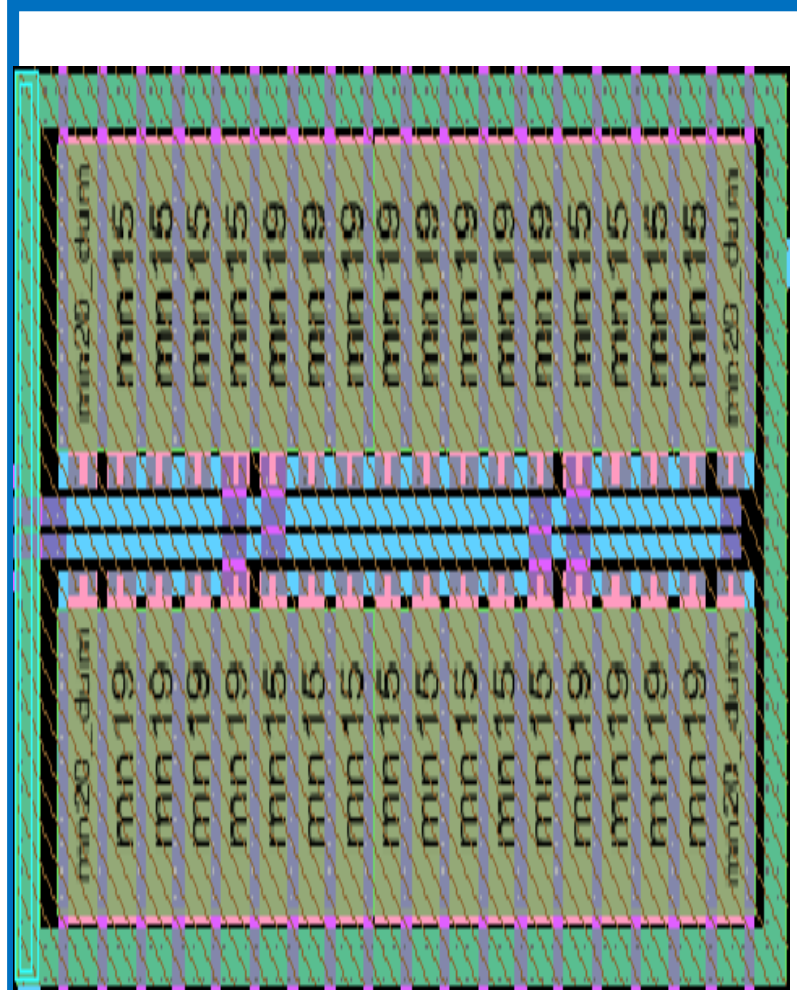
How I Layout my Differential Pairs : PLACEMENT

Matching Guidelines:

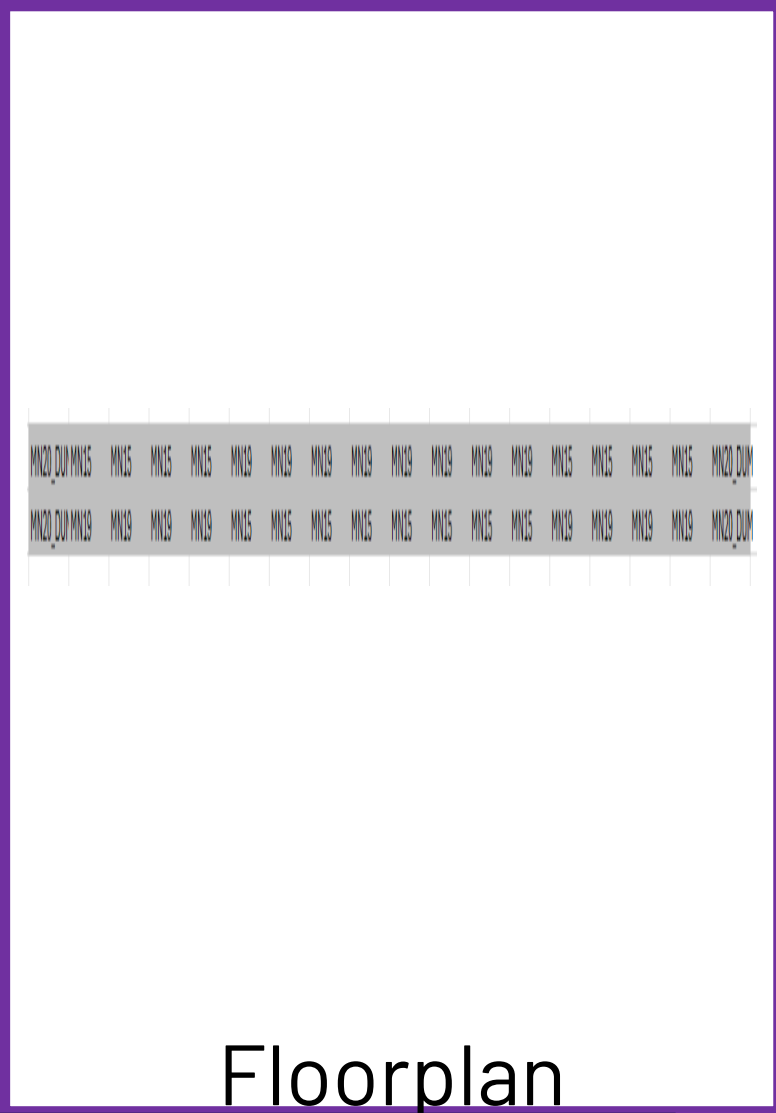
- Cross Quad
- Shared Diffusion
- Surround Dummies
- Enclosed Guardring



Schematic View



Layout View



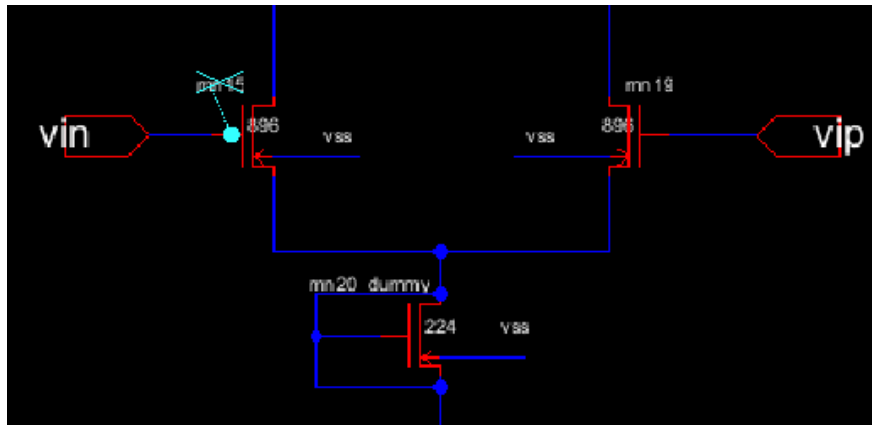
Floorplan

THIS TYPE OF PLACEMENT APPLIES IN (mn19,mn15,mn20_dum)

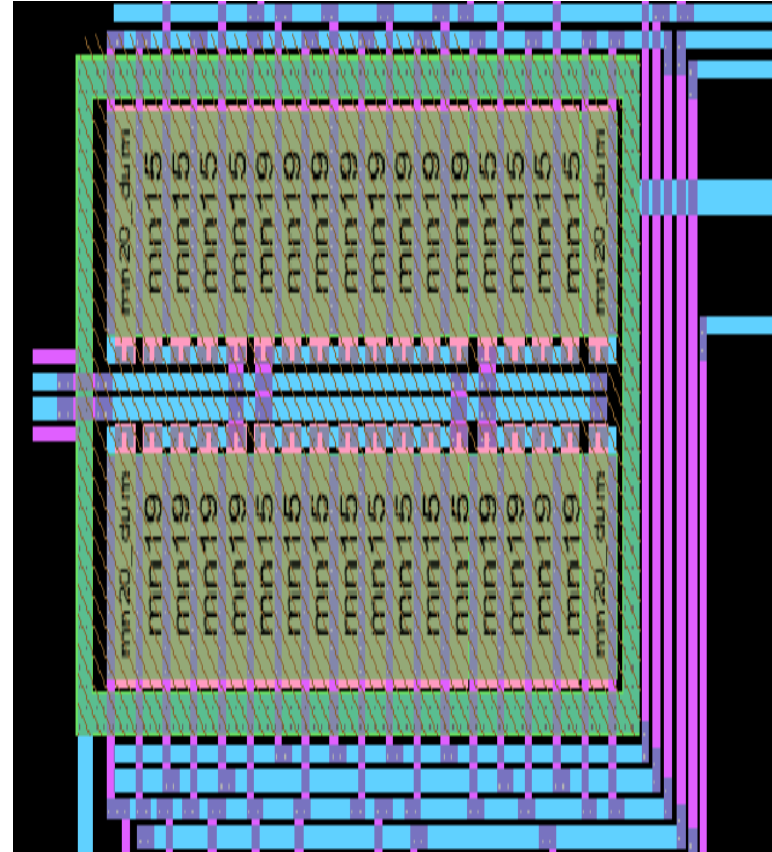
How I Layout my Differential Pairs : ROUTING

Matching Guidelines:

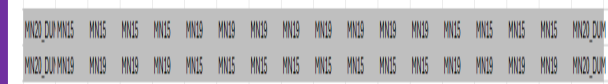
- Match the length of wires
- Consider shielding input signals
- Match the parasitics, both resistance and capacitance
- Keep aggressors away from the differential pair



Schematic View



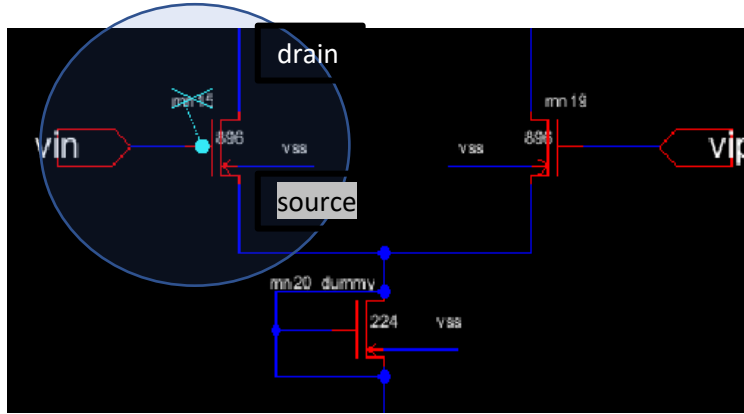
Layout View



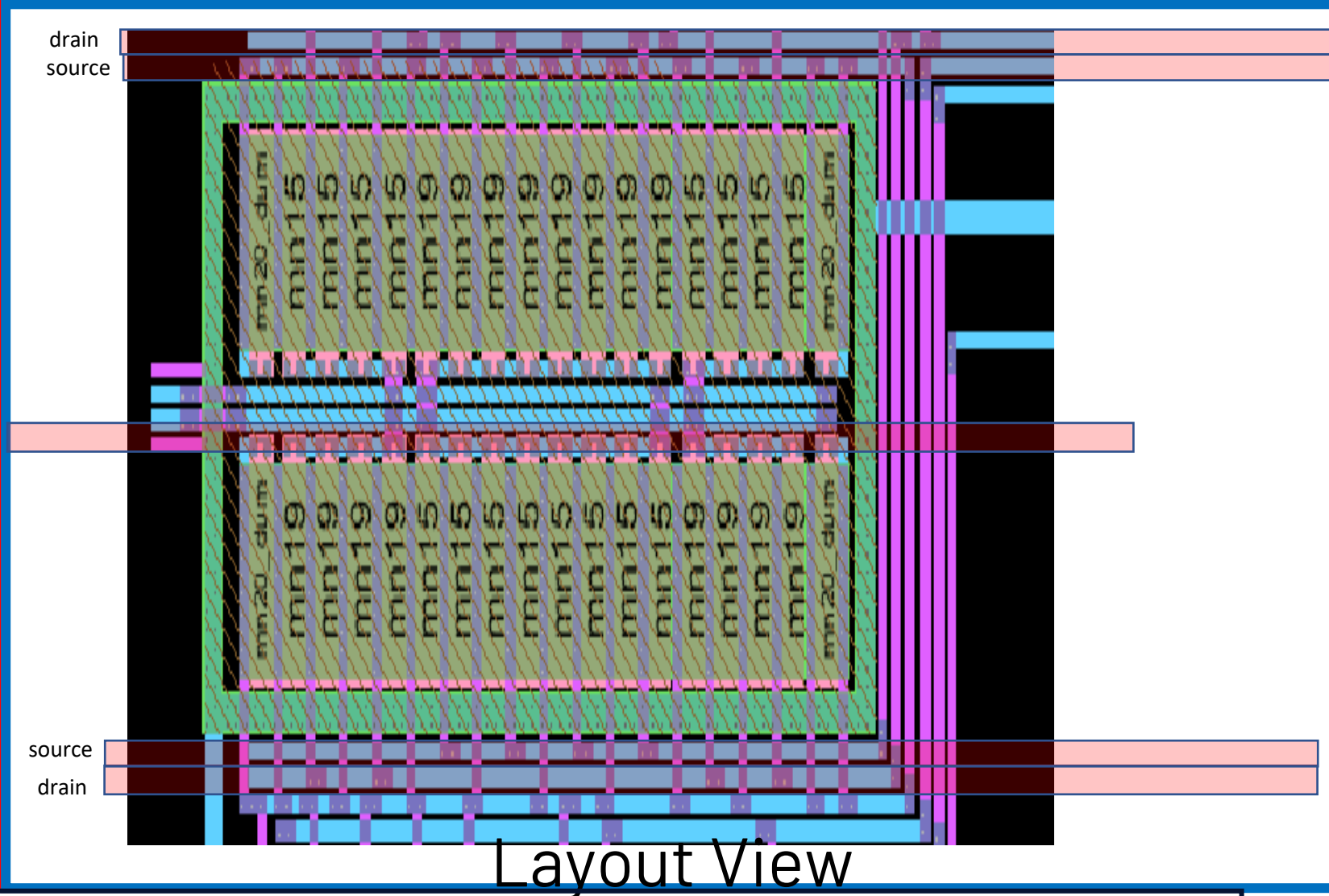
Floorplan

THIS TYPE OF ROUTING APPLIES IN (**mn19,mn15,mn20_dum**)

How I Layout my Differential Pairs : ROUTING



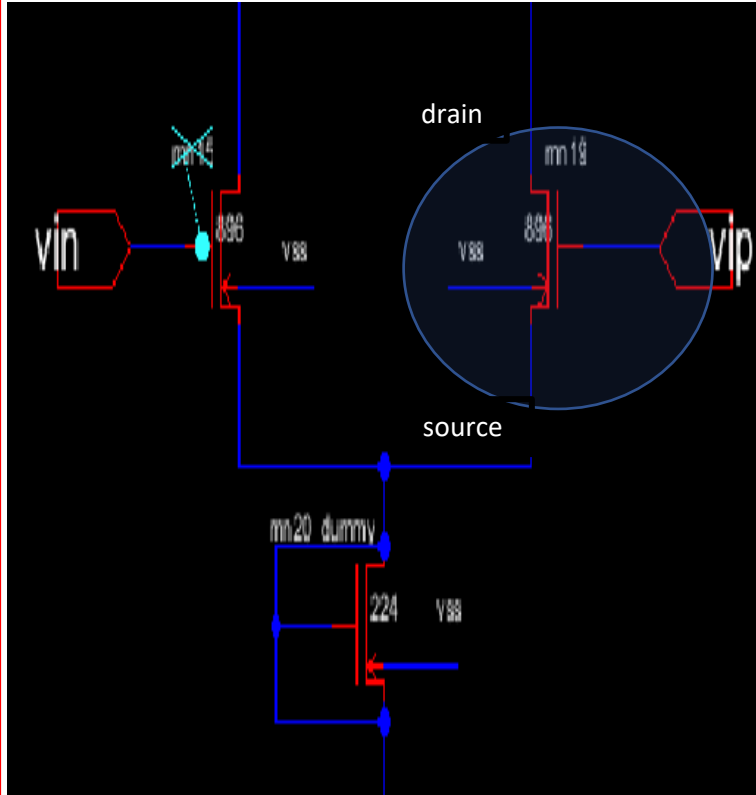
Schematic View



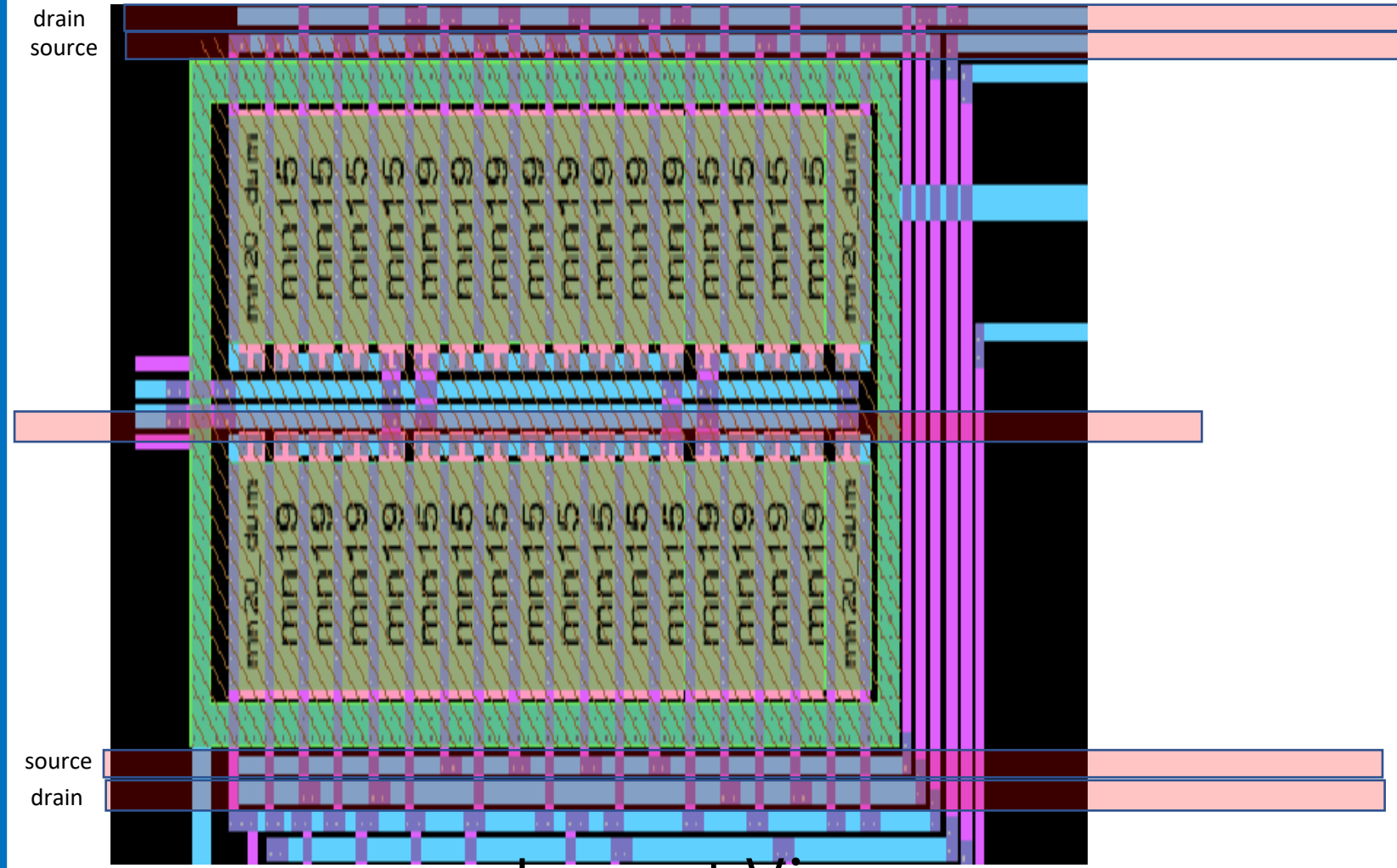
Layout View

THIS TYPE OF ROUTING APPLIES IN (mn19,mn15,mn20_dum)

How I Layout my Differential Pairs : ROUTING



Schematic View



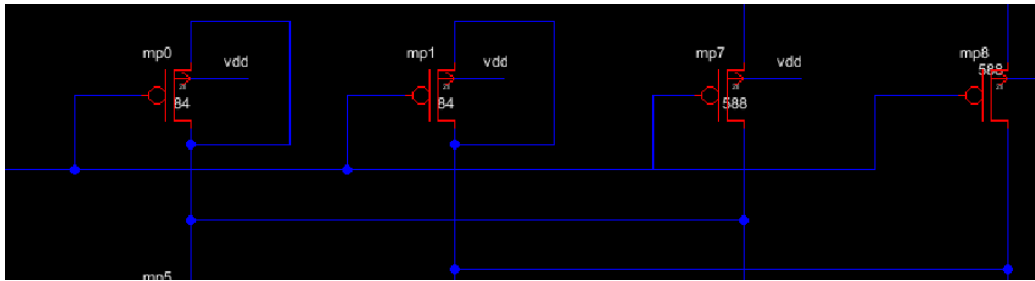
Layout View

THIS TYPE OF ROUTING APPLIES IN (**mn19,mn15,mn20_dum**)

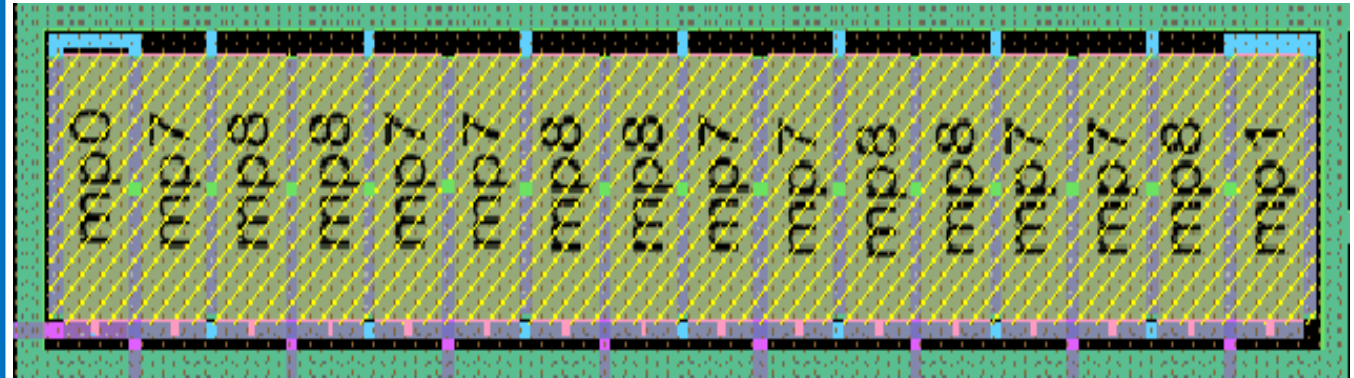
How I Layout my Current Mirrors : PLACEMENT

Matching Guidelines:

Place the current mirrors around the
current reference
Surround dummies
Enclose with guardring



Schematic View



Layout View



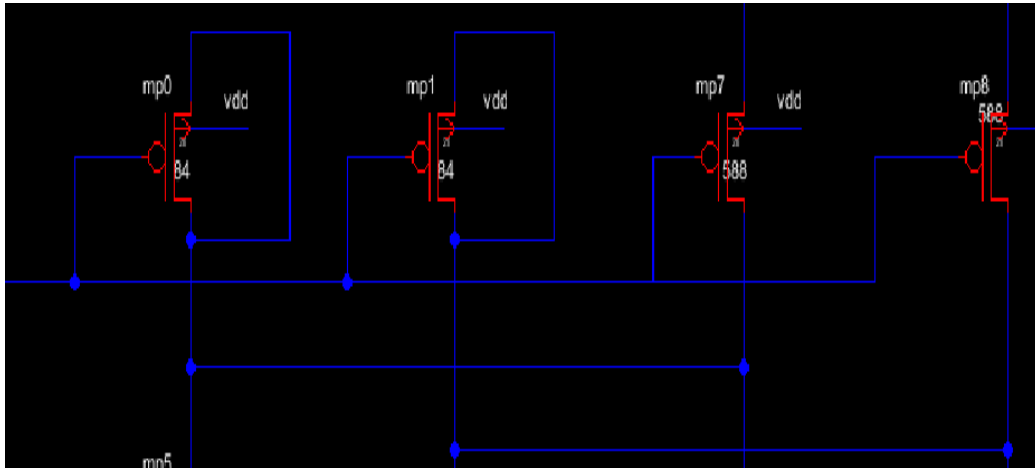
Floorplan

THIS TYPE OF PLACEMENT APPLIES IN (mp0,mp1,mp7,mp8)

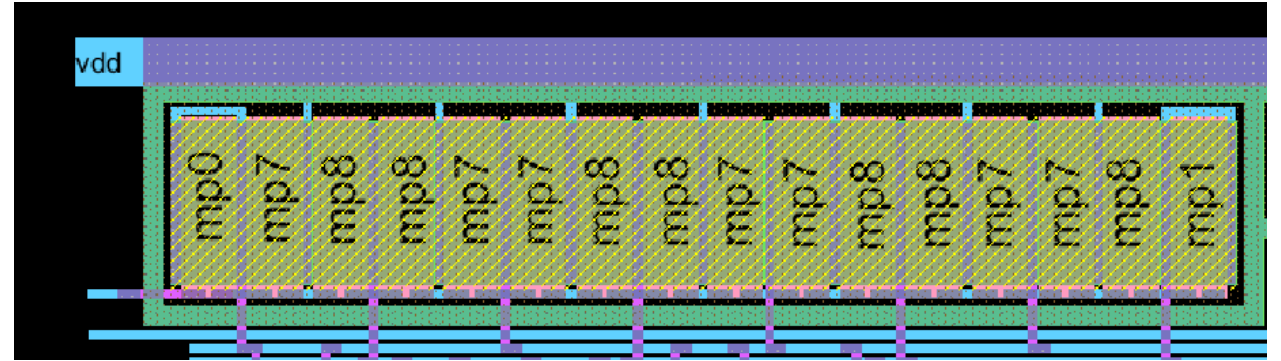
How I Layout my Current Mirrors : ROUTING

Matching Guidelines:

- Connect all gate terminals
- Connect the source terminals to BG
- Connect the drain of each segment



Schematic View



Layout View



Floorplan

THIS TYPE OF ROUTING APPLIES IN (mp0,mp1,mp7,mp8)



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Layout Takeaways

ANALOG IC DESIGN IMPLEMENTATION - LAYOUT REVIEW

LAYOUT TAKEAWAYS

- Proper Layout Structure
- Correct sizing of metals and Transistors
- General Layout Rules
- Proper implementation of Layout design



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Question and Answer

ANALOG IC DESIGN IMPLEMENTATION - LAYOUT REVIEW

THANK YOU

Elective 3 Block Layout Review

Analog IC Design Implementation