

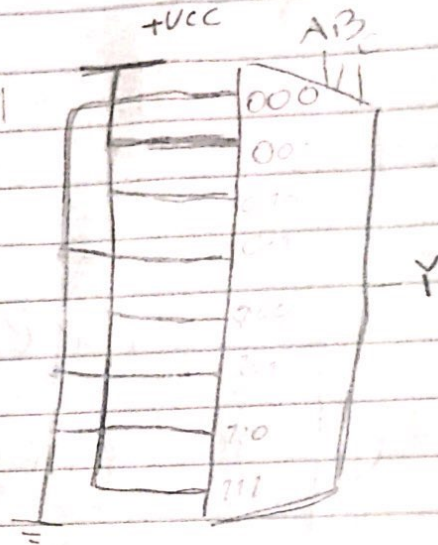
Laboratorio #15

Ejercicio 01

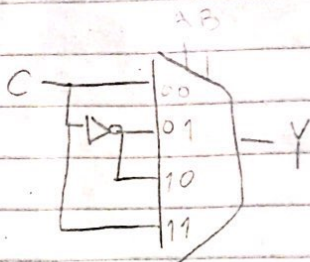
Tabla 01

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

MUX 8:1



MUX 4:1



A  
B  
C

MUX 2:1

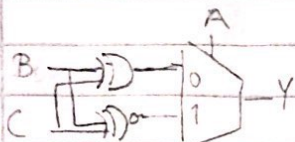
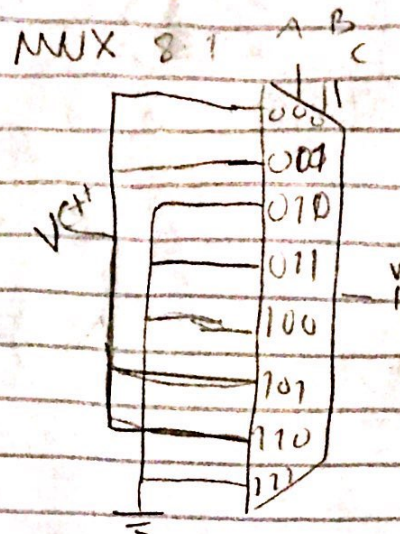


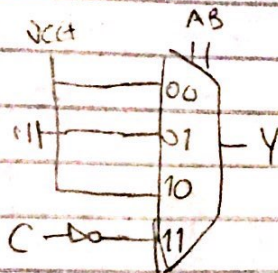


Tabla 02

A	B	C	Y
0	0	0	1
0	0	1	X (+)
0	1	0	0
0	1	1	0
1	0	0	X (-)
1	0	1	1
1	1	0	1
1	1	1	0



MUX 4:1



## Ejercicio 05

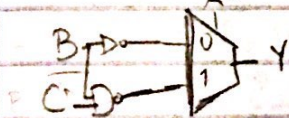
### Propagation Delay

Es el máx delay que ocurre tras un cambio en su entrada

### Contamination Delay

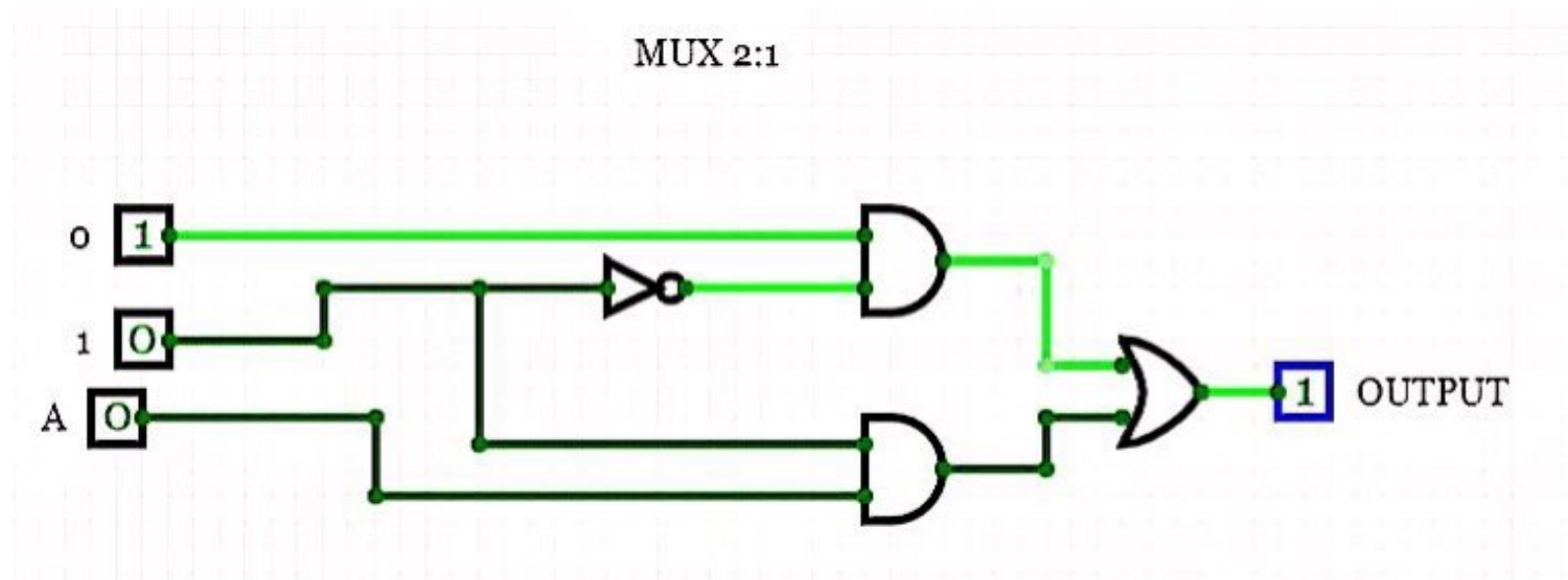
Es el delay min causado por suceso o imperfección en un circuito mostrado en su entrada.

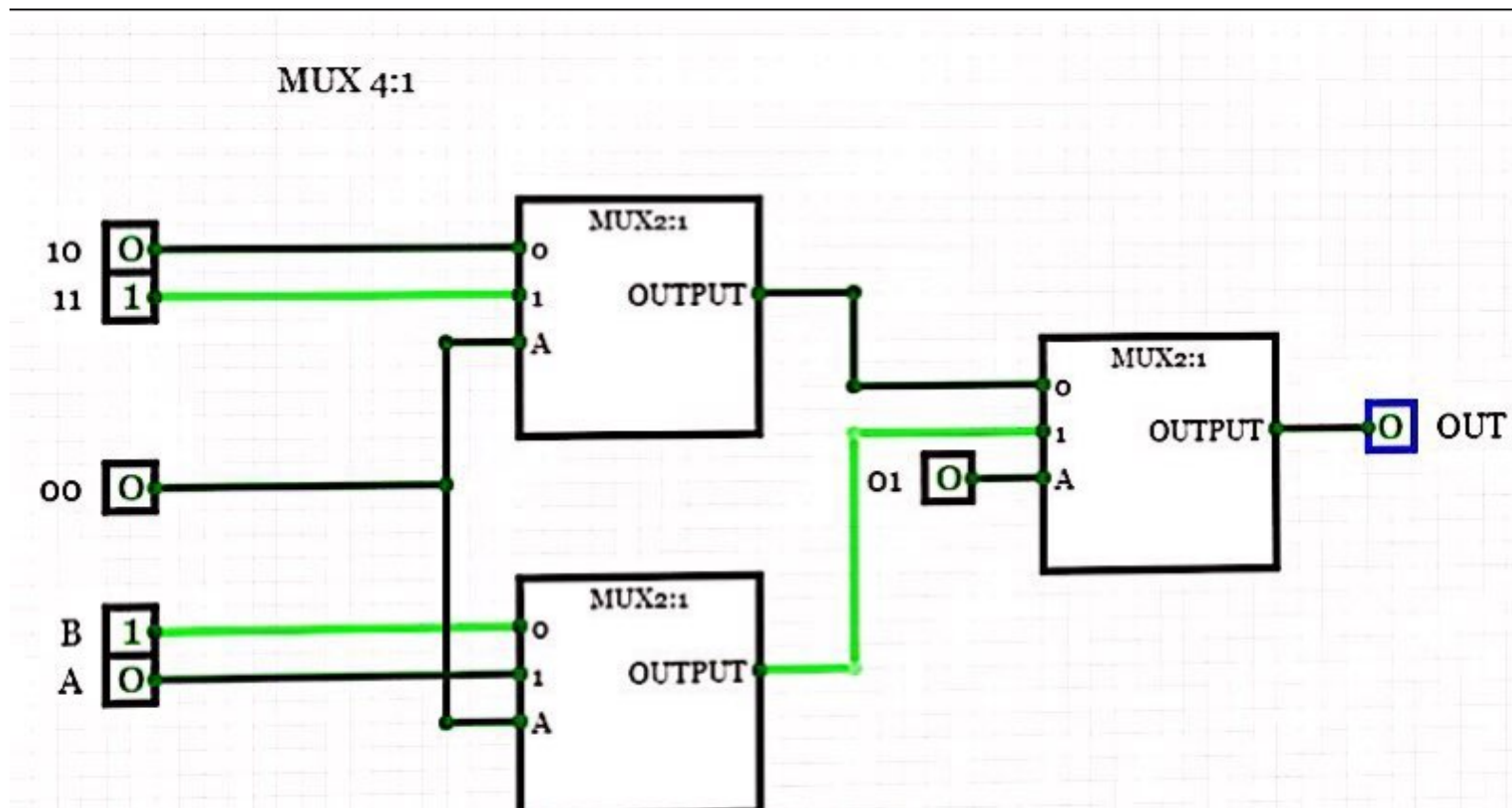
MUX 2:1



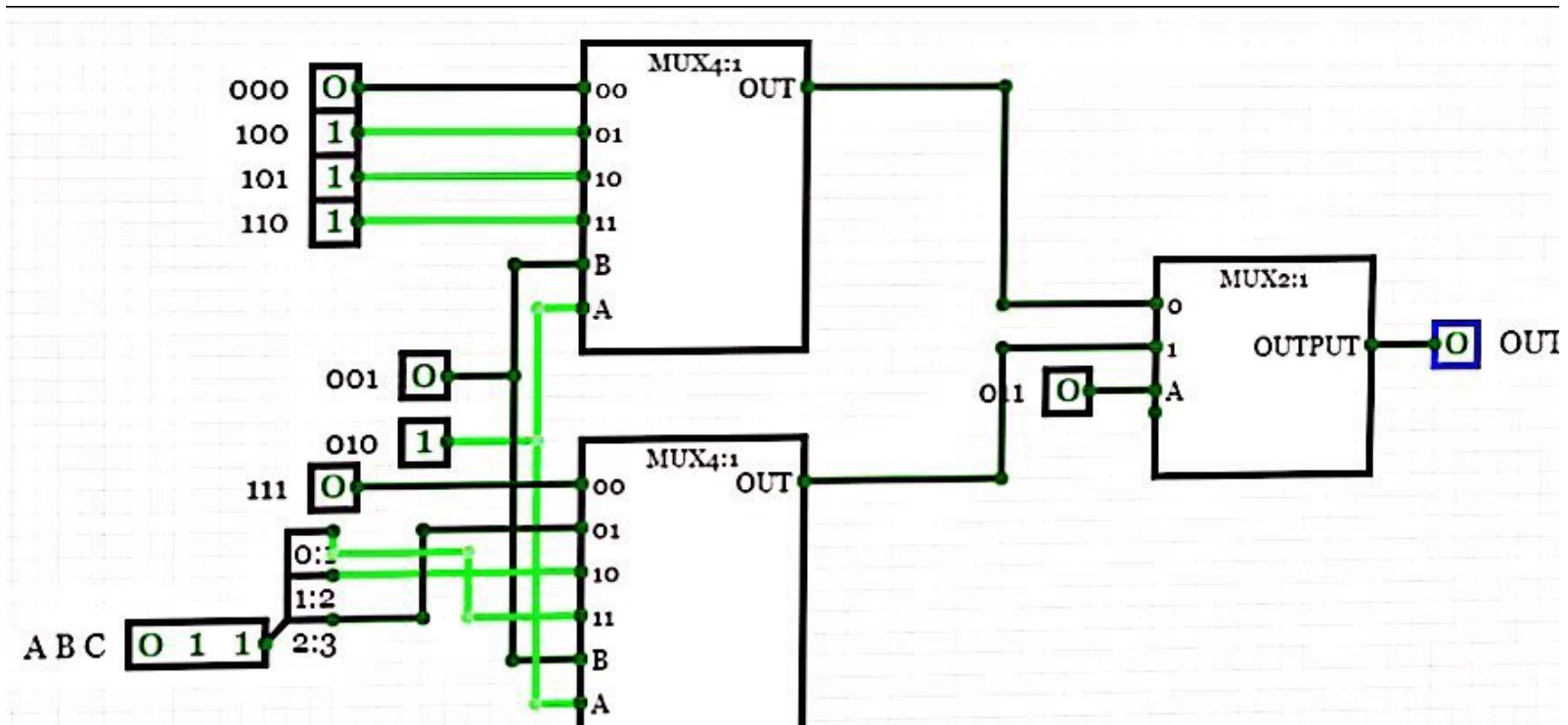
Ruta Crítica La suma tpd de la ruta más alta.

Ruta Corta La suma tcd de la ruta es la más baja.









# Ejercicio 03

TABLA 01

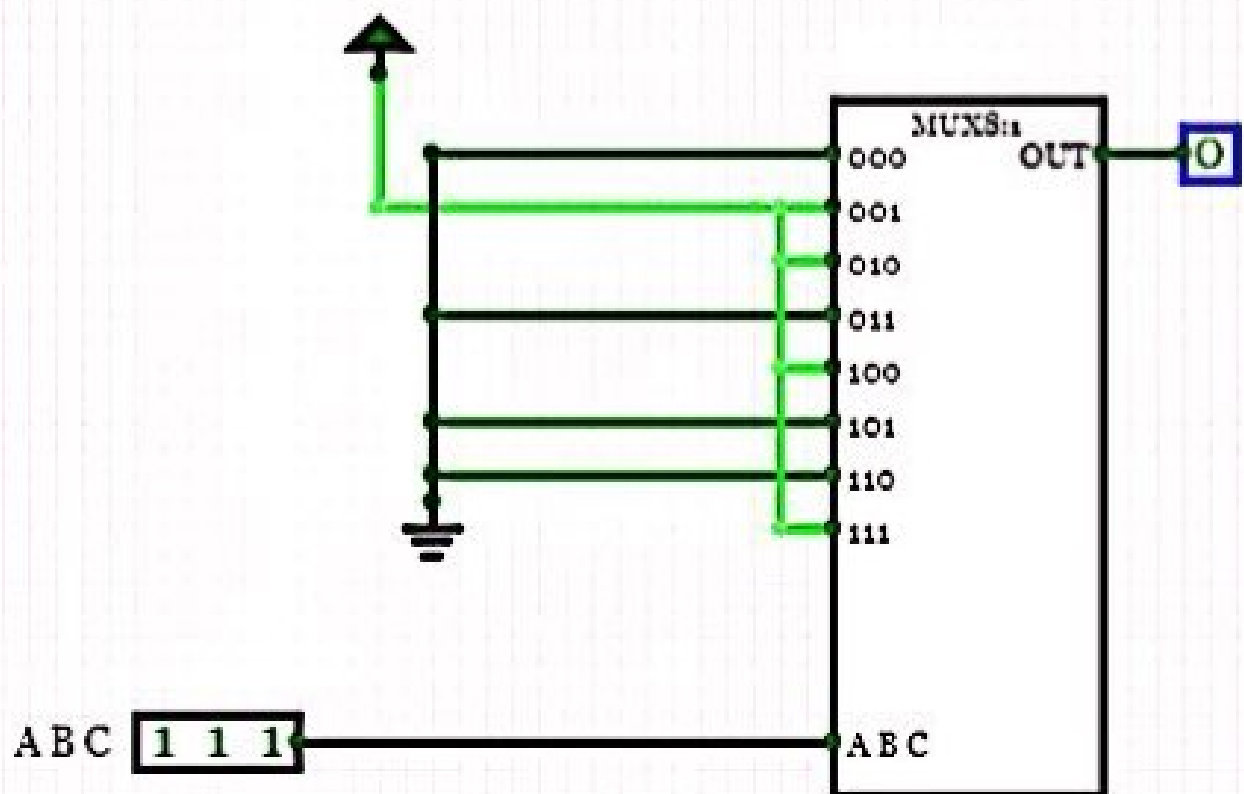
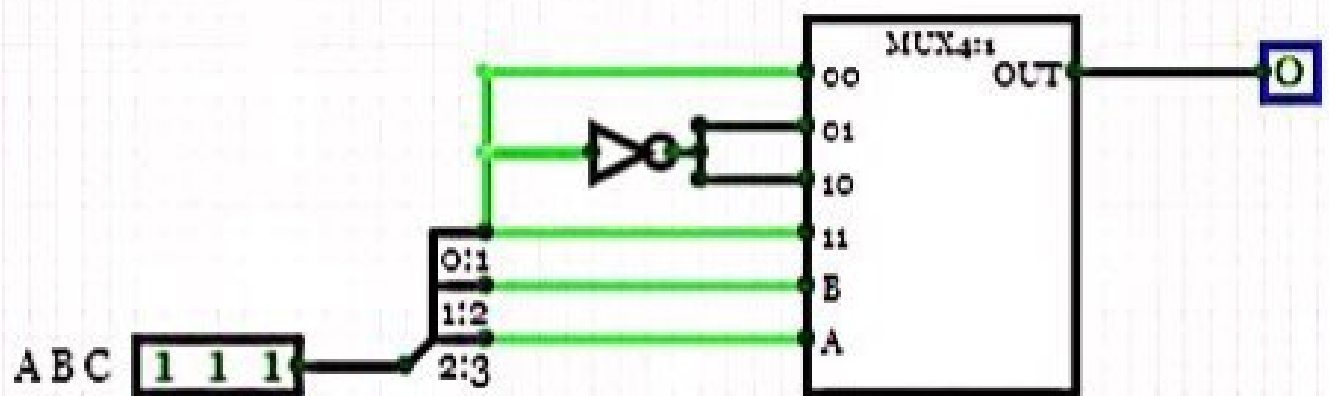
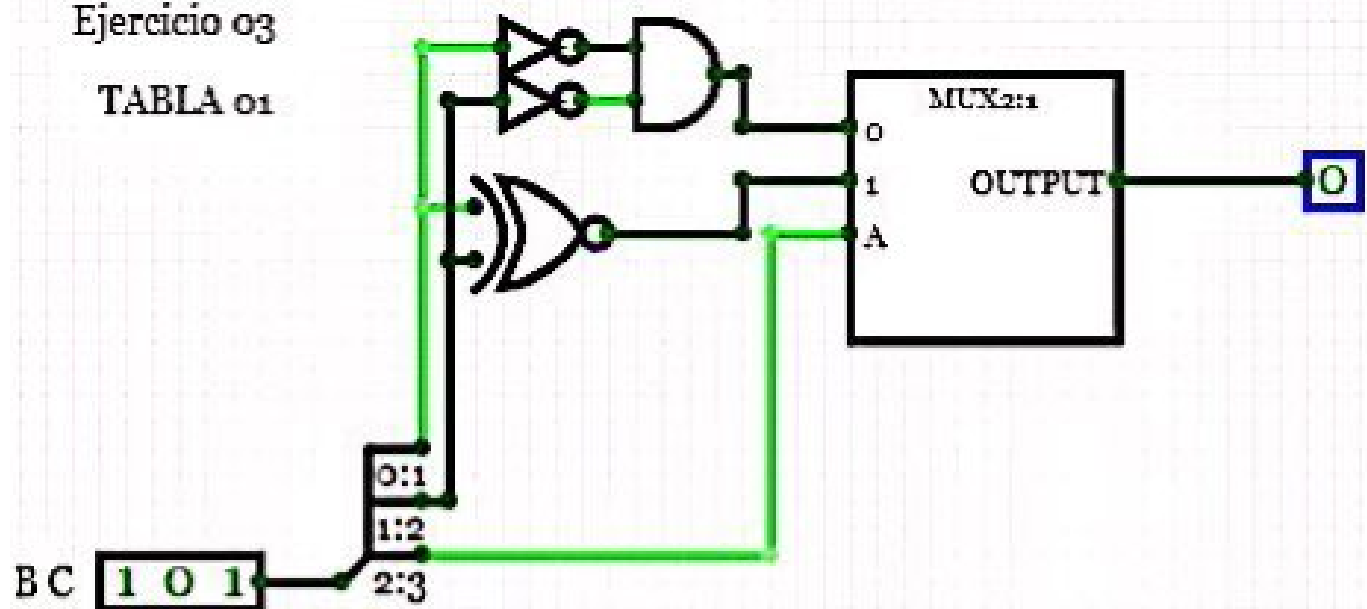
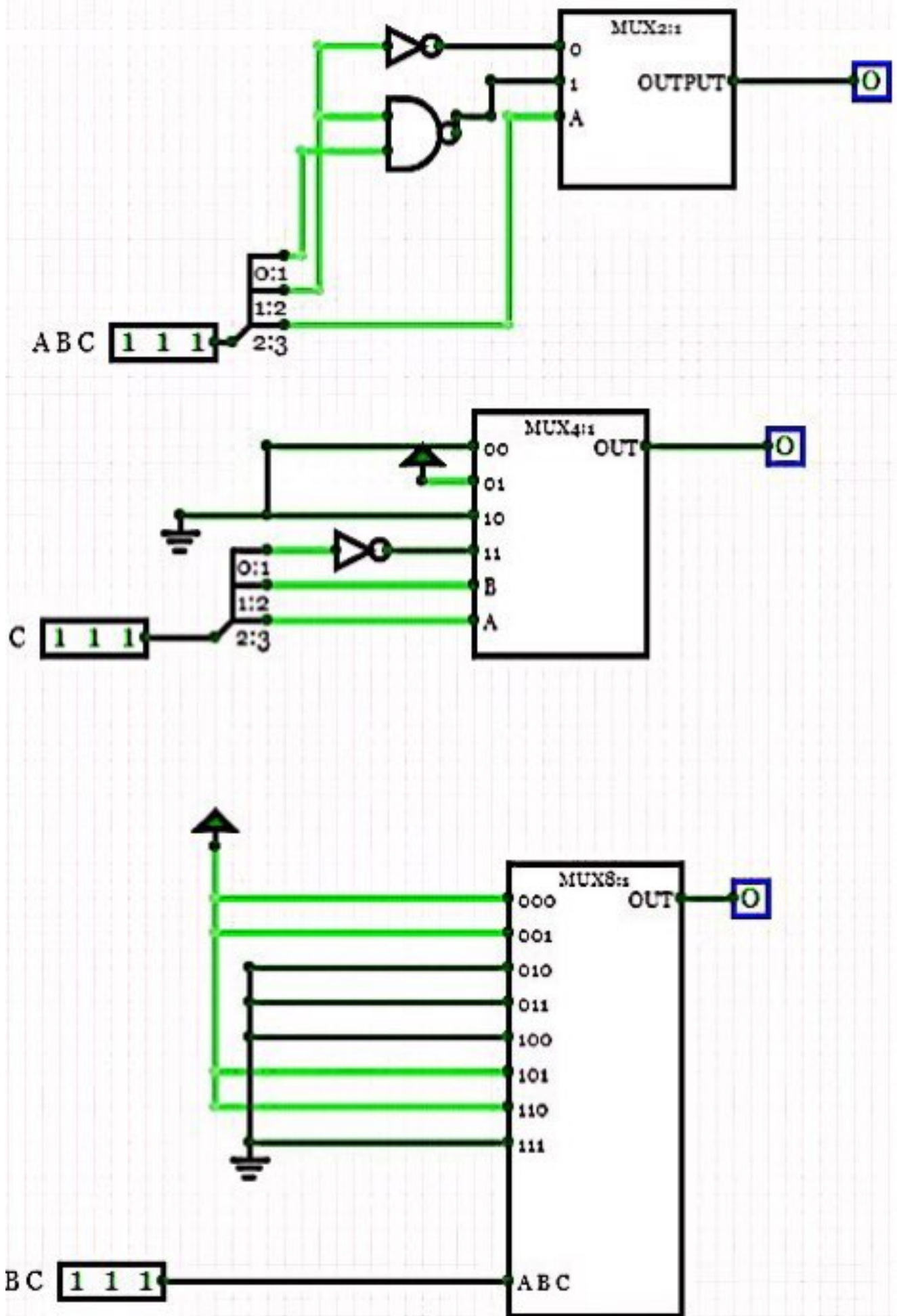


TABLA 02



Ejercicio 03  
Tabla 01

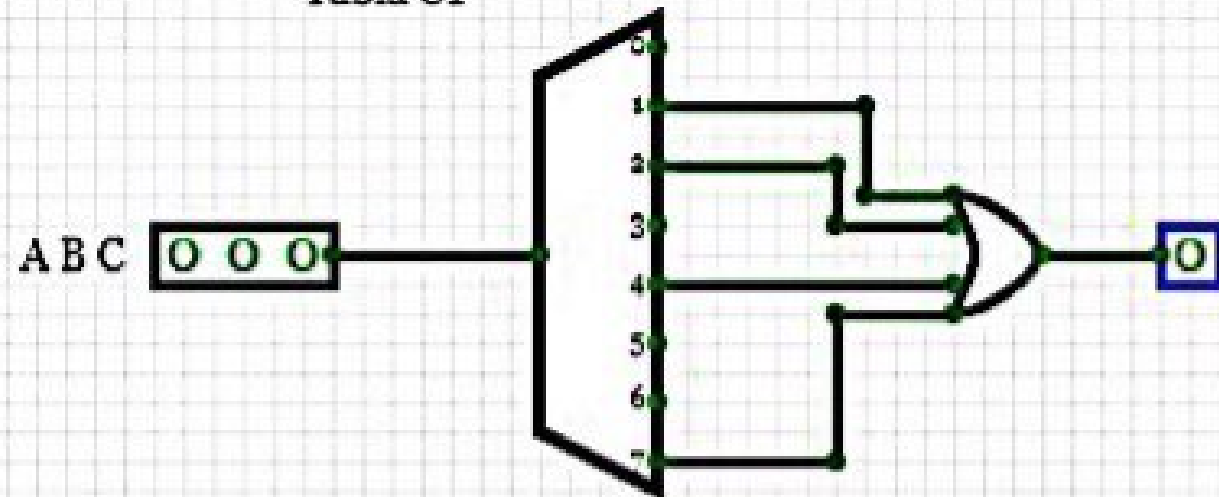
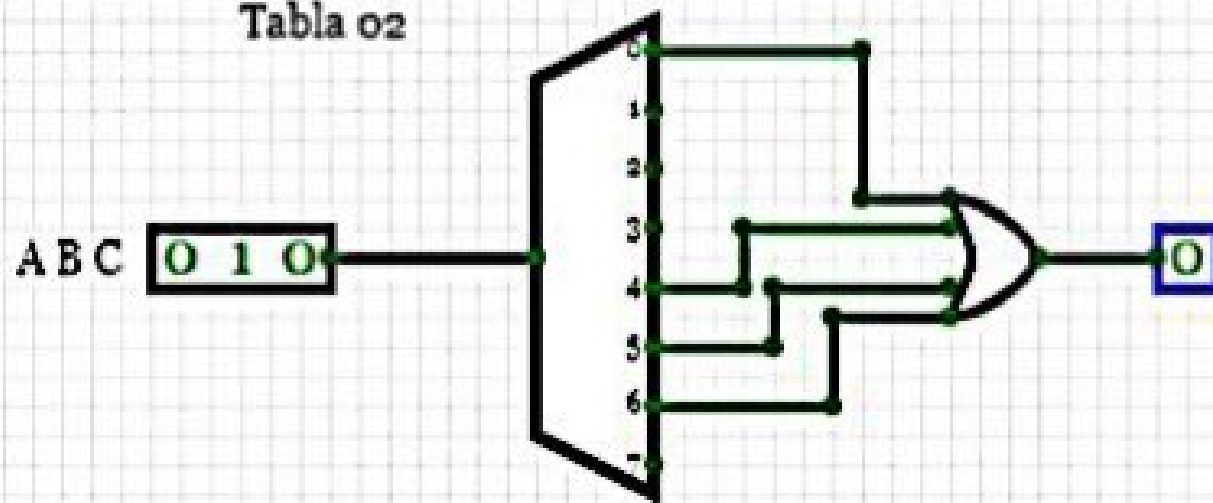
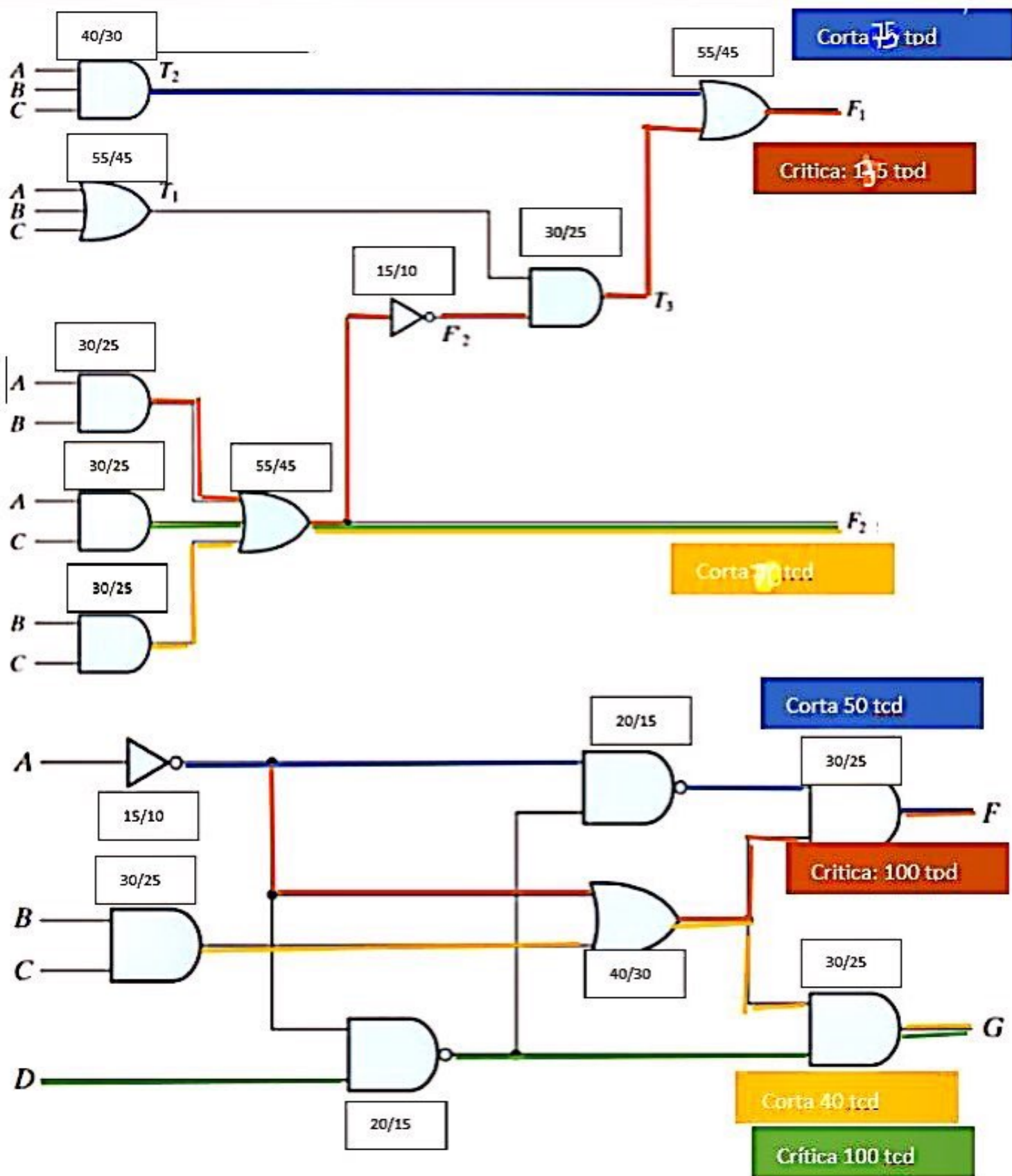
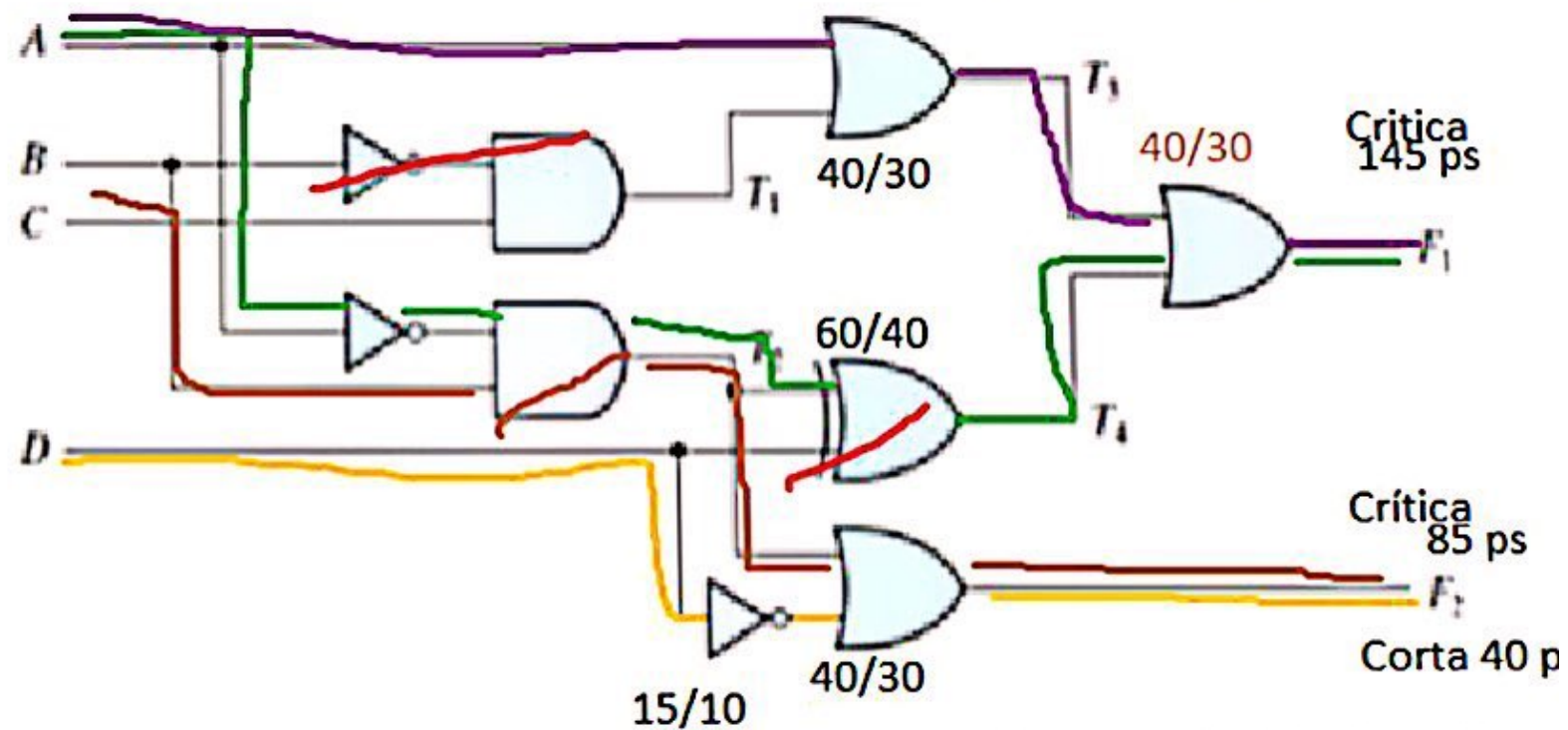
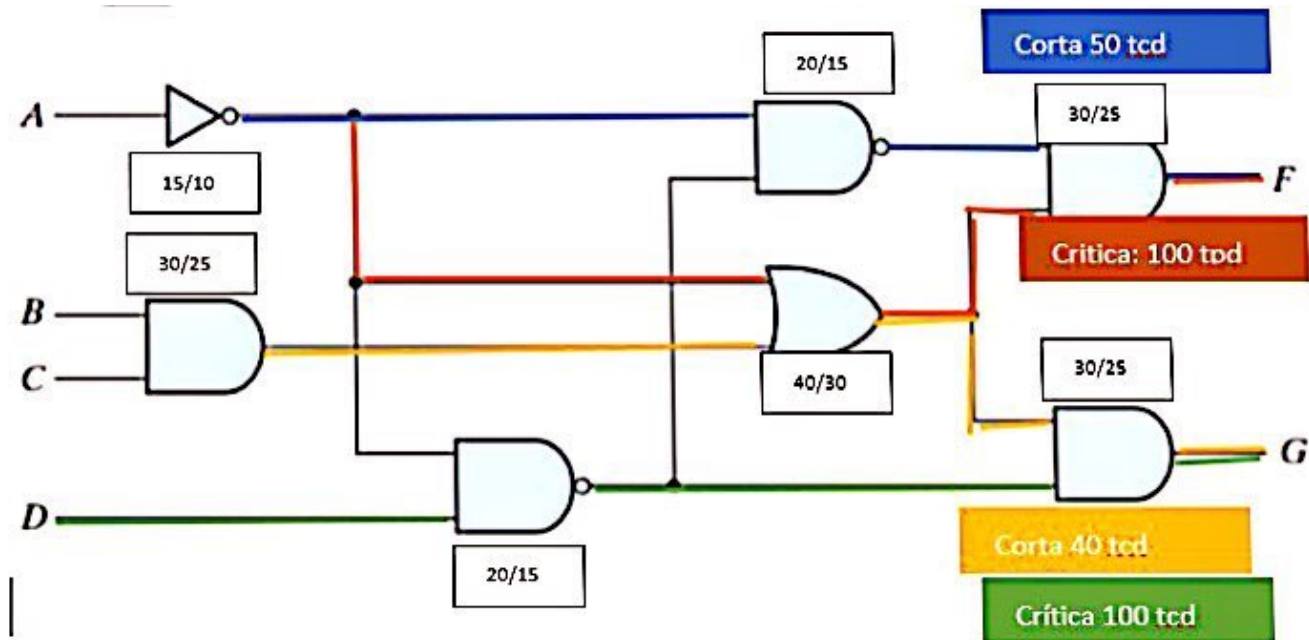


Tabla 02









SST

testbench

Type Signals

reg b221  
reg b241  
reg b281  
reg c21  
reg c41  
reg c81  
reg c221  
reg c241  
reg c281

wire t1mux21  
wire t1mux41  
wire t1mux81  
wire t2mux21  
wire t2mux41  
wire t2mux81

Filter:

Append Insert Replace

Signals

Time  
t1mux21  
t1mux41  
t1mux81  
t2mux21  
t2mux41  
t2mux81

Waves

