TCES 330, Spring 2025

Programmable Processor

Timelines:
Week 8: (ModelSim only) Design and testing of Datapath; (FINISH HW6!)

1. Design and testing of Mux2to1 module.
2. Design and testing of ALU module.
3. Design and testing of the RegisterFile module.
4. Design and testing of the DRAM module.
5. Design and testing of the submodule DRAM+RegisterFile.
6. Design and testing of the submodule RegisterFile +ALU.
7. Design and testing of the DataPath module.

Week 9: (ModelSim only) Design and testing of Control Unit; starting the combination of Datapath and Control Unit so the Processor is built

1. Design and testing of the DROM module.
2. Design and testing of the Finite State Machine.
3. Design and testing of the submodule PC+DROM+IR
4. Design and testing of the ControlUnit module
5. Combine the DataPath and ControlUnit, start the testing

Week 10: (Both ModelSim and Quartus) Testing the processor; fix bugs of the Quartus project; demo

1. Finish the testing of processor using ModelSim
2. Add other modules and test the processor using DE2 board
3. Demo (Thursday 06/05) or video submission (06/08)

Final exam: 06/12 (DE2 board must be returned on final exam day, or earlier)

Zip (project folder + Report) file due: 06/08