

## Programmable Processor

### General Comments:

This is a 3-week team project on which discussion starts in class. You will work in teams; one submission per group is required. The submission for this exercise will consist of your ModelSim files, a Quartus project, and a written report. Your written report should follow the [required format](#).

Make sure that all team members share proper amount of workload for this project as equally as possible. The work you turn in must come from your group only. Do not share your work with other groups.

### Problem.

- Implement the six-instruction programmable processor as discussed in class using SystemVerilog.
- Your Quartus project should be in a **folder called Project** and your top-level module should also be called **Project.sv**. Your top-level module will instantiate your processor module named **Processor.sv** and interface to the DE2 board as follows:
  - KEY[2] acts as your system clock; (so we don't wear out KEY[0])
  - KEY[1] acts as a synchronous system reset;
    - Note that reset will not be able to reload memory contents, but it should reinitialize your state machine and reset (clear) all your flip-flops. Notice your register file doesn't need reset signal.
  - Several internal variables are brought to the top-level for debug and display purposes. These include the program counter, the instruction register, state machine current state, both inputs to the ALU, and the ALU output.
  - HEX3, 2, 1, and 0 always display the current contents of the IR;
  - SW[17:15] work as selecting signals to determine what HEX 7, 6, 5, and 4 should display as follows:
    - 0 => HEX7, HEX6 = PC; HEX5, HEX4 = Current State; Note: for this to correspond to the values you set for your states, you should tell Quartus to use your state machine encoding.
    - 1 => HEX7, 6, 5, 4 = ALU\_A (A-side input to ALU)
    - 2 => HEX7, 6, 5, 4 = ALU\_B (B-side input to ALU)
    - 3 => HEX7, 6, 5, 4 = ALU\_Out (ALU output)
    - 4 => Next State (FSM next state variable, if you use one)
    - 5 Unused
    - 6 Unused
    - 7 Unused
  - Your top level module (**Project.sv**) should instantiate a processor module, a multiplexer for selecting displays (described above) and a key conditioner (described below). Your top level RTL view should look very close to the picture as shown in Figure 1 (**just for references!**).

- Load your translation of the given program (given in Lab4) into and Instruction Memory:

```
RF[0A] = D[1B] - D[2A] + D[3C] - D[7E];
D[6A] = RF[0A];
HALT
```

Data memory should initially contain

```
D[1B] = 0x21BA
D[2A] = 0xA04E
D[3C] = 0x71AC
D[7E] = 0xB17F
```

- A high-level ModelSim testbench will be provided (in a file called **testProcessor.sv**), so the **Processor.sv** module you turn in must use this signature (if your processor does not conform to this signature, change your processor, not the testbench):

```
module Processor( Clk, Reset, IR_Out, PC_Out, State, NextState, ALU_A,
ALU_B, ALU_Out);

input Clk;           // processor clock
input Reset;         // system reset
output [15:0] IR_Out; // Instruction register
output [7:0] PC_Out;  // Program counter
output [3:0] State;   // FSM current state
output [3:0] NextState; // FSM next state (or 0 if you don't use one)
output [15:0] ALU_A;  // ALU A-Side Input
output [15:0] ALU_B;  // ALU B-Side Input
output [15:0] ALU_Out; // ALU current output
```

You will want to run testbenches for your various modules, **but the runrtl.do and wave.do that you turn in should be reserved to run the given testbench as specified above.**

- Make sure that the In System Memory Content Editor can display the contents of your instruction memory and your data memory; it cannot be used on your register file memory.
- Try to make sure Quartus recognizes your processor state machine (as a state machine) by following the [FSM template file](#). Note that there will be a second state machine in your Quartus design: the **ButtonSync** state machine. In Quartus State Machine View you can select which state machine to view in the upper left corner of the state machine window.
- Data memory should be a 256 X 16 Quartus RAM LPM with Memory Content Editor enabled.
- The Register File (16 X 16) should be implemented with System Verilog as discussed in class.

- The ALU is assigned in Lab4.
- The Instruction memory should be a 128 X 16 Quartus ROM LPM with Memory Content Editor enabled.
- The controller state machine should be designed and tested as discussed in class.
- Run TimeQuest and include the .sdc file in your Quartus project. Note that there will be two clocks in this project (the 50 MHz clock for the key conditioning circuits and the processor clock derived from the KEY), as we discussed in class.
- A ModelSim testbench, i.e., **testProcessor.sv**, will be provided. Run this testbench and include a screen shot of the ModelSim Transcript area where the results are printed in your report. Of course you can also include the waveforms in your report, if you wish along with other tests that you might have used.
- Write your report using the same outline as before. You know by now to be very explicit and detailed about your test procedure and test results; go back and review the [sample lab report](#). Photographs are allowed!

#### **When you are done with your project.**

Zip your project folder, plus your written report, into a zip file (the exact name of the zip file is not critical, but should contain the name of at least one of your team members). When I open your zip file, I should see a top-level folder called **Project**, and a report file (either .doc or .pdf is fine). Make sure that you turn in all files necessary for the project and that these files are in the proper locations for compilation. It's a good idea to test this by unzipping your files to a new location and recompile using Quartus. Make sure that the correct \*.mif files get loaded and that the In System Memory Content Editor can find the data in your memories; this is often a source of difficulties. Submit the complete package on Canvas by the due time.

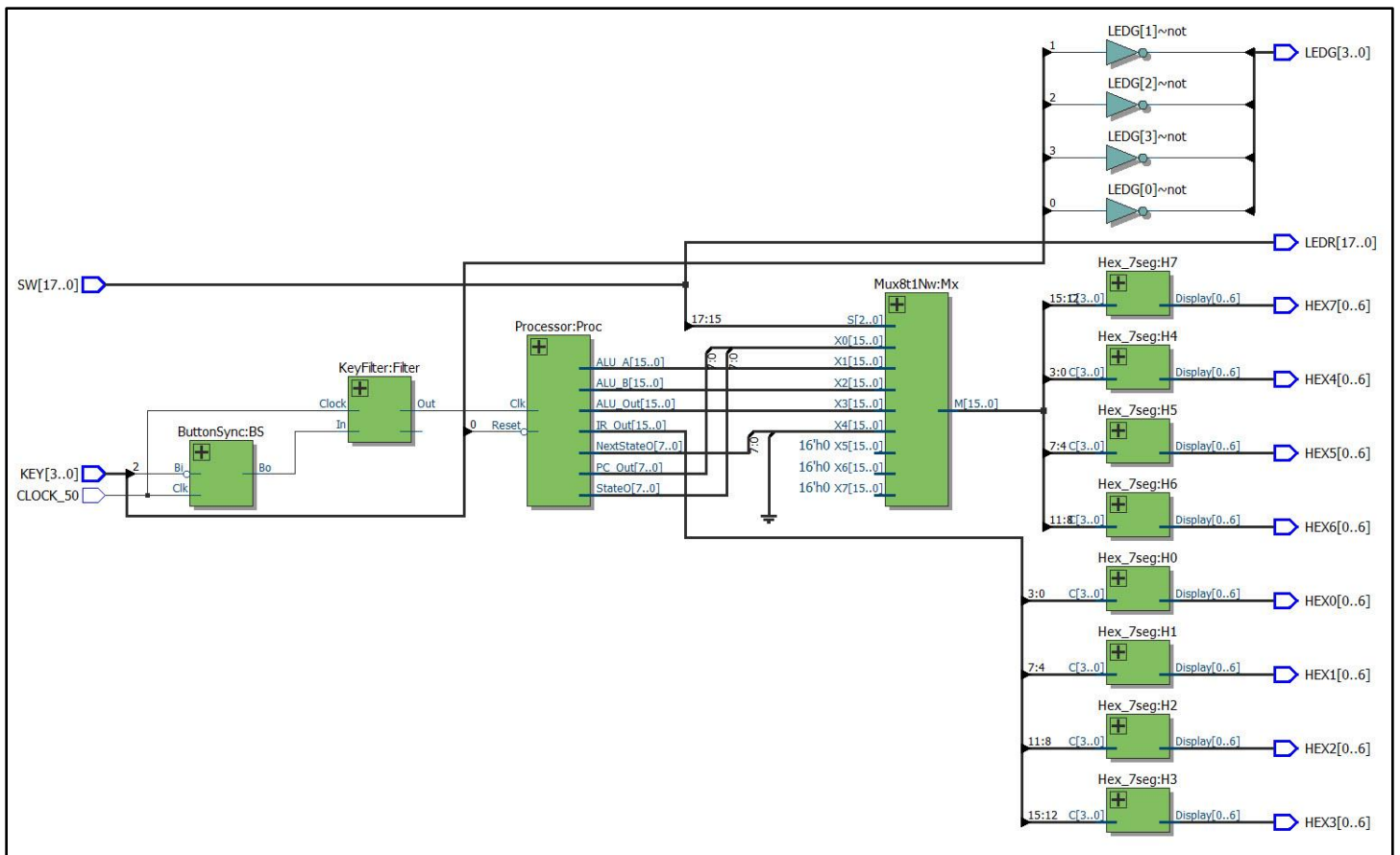


Figure 1. Top-level RTL View (for reference only)

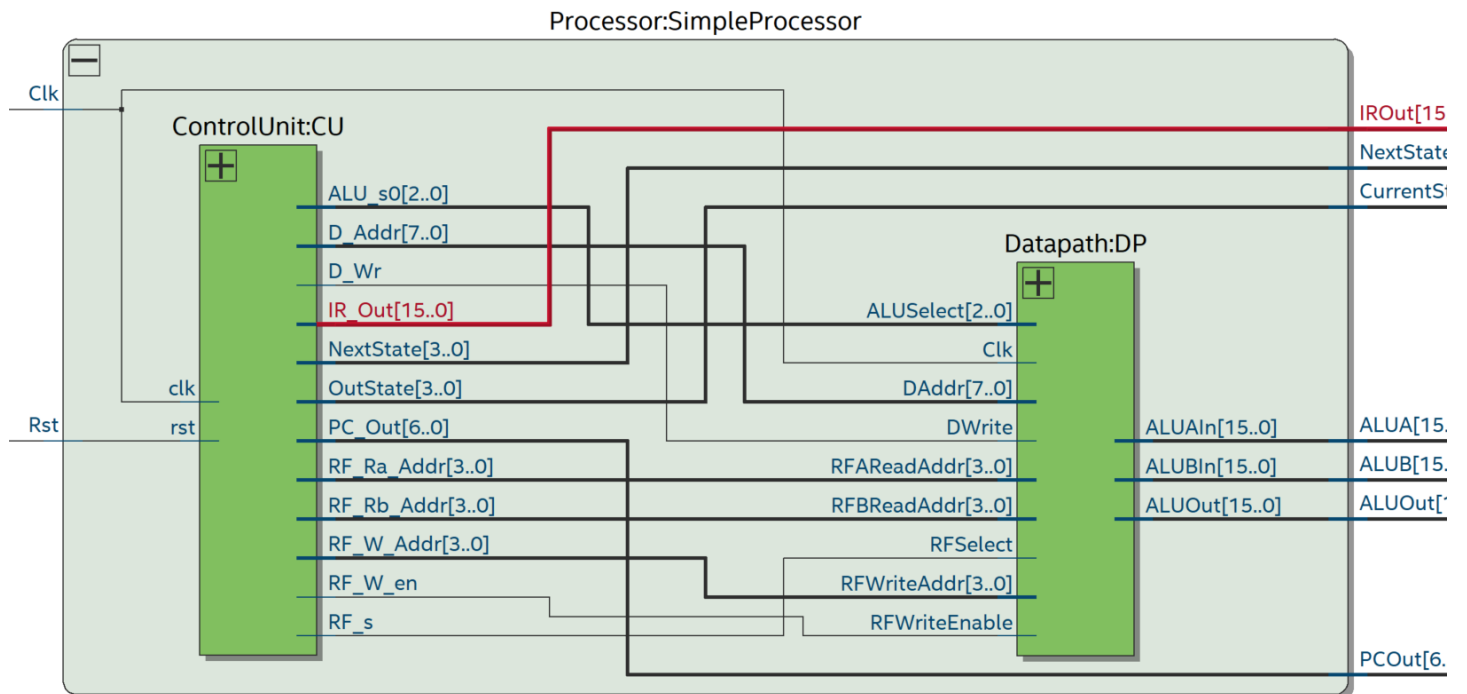


Figure 2. Processor View (for reference only)

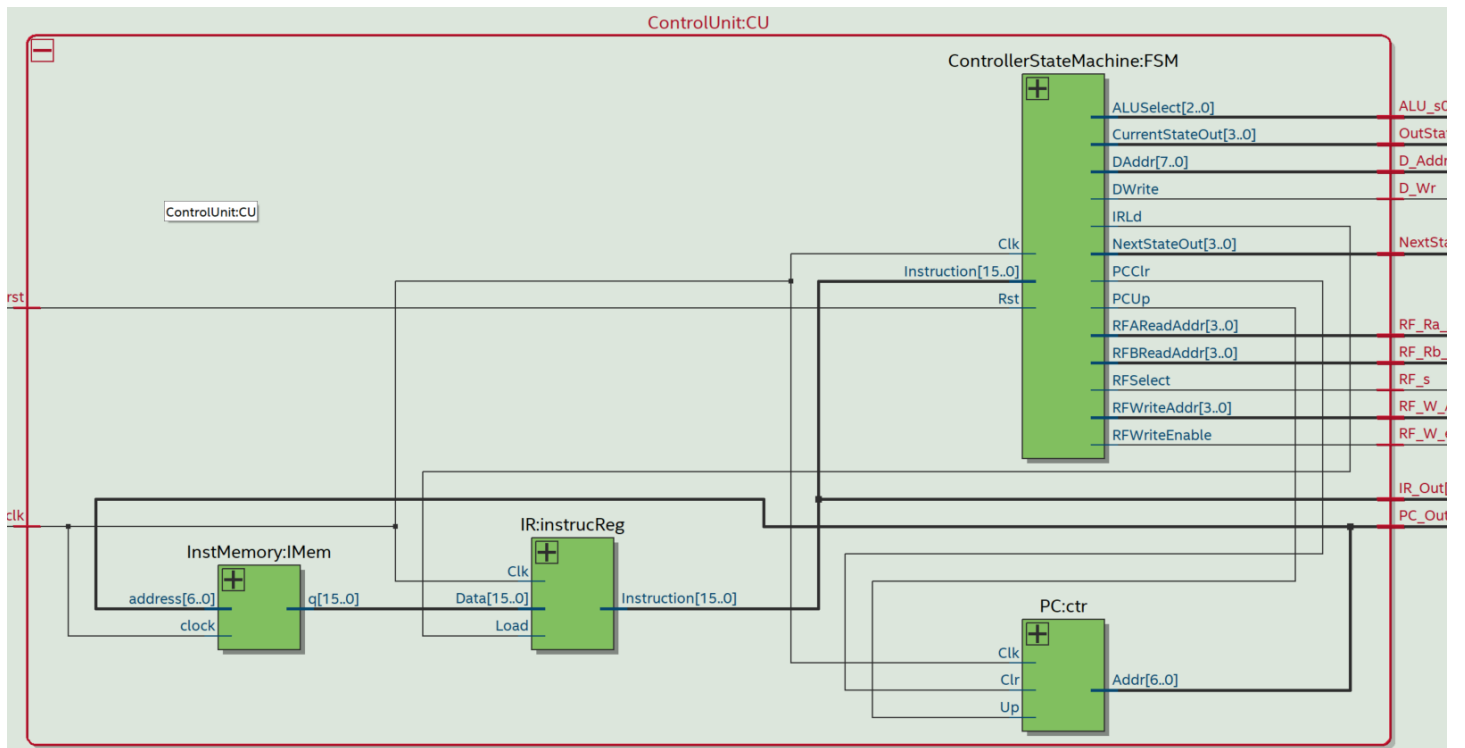


Figure 3. Control Unit View (for reference only)

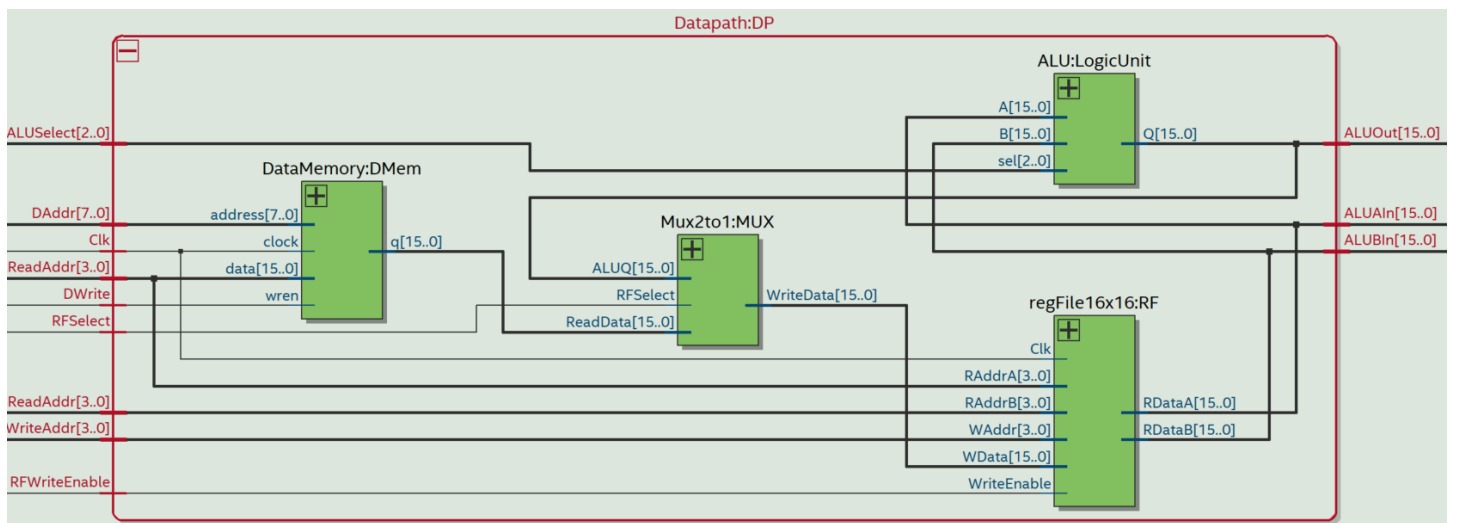


Figure 4. Datapath View (for reference only)