Course Project

Programmable Processer

TCES330 Digital System Design

Spring 2025

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Appendix

Before you start reporting the details involved in this course project, first briefly talk about the purpose of this project; then introduce your team members and how you manage the workload.

**1.Requirements**

Briefly describe the project requirements in general. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. See below.

Add your picture here

Figure x. Brief describe the picture you insert here, e.g., Processor Structure, etc

* 1. **Requirements for Controller.sv**

Briefly describe design requirements for the module **Controller**. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references.

* 1. **Requirements for Datapath.sv**

Briefly describe the design requirements for the module **Datapath**. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references.

* 1. **Requirements for Processor.sv**

Briefly describe the design requirements for the module **Processor**. Use pictures/figures is always a good idea. When using pictures/figures, please add captions for references.

* 1. **Requirements for Project.sv**

Briefly describe the design requirements for the top-level module **Project** (by adding other modules like **Buttonsync**, **Keyfilter**, **Decoder**, **Mux\_nW\_8\_to\_1** to the **processor**). Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references.

**2. Design**

Describe in detail the project modules’ design procedure. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references.

**2.1 Controller.sv**

Describe in detail the design of the **Controller** module. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. If you think certain segments of the SystemVerilog codes can reflect your design idea, you can add them here for discussion too (and don’t forget to add captions).

**2.2 Datapath.sv**

Describe in detail the design of the **Datapath** module. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. If you think certain segments of the SystemVerilog codes can reflect your design idea, you can add them here for discussion too (and don’t forget to add captions).

**2.3 Processor.sv**

Describe in detail the design of the **Processor** module. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. If you think certain segments of the SystemVerilog codes can reflect your design idea, you can add them here for discussion too (and don’t forget to add captions).

**2.4 Project.sv**

Describe in detail the design of the top level **Project** module. Discuss the usage of submodules including Button Synchronizer, Key Filter, etc. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. If you think certain segments of the SystemVerilog codes can reflect your design idea, you can add them here for discussion too (and don’t forget to add captions).

**3. Test Procedures and Results**

Describe in detail the testbench design of each module. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. If you think certain segments of the SystemVerilog codes can reflect your design idea, you can add them here for discussion too (and don’t forget to add captions).

Also please include the simulation results by running each testbench. Comment properly on whether the testing results meet the design requirements presented in **Section 1: Requirements**.

**3.1 FSM\_tb**

Describe in detail the design of FSM testbench. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. If you think certain segments of the SystemVerilog codes can reflect your design idea, you can add them here for discussion too (and don’t forget to add captions).

**3.2 Controller\_tb**

Describe in detail the design of the Controller testbench. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. If you think certain segments of the SystemVerilog codes can reflect your design idea, you can add them here for discussion too (and don’t forget to add captions).

**3.3 Datapath\_tb**

Describe in detail the design of the Datapath testbench. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references. If you think certain segments of the SystemVerilog codes can reflect your design idea, you can add them here for discussion too (and don’t forget to add captions).

**3.4 testProcessor**

The Processor testbench, **testProcessor.sv** will be provided. Show your understanding of the test bench. If you have ever tried anything different from the given version, properly talk about it and explain why your version is a reasonable (or preferable) alternative.

**4. DE2 Board Test Results**

Provide your observations through project testing on DE2 board. If you or your group ever encountered some warning messages, or error messages during Quartus compilation, how your group solved the problem and removed those warning/error messages. Using pictures/figures is always a good idea. When using pictures/figures, please add captions for references.

**5. Conclusion**

Provide a summary of your learning from the course project, learning of course subjects, as well as learning from the teamwork experience.

**6. References**

List documents/materials/webpages you and/or your group referred to when you work on this project and when you write this report.

**Appendix**

If you and/or your group has some extra information/work to share, please put it in this section. As an example, if you tried the extra credits part, you can have description and discussion on those contents here.