A compact size, 64-channel, 80 MS/s, 14-bit dynamic range ADC module for the PANDA Electromagnetic Calorimeter

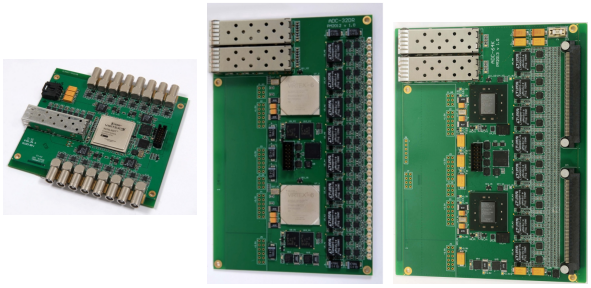
Abstract

A compact size, 64-channel, 80 MS/s, 14-bit dynamic range ADC module for the electromagnetic calorimeter of the PANDA experiment was developed and used for testing in various detector readout set-ups [1]. To minimize cabling bulk, the modules are planned to be placed inside the PANDA detector volume, where they will be exposed to magnetic field of up to 2 T and a non-negligible radiation flux. The module performs signal filtration, extracts important signal parameters and allows for resolving and parametrizing overlapping pulses. A dual FPGA structure and a hardwired arbitration circuit allows for resolving potentially catastrophic situations caused by radiation-induced (SEU) configuration damages. The FPGAs are prepared for self-detection and recovery from SEU. Processed data are pushed to the optical links running at 2 Gbit/s. The ADC module is compliant with a "Synchronization Of Data Acquisition" (SODA) System, which allows for obtaining defined latencies with a reference time accuracy of 50 ps [2]. The paper describes construction details and test environments. The results of performance test, including dynamic range, linearity, magnetic field and preliminary radiation sustainability are also presented.

1 Introduction

The Electromagnetic Calorimeter (EMC) of the Anti-Proton Annihilation at Darmstadt (PANDA) experiment at the Facility for Antiproton and Ion Research (FAIR) consists of over 15000 lead tungstate (PbWO4) crystals and is designed for detection and parametrization of particles with kinetic energies up to 12 GeV. For accurate reconstruction of events in the PANDA detector, a correct merging of energy spills as low as 3 MeV in the calorimeter crystals is desired. This requires front-end electronics with 14-bit dynamic range. Since the experiment will essentially be triggerless, the event-building and data selection will be performed on-line. All detector signals will need a continuous high-speed sampling and autonomous pulse detection and parametrization systems. Due to a close to $4\,\pi$ coverage of the solid angle by the active detector material, the cross-section of the opening holes in the detector's construction does not allow for routing of all individual signal cables outside of the detector. Therefore it was decided to locate the ADCs in a confined space within the detector, where the devices will perform the digitization and extraction of important features of signals, like pulse amplitudes, integrals and times to be sent to the Data Acquisition System (DAQ) over optical links. The ADC system will be exposed to ionizing radiation and a magnetic field of a flux density reaching 2 T.

The limited space provided in the detector for the ADC system requires high channel density and liquid cooling of the devices. In order to define the optimal design for the task, a number of different 14-bit sampling ADC modules were constructed, see Fig. 1.



(a) (b) (c)

Figure 1: ADC portfolio.
(a) 16-channel, 125 MSPS, Virtex-5 based
(b) 64-channel, 80 MSPS, Virtex-6 based
(c) 64-channel, 80 MSPS, Kintex-7 based

The ADC portfolio includes a 16-channel, 125 MS/s table-top module, a 64-channel, 80 MS/s dual-range high-end module and a 64-channel, 80 MS/s economy module [**?**].

2 Module construction

The 64-channel ADCs are equipped with symmetrizing shapers/amplifiers allowing for user defined CR-$(RC)^3$ filter configurations. In configurations with by-passed CR-$(RC)^3$ filter, the input analog stage features over 100 MHz bandwidth. Obtaining a 14-bit dynamic range required by the PANDA experiment was found to be feasible through using a dual-range ADC structure. By fitting SMD jumpers, a 32-channel dual range configuration can be obtained. Amplified signals are processed by a set of 8-channel 14-bit, 80 MS/s analog-to-digital converter circuits, see Fig. 2

Digitized samples of 64 analog signals are sent to 2 FPGAs using 128 LVDS links running at 560 Mbit/s each. The FPGA firmware performs signal filtration, and ex-

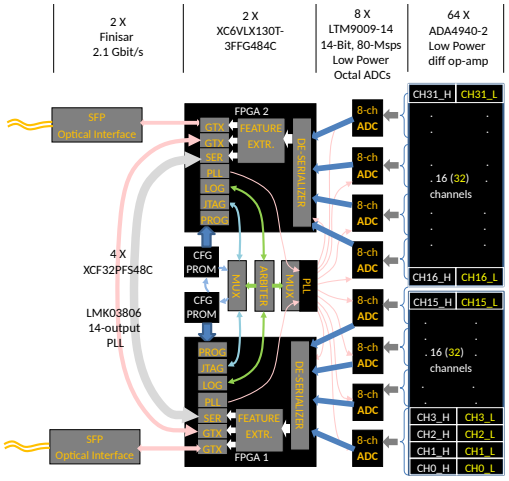


Figure 2: Hardware structure of the PANDA Sampling Analogue-to-Digital Converter board (SADC).

tracts important signal parameters, such as time of arrival, amplitude and integral. The data assembled in output registers are pushed to the optical links via multi-gigabit transceivers (GTX) running at 2 Gbit/s. Depending on data rate and firmware configuration, it is possible to use either both optical links, which are independently controlled by 2 FPGAs or use only one optical link and inter-FPGA serial or parallel data connections. The ADC module is compliant with the SODA System, for which the reference clock is distributed via a DAQ, using the down-link part of the ADCs optical transceiver. It allows for obtaining defined latencies with a reference time accuracy of 50 ps [2]. The received reference clock signal is routed out from the FPGAs and processed by a 14-output PLL/jitter cleaner circuit, providing a set of stable clocks for all digitizers as well as for all GTX inside FPGAs. A dual FPGA structure and a hardwired arbitration circuit provide routing of the JTAG configuration signals to the FPGAs and control of the reference clock source. This allows for resolving potentially catastrophic situations, when a content of a configuration memory is damaged by radiation in such a way that the loaded configuration affects the communication chain, thus locking the possibility for a remote repair of the faulty content. The dimension of 64-channel modules amounts to 100 mm × 150 mm, including the area designated for DC/DC converters. Despite a high channel density, no measurable crosstalk has been observed. The proximity of specially designed DC/DC converters also doesn't give any measurable rise to the signal noise. The power consumption amounts to 22 W for the Kintex-7 version and 27 W for the Virtex-6 version. This requires efficient cooling, which in the PANDA will be accomplished by liquid-cooled aluminum encapsulations.

3 ADC test and measurement setup

The test setup was based on a firmware developed for the Crystal Barrel experiment at the Bonn University. The firmware allows self-triggering with variable threshold, as well as external trigger and network-based trigger. Several algorithms for pulse integral determination, peak-sensing and digital constant fraction discrimination allow to characterize the waveform such that it's properties can be determined efficiently with regards to memory and bandwidth. Additionally, the transmission of full samples with a length of 12.8 µs is possible for

any channel. With the versatile AXI interface, the data-streams are handed over to a 1GB/s UDP/IP core, based on an open source code (opencores.org, BSD). The usage of Ethernet with UDP/IP has allowed for a great simplification of lab setups, introducing the possibility to directly connect the SADC to a computer. Data taking as well as configuration can be done within one simple framework, see Fig. 3. The setup was used for evaluation of the detector sensitivity and noise, as well as for performance analysis of the ADC module.

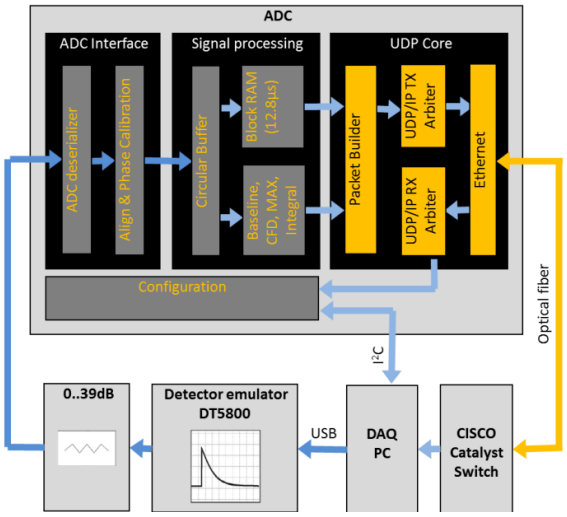


Figure 3: ADC and detector performance test setup.

4 Performance of the ADC analog stage

Given the light yield of the PbWO4 crystals, the quantum efficiency, the gain of the photo-sensors, as well as the pre-amplifier gain, the signals amplitude at the ADC inputs corresponding to energy depositions of 1 MeV to 12 GeV will range from 160 µV to 2.2 V respectively. To achieve a high resolution of the ADC, every detector signal is processed by a high-gain and a low-gain channel, see Table. 1. The noise,

Table 1: ADC analog performance.

Parameter	Low Gain	High Gain
Gain	0.5	7.2
Input amplitude	$< \pm 2.2$ V (0 – 12 GeV)	$< \pm 0.14$ V (0 – 1 GeV)
Noise	1.3 mV (8 MeV)	0.08 mV (0.5 MeV)
Bandwidth	> 100 MHz	> 20 MHz
Linearity	0.6 %	
Amplitude Resolution	< 0.1 %	
Charge Resolution	< 0.1 %	

linearity, amplitude and charge resolution figures were measured at Ruhr-University Bochum with the help of a detector emulator device (CAEN DT5800), which was configured to deliver pulses comparable to the preamplifier signals in the experiment. The ADC was set to a self-triggered mode of operation. The baseline was calculated using the moving average of 200 samples preceding the signal. The RMS noise of the ADC in high-gain channels amounts to 0.08 mV (0.5 MeV), while the baseline amplitude distribution has a white noise character and does not show signs of the interference from the digital part of the device, see Fig. 4.

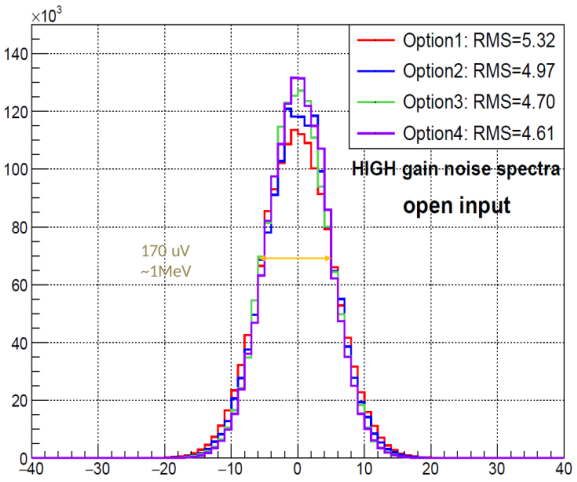


Figure 4: The ADC noise with optional high-pass filters. With 58 bins per 1 MeV in the high-gain channel, the RMS noise amounts to 80µV.

5 Performance of the ADC sampling

- Example of a digitized waveform with a light pulser Fig. 5.
- Example of a digitized waveform with cosmics.
- Example of a digitized waveform with a neutron/proton/gamma beam.
- Time/Energy resolution for each example.
- Different waveforms for several energy values and Low/High gain could be shown.

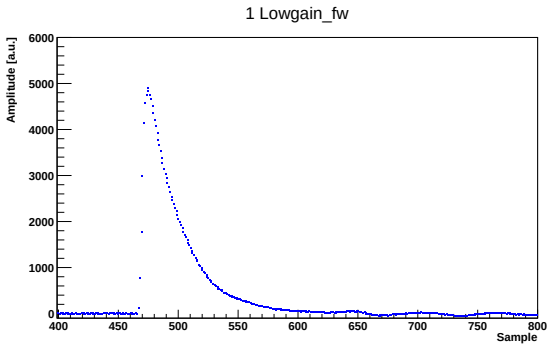
6 Analog and digital signal filters

This part of the design is under evaluation with the goal to detect energy spills as low as 3 MeV as well as resolve and parametrize signal pileups occurring with down to 200 ns time separation with the best achievable time and energy resolution. Detecting the weakest signals requires signal filtration, while the optimal filter parameters depend on the expected particle rate in the detector. In case of low rates, adequately longer signal shaping constants result in better signal to noise ratio, hence in better energy resolution and wider dynamic range, see Fig. 6. Signal filtration methods for higher rates as well as multiple pulse detection and parametrization using Moving Window Deconvolution (MWD), Moving Averaging (MA) and Constant Fraction Timing (CFT) were developed and tested at KVI-CART, Groningen, The Netherlands [3]. The ADCs were successfully tested with a readout system running the SODANET protocol.

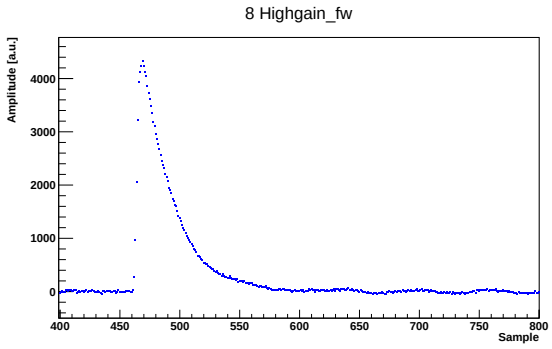
7 Feature Extraction Firmware on the SADC module

The feature extraction algorithm was designed for implementation on the developed SADC module, which is required to process signals at high interaction rates. The signal filters mentioned in a previous section are used for efficient signal processing during the feature extraction procedure.

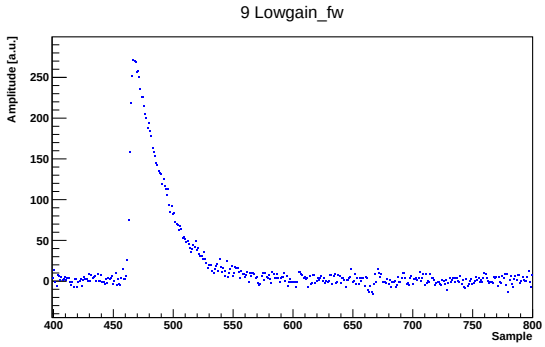
Implementation of the feature extraction



(a) Lightpulser, Lowgain 2.2V (12 GeV).



(b) Lightpulser,Highgain 48mV (262 MeV).



(c) Lightpulser, Lowgain 48mV (262 MeV).

Figure 5: Waveforms example.

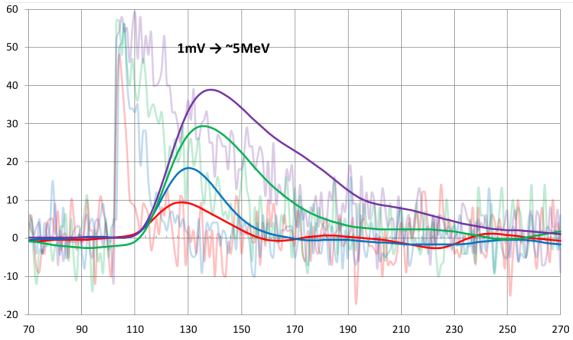


Figure 6: A 1 mV analog signal (corresponding to 5 MeV energy deposition).

algorithm on the FPGA is done in VHDL. The signal-processing logic is shown as a block diagram in Fig. 7. The digitized waveforms from high and low gain ADC channels, i. e. pulses, are simultaneously processed by the feature extraction algorithm.

At the beginning the high (low) gain signal from ADC is sent to the Infinite Impulse Response (IIR) filter, which is similar to the MA filter. They are both used for signal smoothing and noise reduction leading to precise pulse detection at lower thresholds. There is possible to select by the slow control system which of them will be used for the feature extraction.

Thereafter the data flow is processed in parallel by two filters: MWD-long and MWD-short, which are represented by the MWD block on the diagram. Both fil-

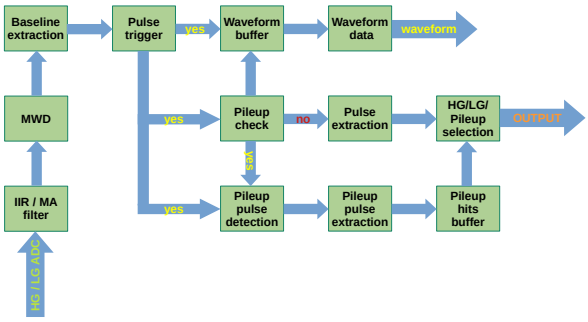


Figure 7: The block diagram of the feature extraction algorithm implemented on the FPGA of the sampling ADC.

ters are used to reduce a trailing edge of waveforms. The MWD-long filter produces a trapezoidal shape from the original waveform, and the MWD-short makes this trapezoid even shorter comparing to the MWD-long. Thus, these filters reduce the processing time of the waveform, which decreases the probability of signal pileup at high data rates. The baseline determination is done in the next module, called Baseline extraction, where a baseline value is subtracted from the ADC signal provided by the previous filters.

A corrected signal is sent to a Pulse trigger module, which checks if this signal is above the set threshold. Once it happens, the baseline extraction module is inhibited while a sample value of waveform is above 1/2 (1/4) of the threshold. This signal that pulse is active, a length of the active pulse and a maximum sample value of waveform (amplitude) are sent to a Pileup check module in case of the MWD-long branch. This module performs several functions using this input data. Firstly, it discards the digitized waveforms, which are too short or too long for further processing; secondly, it checks if the high gain signal is clipping, then the low gain signal is taken; thirdly, an integral value of pulse is calculated; and, finally, it determines that a pileup has occurred if an integral/amplitude ratio of pulse is bigger than a certain value. If a single pulse was detected, the feature extraction happens in a Pulse extraction module. This module is responsible for energy and timestamp determination. An energy of the pulse can be defined by the amplitude or integral of the pulse. The timestamp is found using the CFT filter. The pulse is discarded if the time information cannot be extracted. The obtained pulse data, time and energy, with a current superburst number are sent to a Data Concentrator (DC).

The signal from the MWD-short branch (pileup branch) is taken as the output only in case of pileup detection by the Pileup check module. The pulses have to be again detected by a separate module of pulse detection (see Fig. 7), and can be discarded if they are too short even for the pileup branch. All single pulses, which were found in pileup, are stored in a Pileup hits buffer. When the waveform is regarded as valid pileup case this buffer data is sent to the output.

This feature extraction algorithm also provides possibility to save a waveform signal after the pulse detection in parallel with feature extraction procedures. The waveform data can be stored in a raw format (without baseline correction). This feature is used for the self-tests or offline data analysis.

8 Slow control system

As it was mentioned before the ADC module can be configured via the slow control system, which sets all the feature extraction parameters: thresholds, pileup rejection values, readout regimes and etc. The example of the readout setup for the ADC module, which provides slow control, was realized on a TRBv3 board.

This board has five FPGA units, which can be programmed to perform different functions. In our case they were used as a SODA source, a UDP converter and the DCs. Allocation of these firmware modules on the TRBv3 board is shown in Fig. 8.

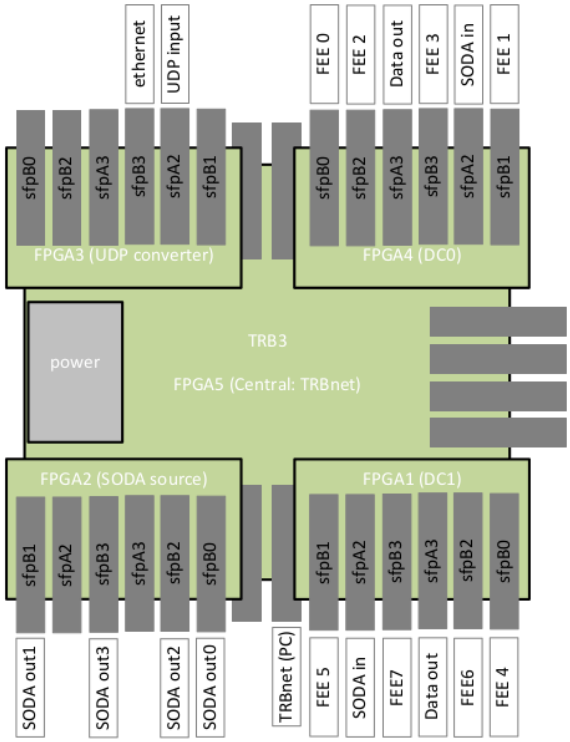


Figure 8: Firmware structure of the TRBv3 board.

The main FPGA unit in the center is responsible for providing communication between the residual FPGA units. The slow control system located at user's PC sends a package of commands to the UDP converter which is read by the central FPGA. Once it has the addresses of the devices, it starts to communicate with them. First, a synchronization signal generated by the SODA source is propagated through the whole readout components. The received device configurations and the obtained SODA signal, which provides the reference clock, are sent to the DC modules distributing them between attached front-end electronics, the SADC modules in our case.

If unexpected outage happens, the DC modules are programmed to keep register information and contentiously provide it to the SADC modules, which secures the stability of data taking and helps during recovery processes of the ADC firmware.

9 Test of the ADC module in a test beam environment

The ADC was used in a detector setup for testing response of EMC Forward End-Cap PbWO4 crystals to photons with energies from 10 MeV to 62 MeV. In the experiment performed at Max Lab III in Lund, 2014, a 3 x 3 matrix of crystals was equipped with Hamamatsu R11375 Vacuum Photo-Tetrodes (VPTT) and SP883d signal preamplifiers from the University of Basel [4]. The signals were processed by the Virtex-6 ADC version equipped with 300ns input shaping filter. The waveform data

were transferred to a PC via a VME-based Data Concentrator module (ATLB) [5]. After off-line energy reconstruction and applying 1.5 MeV thresholds, the relative energy resolution obtained for photon energies of 11 MeV, 26 MeV, 38 MeV and 62 MeV was found to be fulfilling the Technical Design Report requirements of the PANDA EMC with a safety margin, Fig. 9.

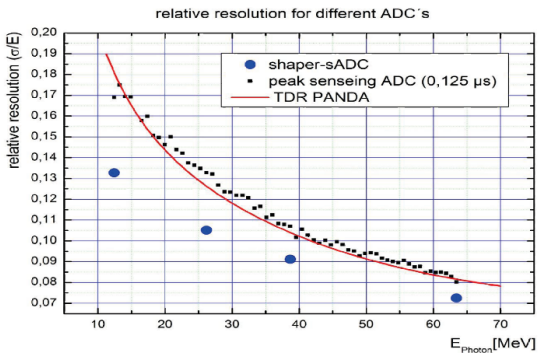


Figure 9: Calorimeter energy resolution for low energy photons.

10 Neutron irradiation of the ADC

In order to test the endurance of the ADC in a radiation environment, the Kintex-7 version of the device was irradiated with a neutron beam at The Svedberg Laboratory (TSL), Uppsala University in June 2016. The purpose of this experiment was to find the cross section of the device for the SEU-induced bit errors and estimate the Mean Time Between Failures (MTBF) of the device when placed inside of the operating PANDA detector. The neutron beam was produced by directing a 180 MeV proton beam into a full-stop tungsten target. The ADC was first placed at the Standard User Position (SUP), perpendicular to the beam which had a diameter of 130 mm. The neutron flux Φ_n (>10 MeV) at this position amounted to $5 \times 10^5 - 10^6 s^{-1} cm^{-2}$ with the energy spectrum as shown in Fig. 10.

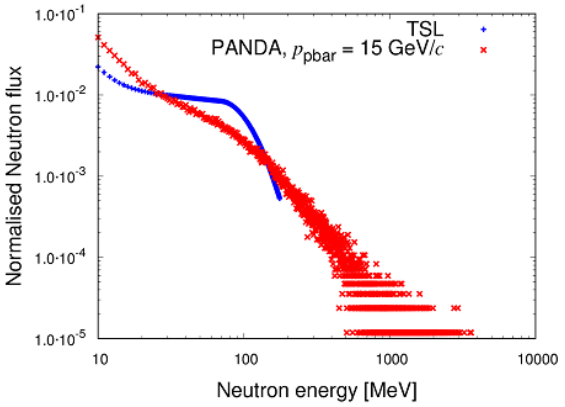


Figure 10: Neutron energy spectrum at the TSL (blue) and the anticipated in the $\overline{\text{P}}$ANDA (red).

During the experiment, the Xilinx Soft Error Mitigation (SEM) Controller was placed in the FPGA [**?**]. The SEM Controller has the ability to detect and correct different types of SEUs and its activity was monitored via a serial link. In this experiment, the SEM was automatically correcting Single-Bit Upsets (SBU) as well as Multiple-Bit Upsets MBU, spread over multiple frames in the FPGA memory (inter-frame). MBU located in the same frame (intra-frame) are not automatically correctable by SEM and require reconfiguration of the affected FPGA, which causes an FPGA dead time of the order of 200 ms. The occurrence of the SBU amounted to 69 %, inter-frame MBU – 26 % and intra-frame MBU – 5 %. After dividing the registered SEU number by beam time and nor-

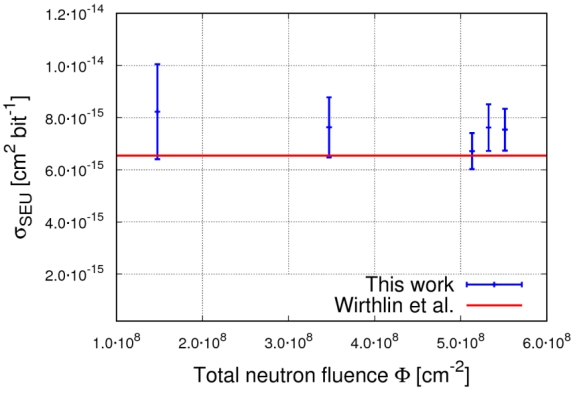


Figure 11: SEU cross sections of the ADC (FPGA) for neutrons.

malizing the result to the neutron flux we have obtained:

$$\sigma_{SEU} = \frac{N_{SEU}}{T_{MEAS} \cdot \Phi_n \cdot N_{BITS}} = \\ = 7.42 \cdot 10^{-15} cm^2 \cdot bit^{-1} \quad (1)$$

per FPGA, which is in agreement with the results achieved by a group of M. J. Wirthlin [6], see Fig. 11. In order to find the MTBF in PANDA, a simulation of the neutron flux in the EMC was made using a PandaRoot simulation package [7]. Given the beam momentum $P_{pbar} = 15\,\mathrm{GeV}/c$ and a luminosity of $L = 2 \cdot 10^{32} cm^{-2} s^{-1}$, the scaled neutron flux at the position of the digitizers in PANDA amounts to $\Phi_n = 150\ s^{-1} cm^{-2}$

11 Proton irradiation of the ADC

In November 2016 the ADC board was irradiated with a proton beam delivered by the AGOR cyclotron at KVI, Groningen. The beam was collimated with a 120 mm collimator, illuminating a top half of the digitizer board, including one of the FPGAs and SFP optical transceivers. Irradiations of an older prototype of the ADC, based on the Virtex-6 FPGA, have been performed at KVI-CART in the past [8]. The new measurements were done at proton energies of 80 MeV, 100 MeV and 184 MeV, allowing for studies of the energy-dependence of the SEU cross section.

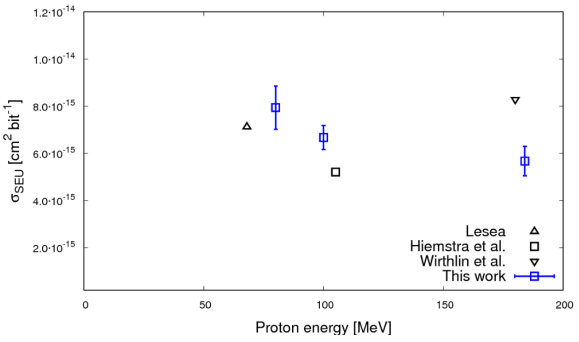


Figure 12: SEU cross sections of the ADC (FPGA) for protons.

By using the same analysis procedure as for the neutron-irradiation data, the obtained cross-sections for a Xilinx XC7K-160T FPGA are summarized in Table. 2. These results agree with previously reported measurements by Hiemstra et al., Leslea et al. and Wirtlin et al., see Fig. 12 [9],[10]. The total number of impact protons on the device during the proton irradiation session amounted to $1.12 \cdot 10^{10} cm^{-2}$. The flux of high-energy charged particles in the PANDA experiment at the location of the ADC modules was also simulated with the PandaRoot framework [8] and amounts to $\Phi_p = 60\ s^{-1} cm^{-2}$. The device was thus exposed to a dose equivalent of 6.5 years of detector operation at high luminosity. After the test, the device is still fully functional

Table 2: Cross sections for proton-induced SEUs at different beam energies for XC7K-160T.

E_{pbeam} [MeV]	σ_{SEU} $[cm^2 \cdot bit^{-1}]$
80	$7.94 \cdot 10^{-15}$
100	$6.67 \cdot 10^{-15}$
184	$5.67 \cdot 10^{-15}$

and no measurable degradation of performance was observed.

12 ADC recovery after irradiation

Recovery of the SADC board from the radiation damage requires time. Thus, the data, expected to arrive from a certain ADC module, will be lost. Hence, it is important to know how many data were lost for proper data correlation later. Therefore, another irradiation experiment was done at KVI in October 2018 to determine the recovery time after the SEU case.

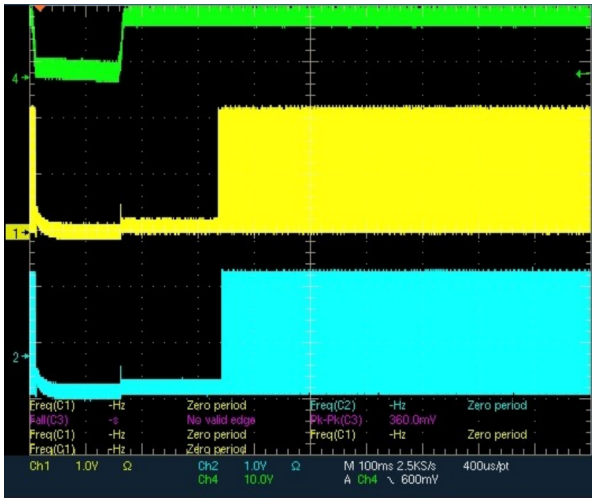


Figure 13: Reboot time of the power supply at the SADC: green line corresponds to the power supply clock, yellow and azure lines show the clock signal of the FPGA-1 and the FPGA-2 correspondingly.

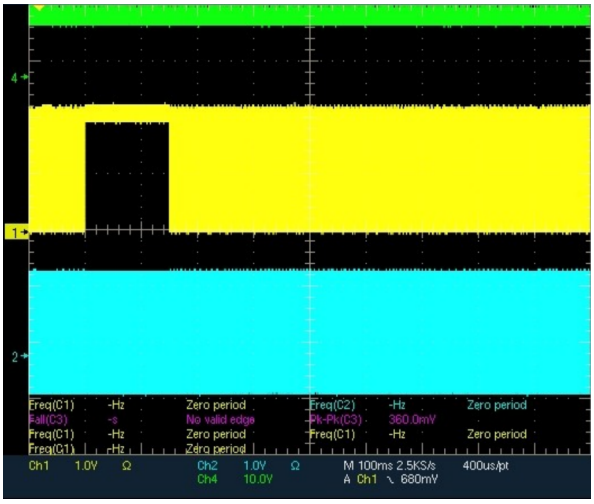


Figure 14: Reboot time of the FPGA at the SADC.

Depending on the place where the SEU has occurred, the SADC board can be fully or partially reset. In case if a power supply of the SADC module suffered from irradiation, the full reboot of the board is required. The mean time of the reboot when the main SODA clock is available for the power supply is 180 ms as shown in Fig. 13. Another possible scenario is damaging the firmware configuration, which was loaded to the FPGA memory. This problem can be resolved with re-configuring the FPGAs. Time, expected for this procedure, you can see in Fig. 14. For one FPGA it is around 150 ms in case of its reboot. Providing the clock does not mean the immediate data production. There is latency

existing between data production and the reboot time of the FPGA, what can be explained by fetching the configuration settings from the main DAQ system to the DC and further to the SADC board. This latency is shown in Fig. 15. On average, it is 15 ms. Thus, within the 200 ms the presented SADC board can back into full operation mode in both cases of the SEU occurrence, which means continuing data collection.

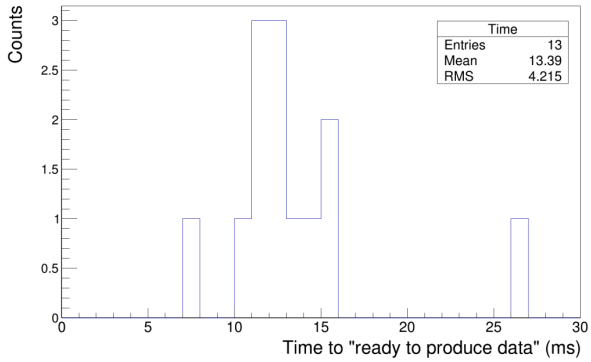


Figure 15: Latency of the SADC before data production.

13 Conclusion

A number of prototypes of the signal digitizer for EMC for the PANDA experiment were constructed and tested. The device was found to be fulfilling the requirements concerning performance and robustness described in the Technical Design Report. The device is ready for moving to a volume production phase.

References

[1] panda Collaboration. Technical design report for the panda electromagnetic calorimeter. 2008. https://panda.gsi.de/publication/re-tdr-2008-001.

[2] Igor Konorov et al. Time distribution system for the panda experiment. pages 1863 – 1865, 2009. https://doi.org/10.1109/NSSMIC.2009.5402172.

[3] G Tambave, M Kavatsyuk, E Guliyev, F Schreuder, H Moeini, and H Löhner. Pulse pile-up recovery for the front-end electronics of the PANDA electromagnetic calorimeter. *Journal of Instrumentation*, 7(11):P11001–P11001, nov 2012.

[4] I Keshelashvili, W Erni, F Müller, M Steinacher, and B Krusche. Development of low-noise / low-power preamplifier for the readout of inorganic scintillators and their mass production test system. *Journal of Physics: Conference Series*, 587:012024, feb 2015.

[5] P. Marciniewski, P. Pluciński, K. Fransson, L. Heijkenskojld, A. Kupść, J. Zlomanczuk, M. Wolke, H. Calén, T. Johansson, B. Hoistad, W. Erven, P. Wuestner, H. Kleines, V. Hejny, and D. Coderre. A trigger system based on fast sampling adcs - implementation and tests. *2011 IEEE Nuclear Science Symposium Conference Record*, pages 38–42, 2011.

[6] M J Wirthlin, H Takai, and A Harding. Soft error rate estimations of the kintex-7 FPGA within the ATLAS liquid argon (LAr) calorimeter. *Journal of Instrumentation*, 9(01):C01025–C01025, jan 2014.

[7] Johan Messchendorp. Computing activities for the panda experiment at fair. *J. Phys. Conf. Ser.*, 219:042016, 2010.

[8] M. Kavatsyuk, D. Bremer, P. Drexler, T. Eissner, M. Hevinga, T. Kuske, P.J.J. Lemmens, H. Moeini, T. Nishizawa, P. Schakel, F. Schreuder, R. Speelman, G. Tambave, and H. Löhner. Trigger-less readout of the panda electromagnetic calorimeter. In *2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC)*, pages 1796–1801, 2012.

[9] A. Lesea. A tale of two test chips : 28nm configuration ram and dual-port ram. in silicon errors in logic - system effects, March 2012.

[10] V. Kirischian D. M. Hiemstra. Single event upset characterization of the kintex-7 field programmable gate array using proton irradiation. in radiation effects data workshop (redw), July 2014.