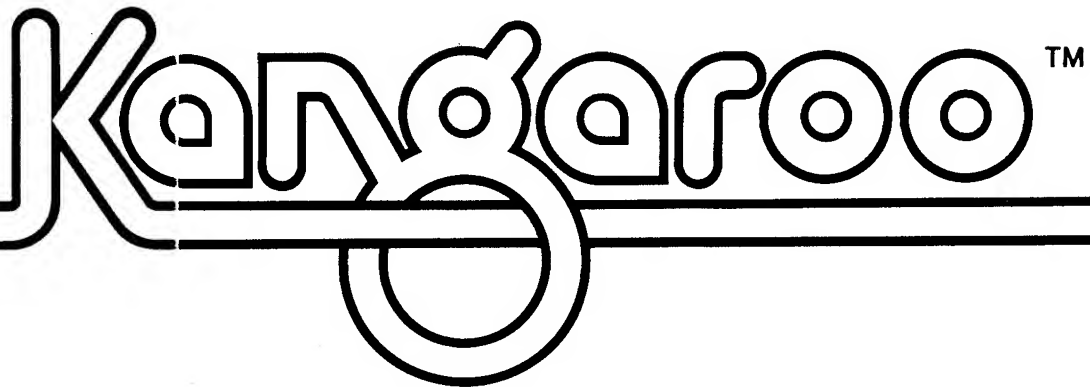


Schematic Package Supplement to



Operation, Maintenance and Service Manual

NOTE

This staple temporarily holds the schematic package together. Remove the staple before using the schematics.



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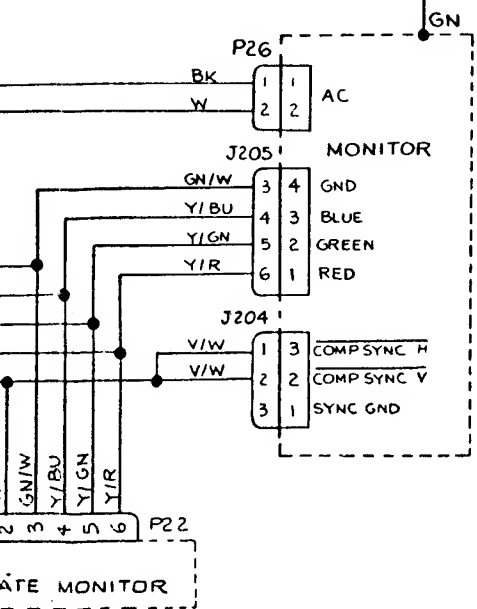
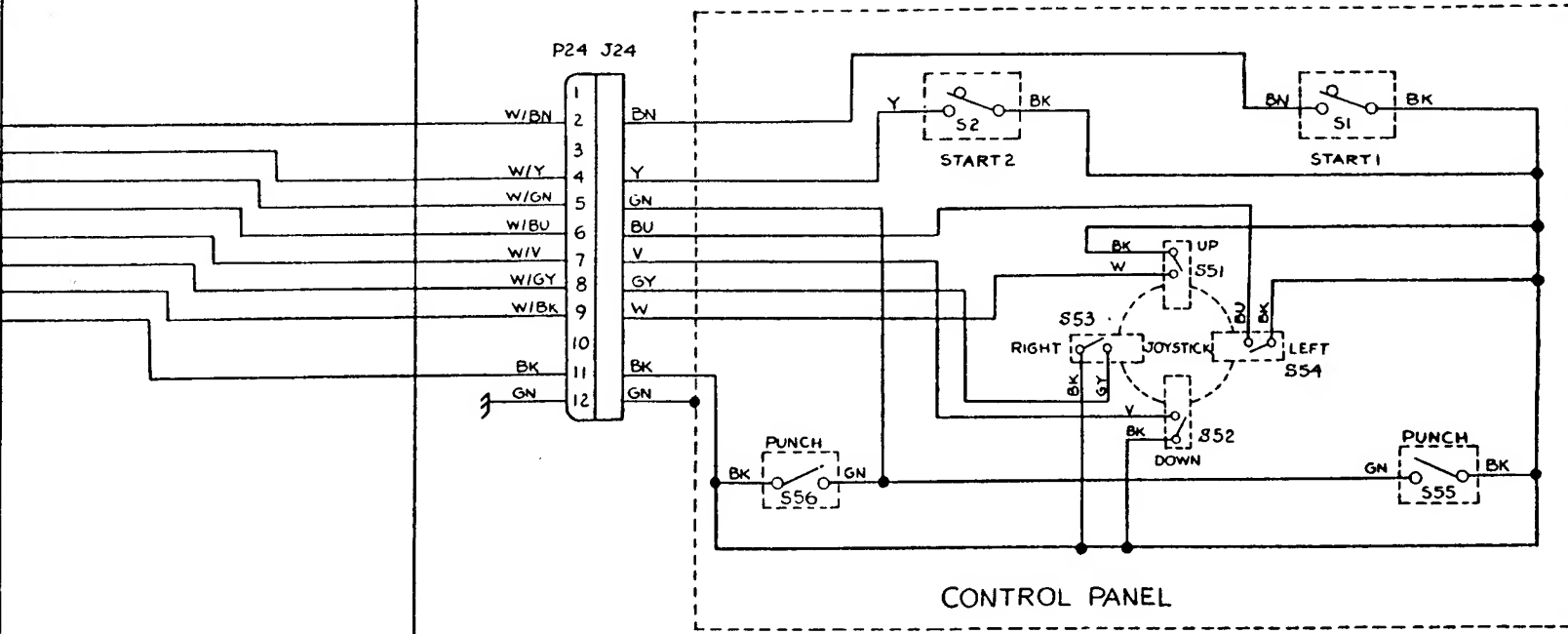
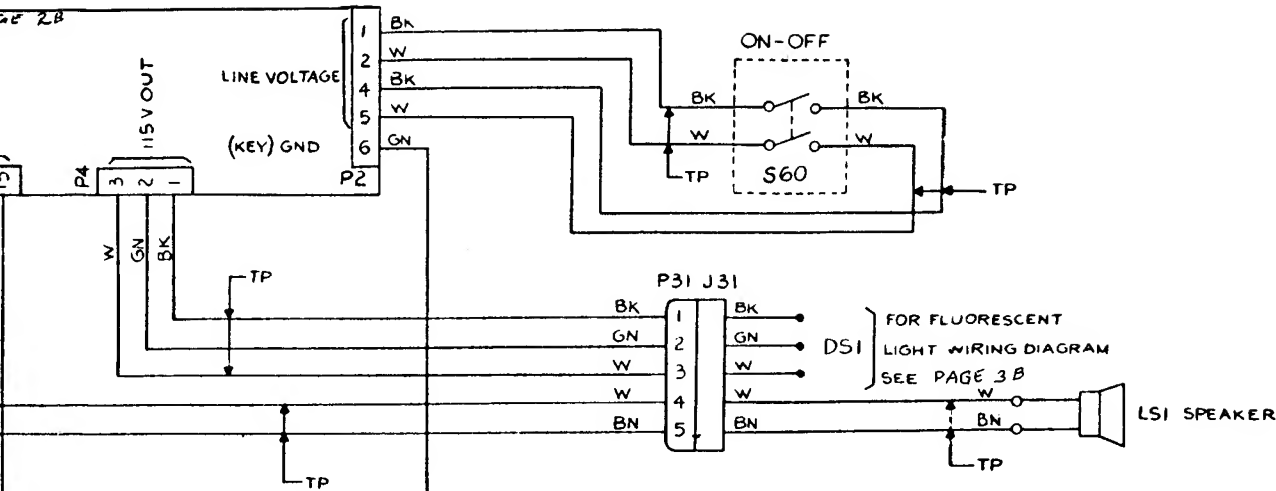
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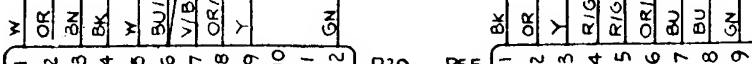
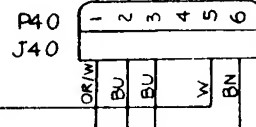
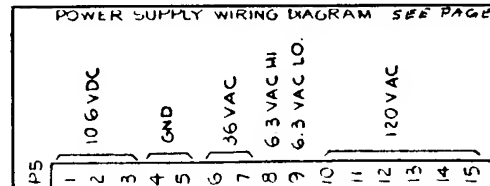
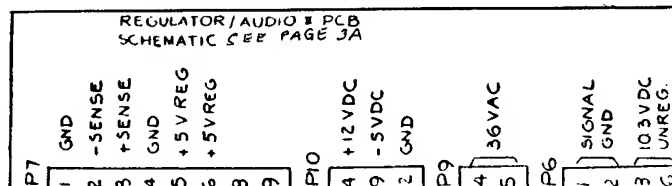
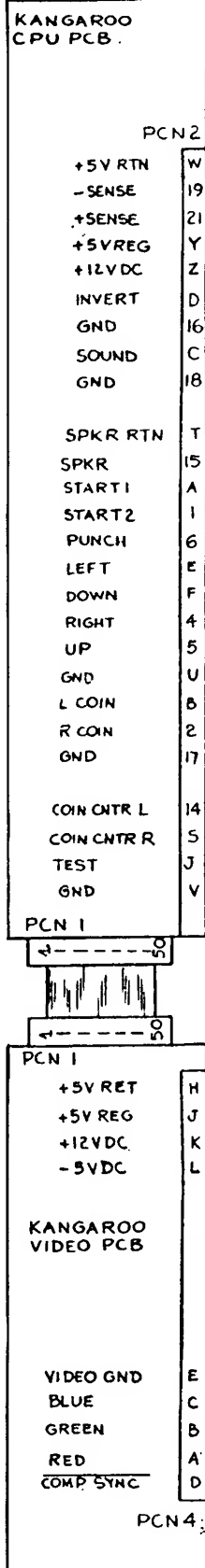
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Kangaroo Upright Game Wiring Diagram

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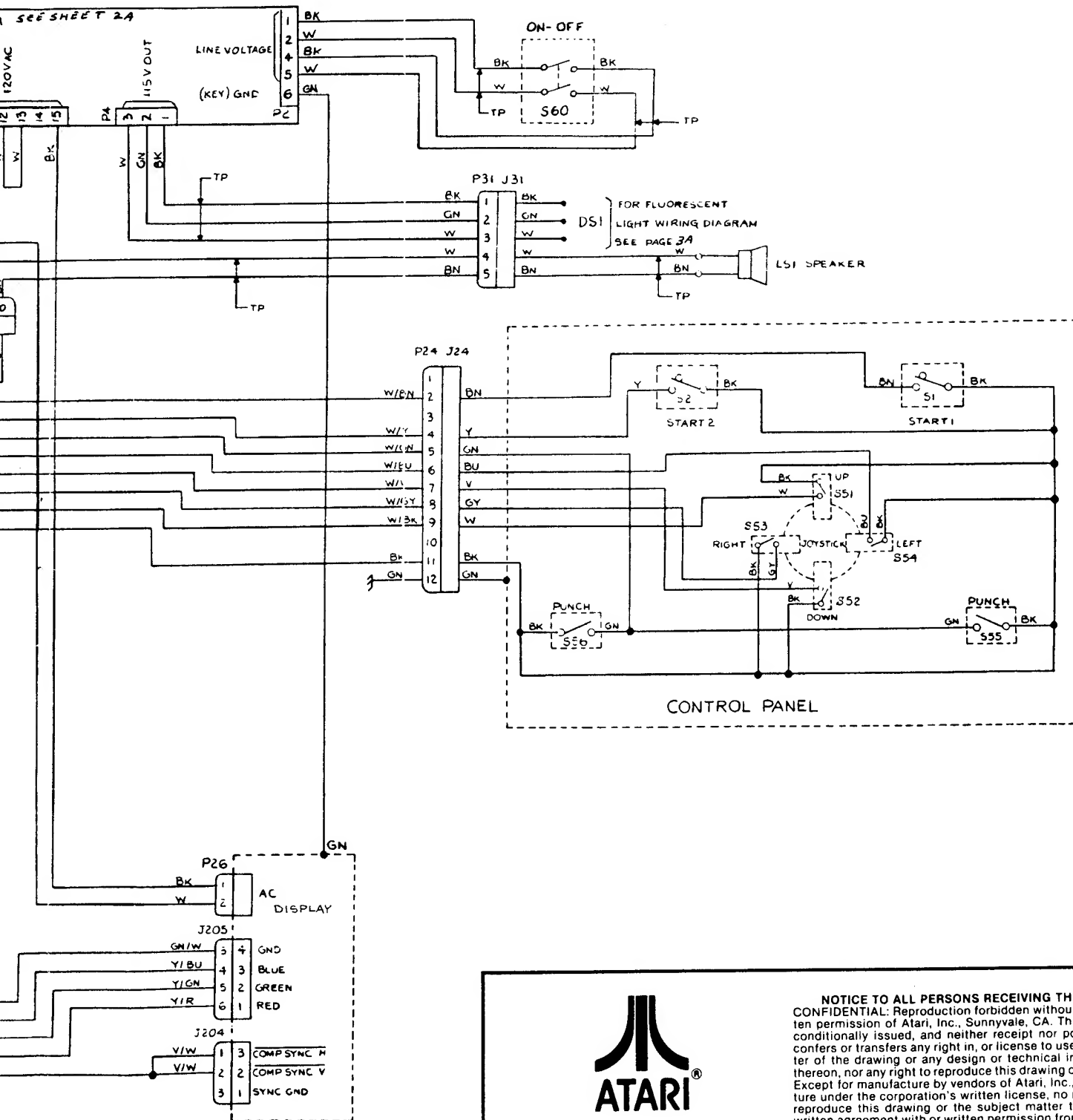
SP-204 Sheet 1B
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FOR COMPONENT WIRING
DIAGRAM SEE PAGE 3B

FOR COIN DOOR WIRING
DIAGRAM SEE PAGE 3B

ALTERNATE



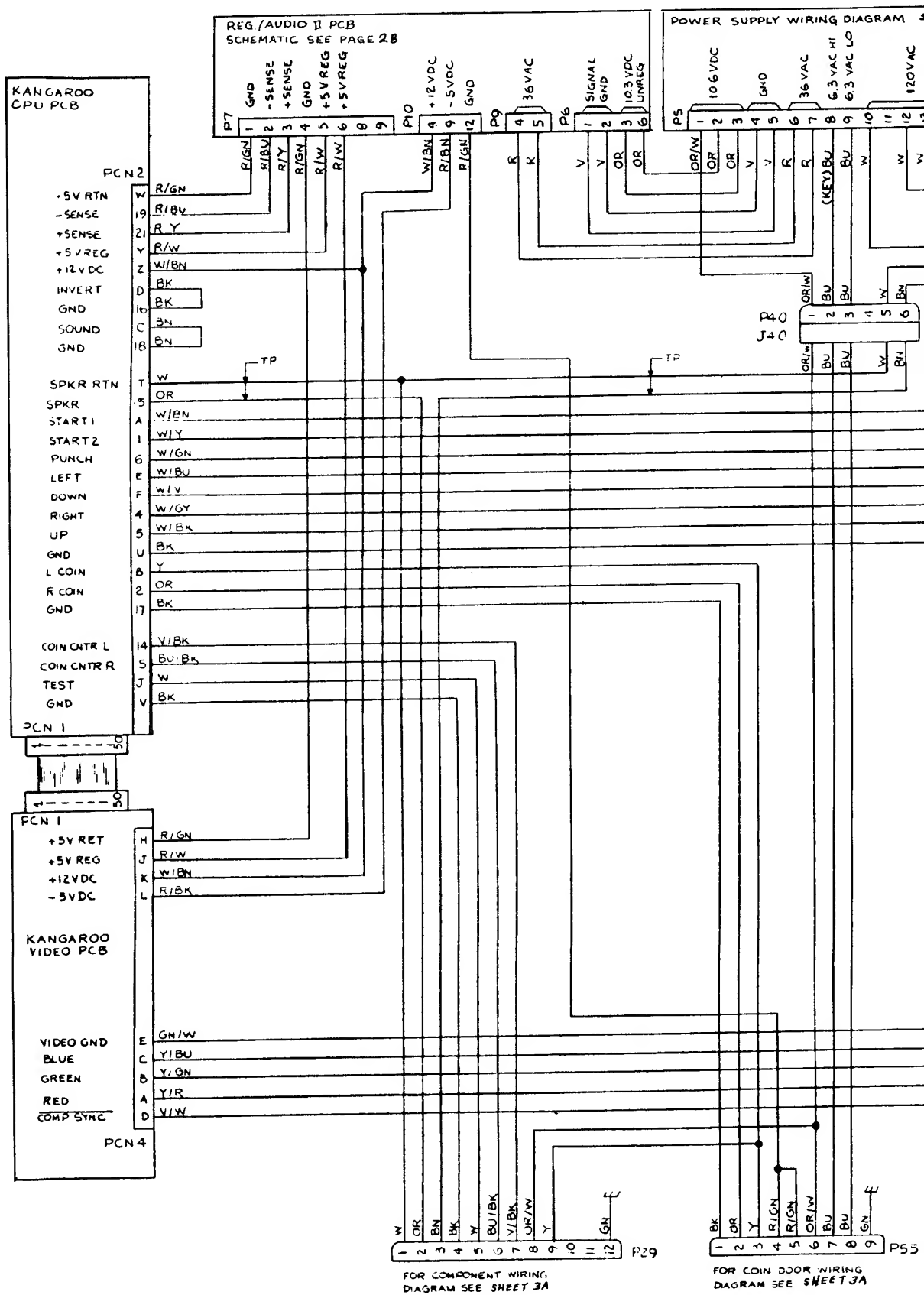
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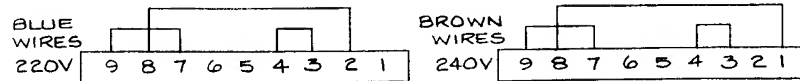
Ireland-Built Kangaroo Game Wiring Diagram

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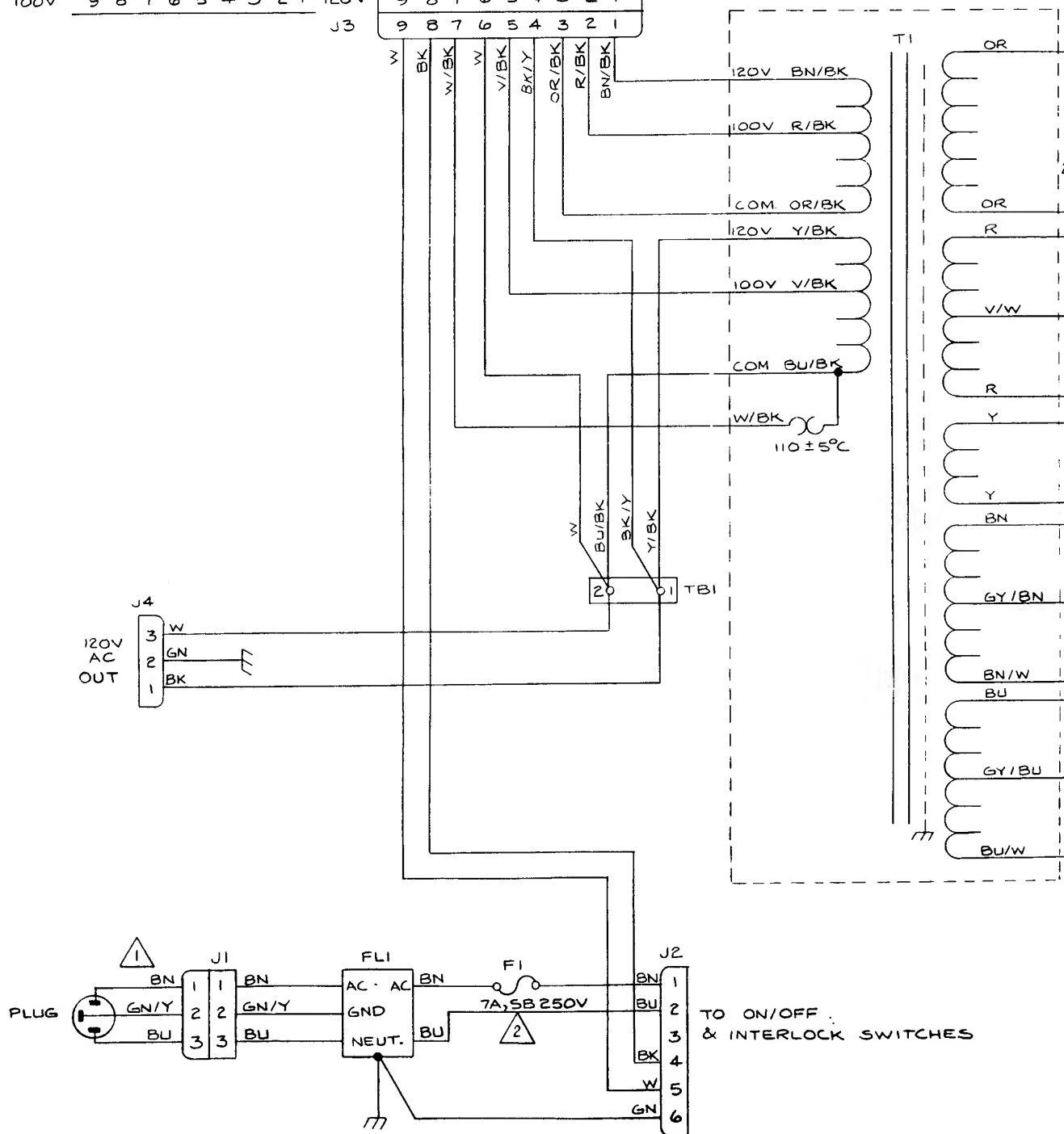
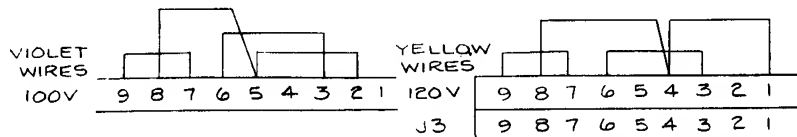
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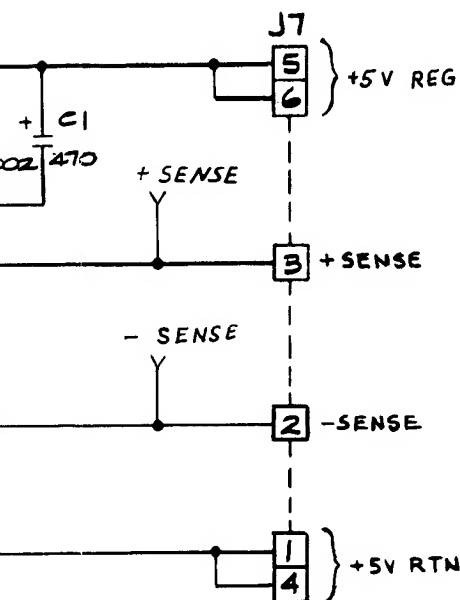
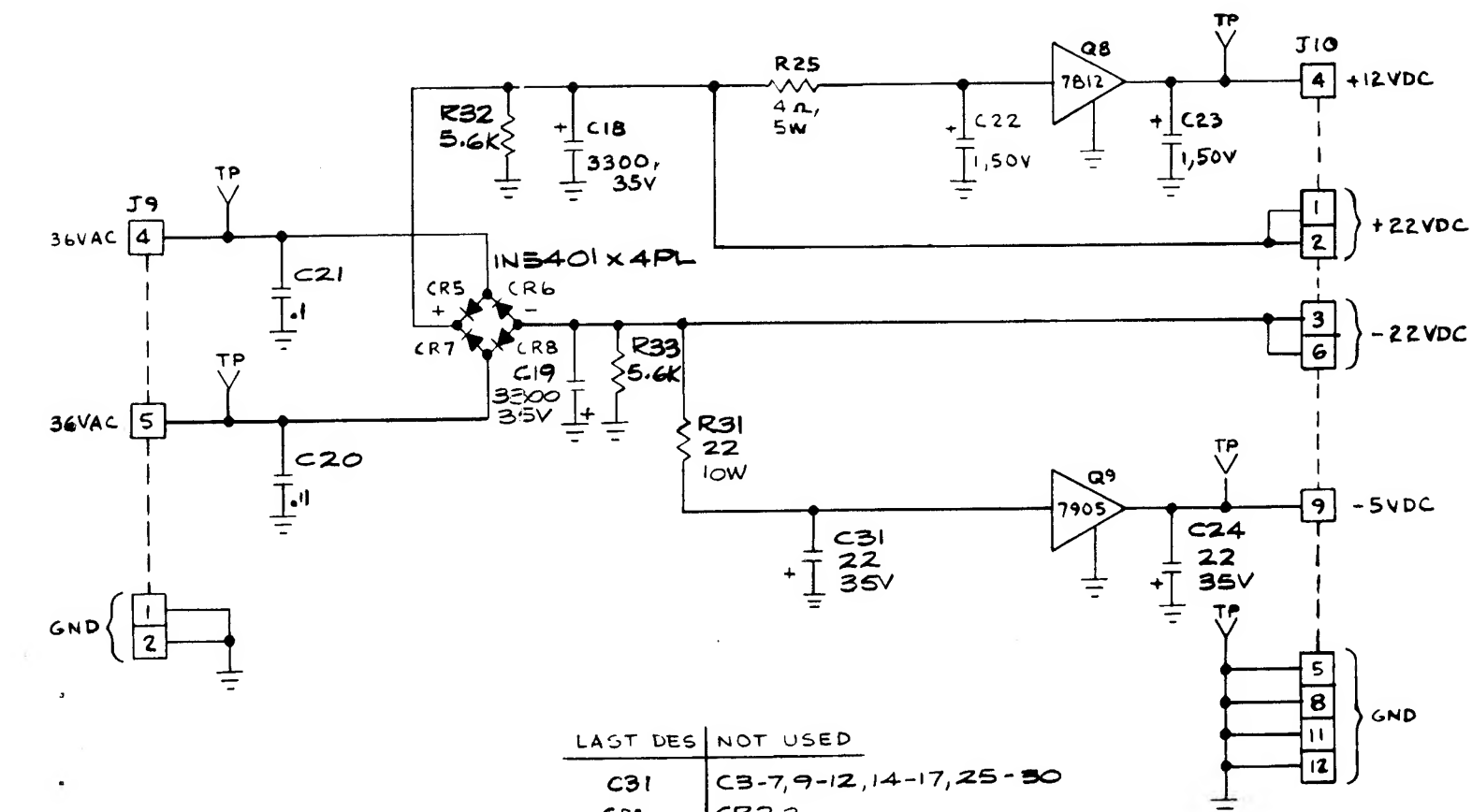
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VOLTAGE SELECTION BLOCKS





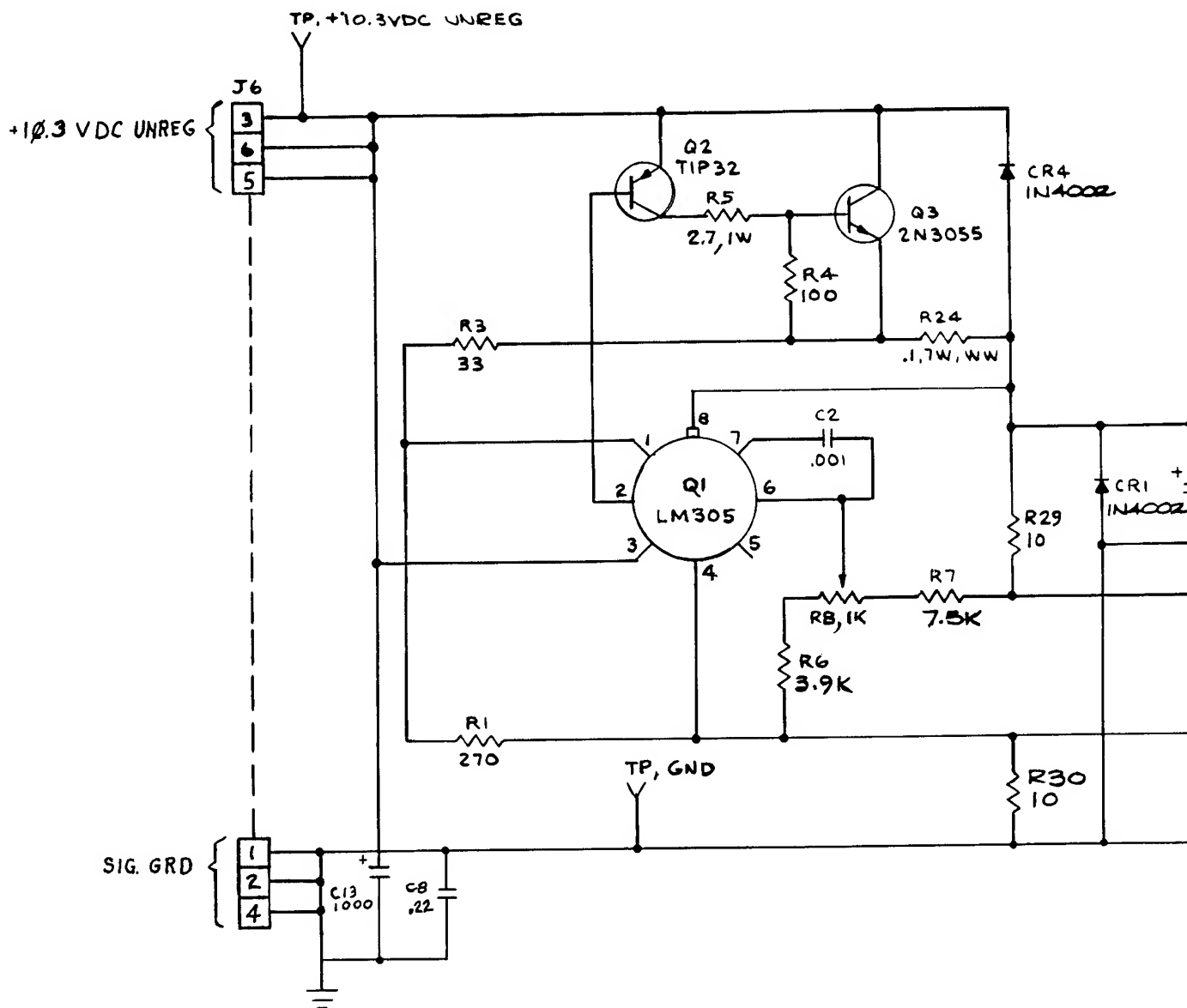
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Kangaroo Reg./Audio II PCB Schematic Diagram

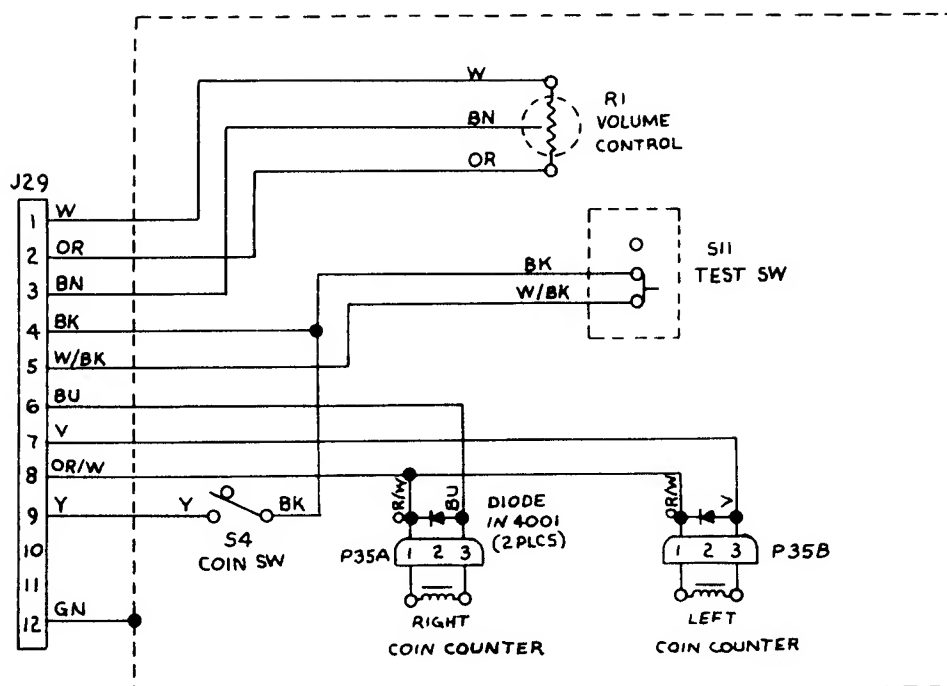
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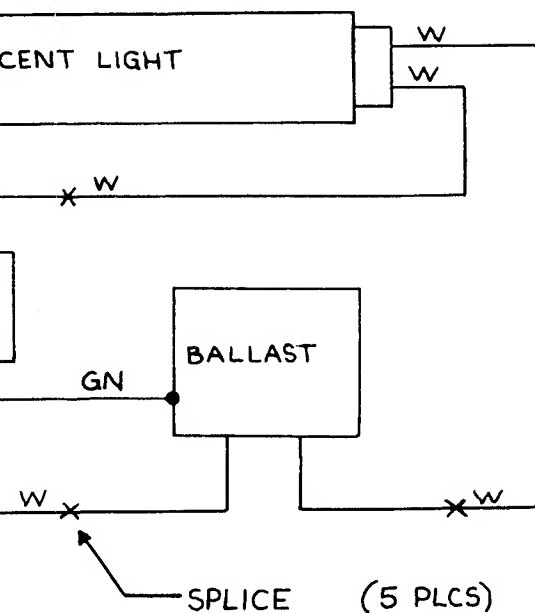
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Utility Panel Wiring Diagram



Speaker Wiring Diagram



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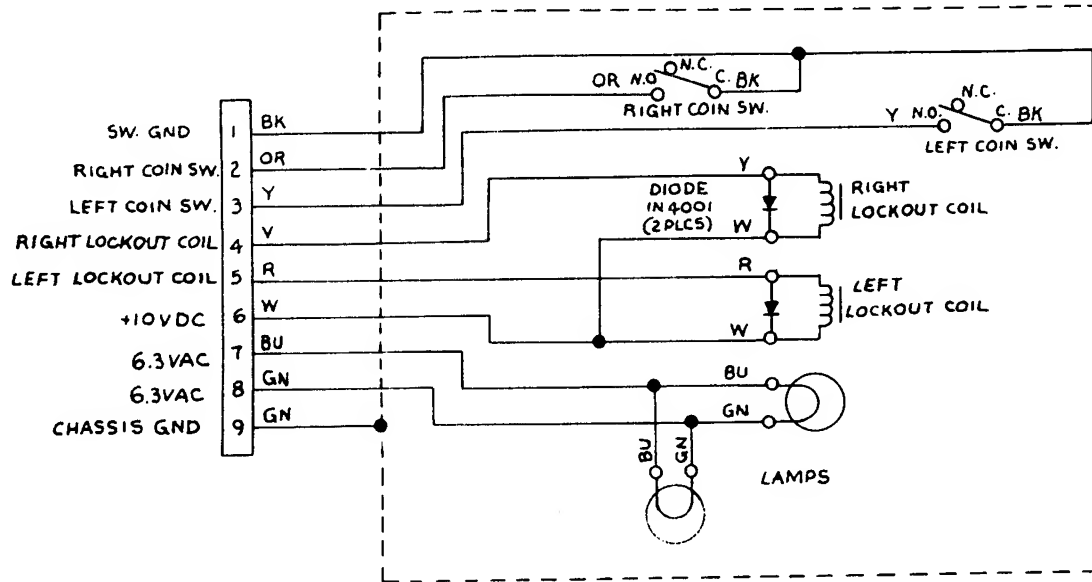
Kangaroo Game Wiring Interfaces

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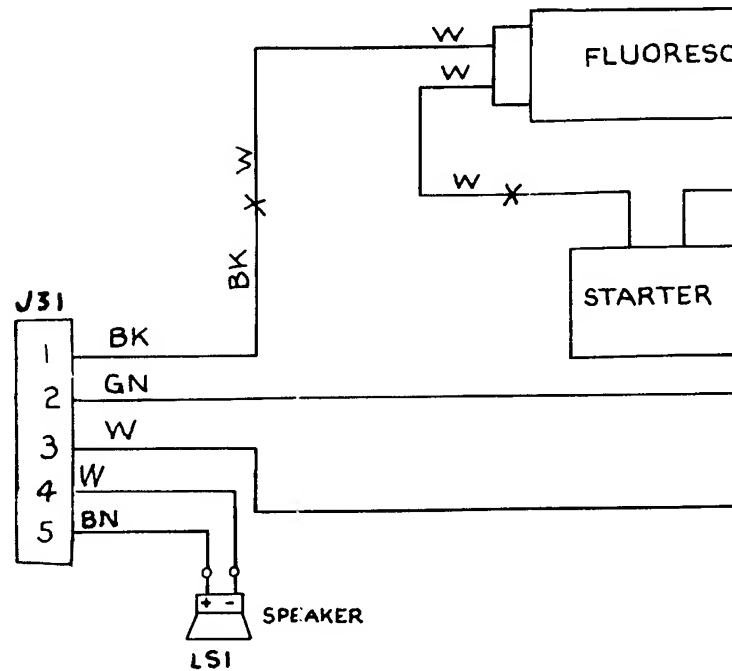
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Coin Door Wiring Diagram

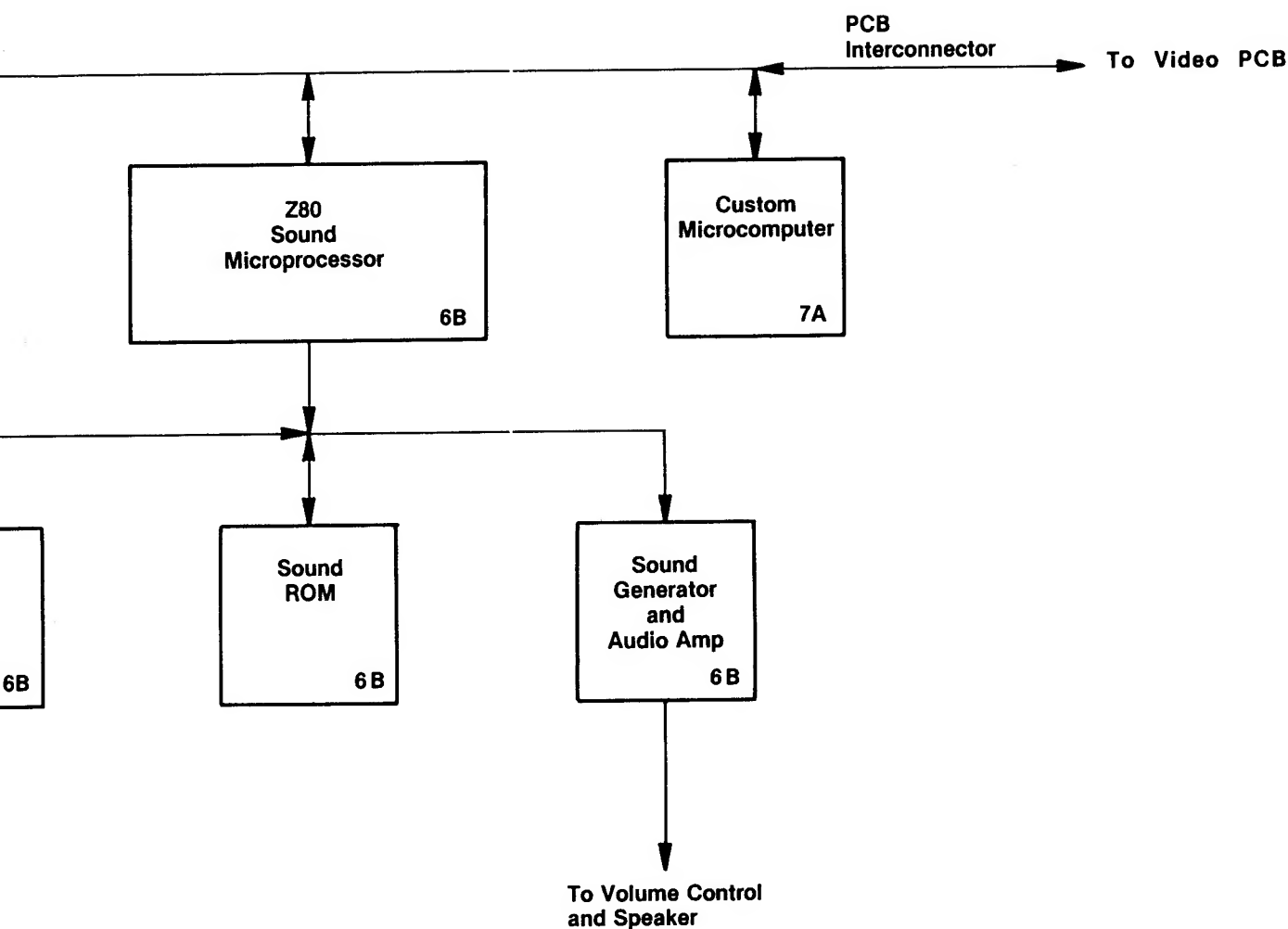


Fluorescent Light and



NOTE

The **service switch**, located on the CPU PCB, allows you to enter credits without tripping the coin counter.



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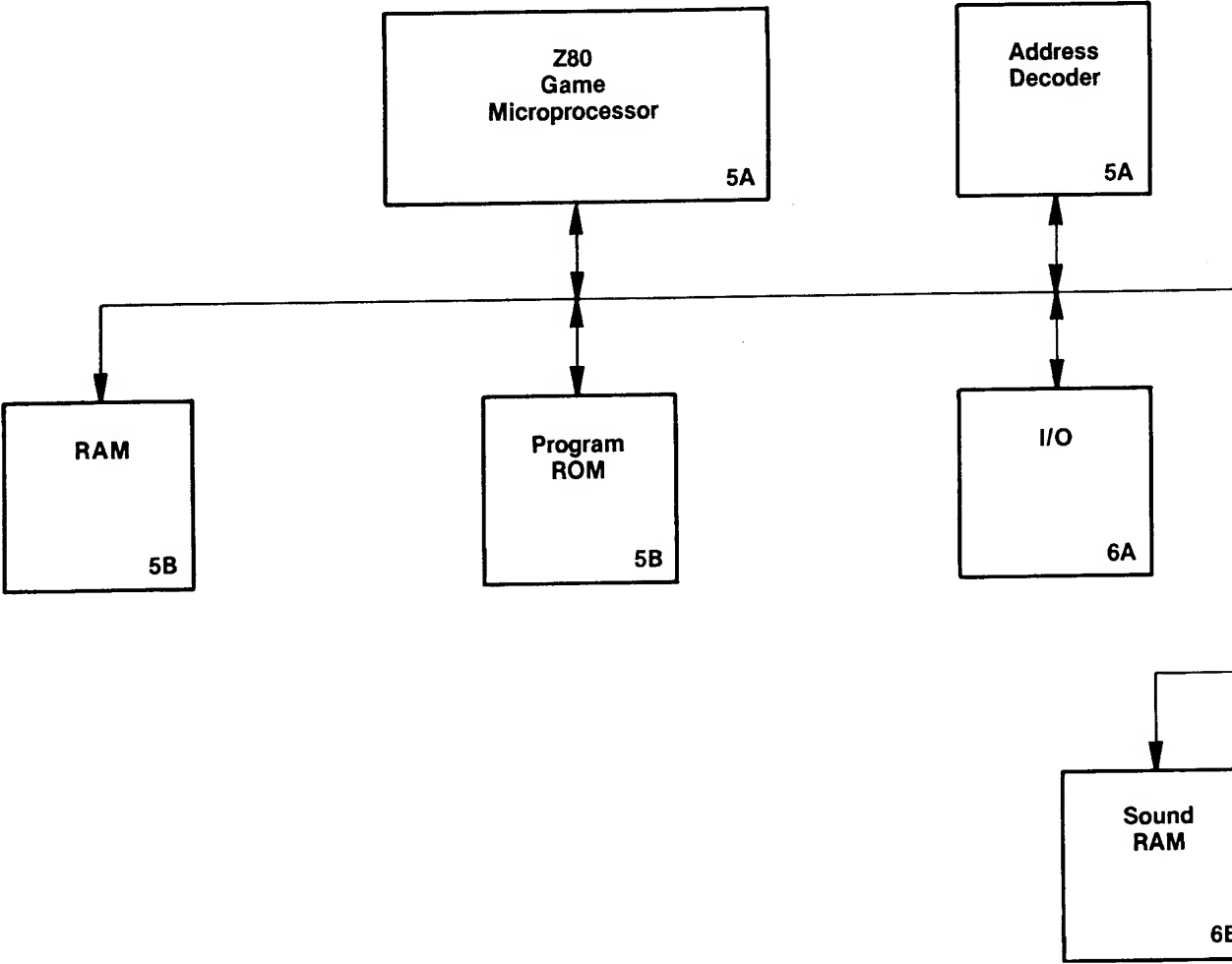
Kangaroo CPU PCB Schematic Diagram

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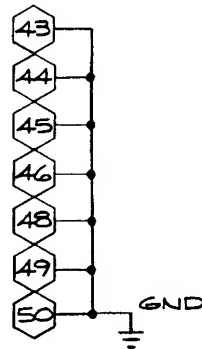
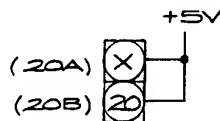
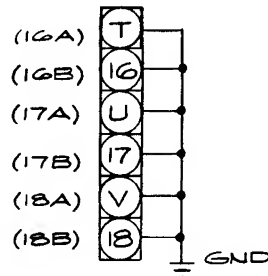
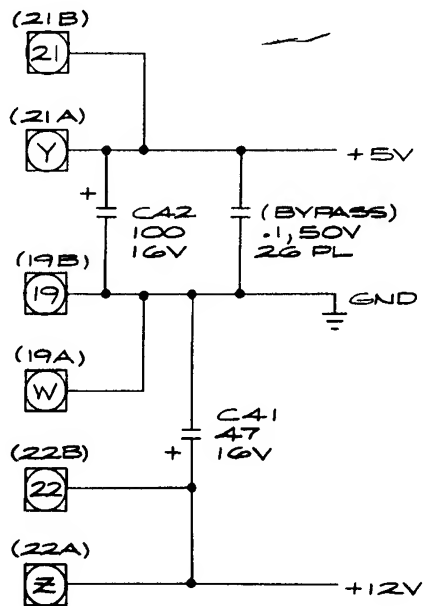
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Block Diagram (CPU PCB)



CPU Power Input



NOTES:

1.  = CONNECTOR CN2
2.  = CONNECTOR CN1



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Kangaroo CPU PCB Schematic Diagram

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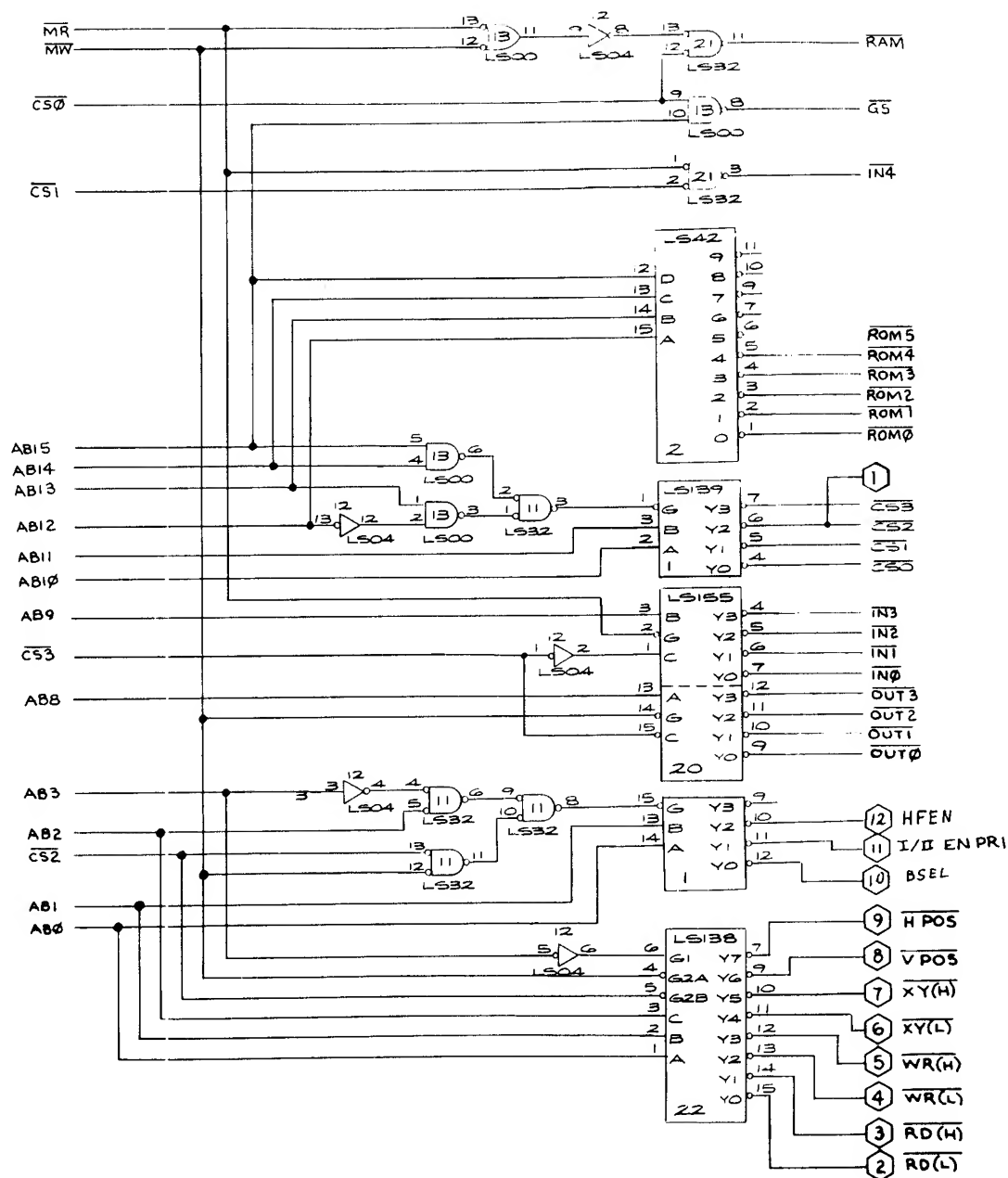
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Memory Map

[illegible]

Address Decoder



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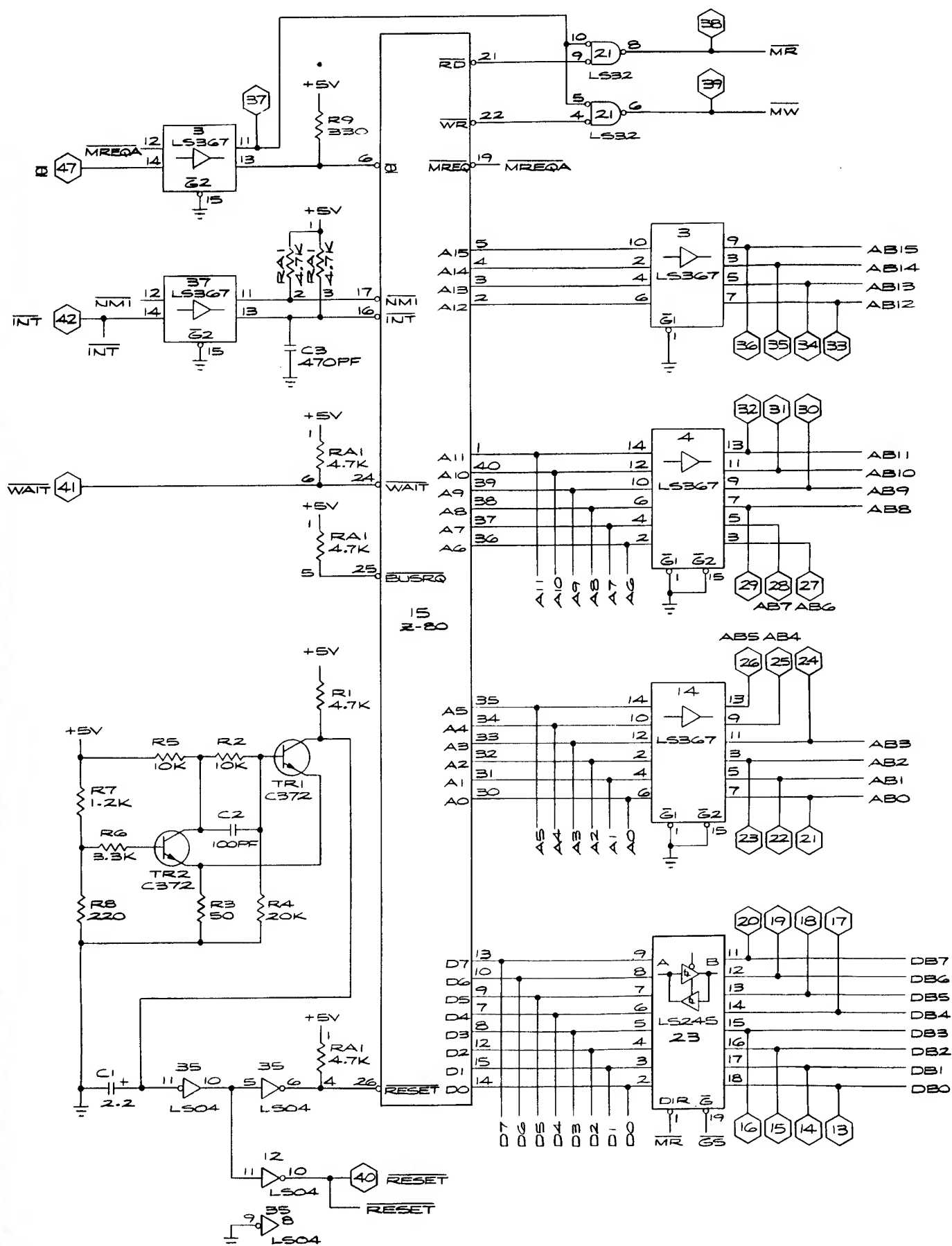
Kangaroo CPU PCB Schematic Diagram

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Game Microprocessor





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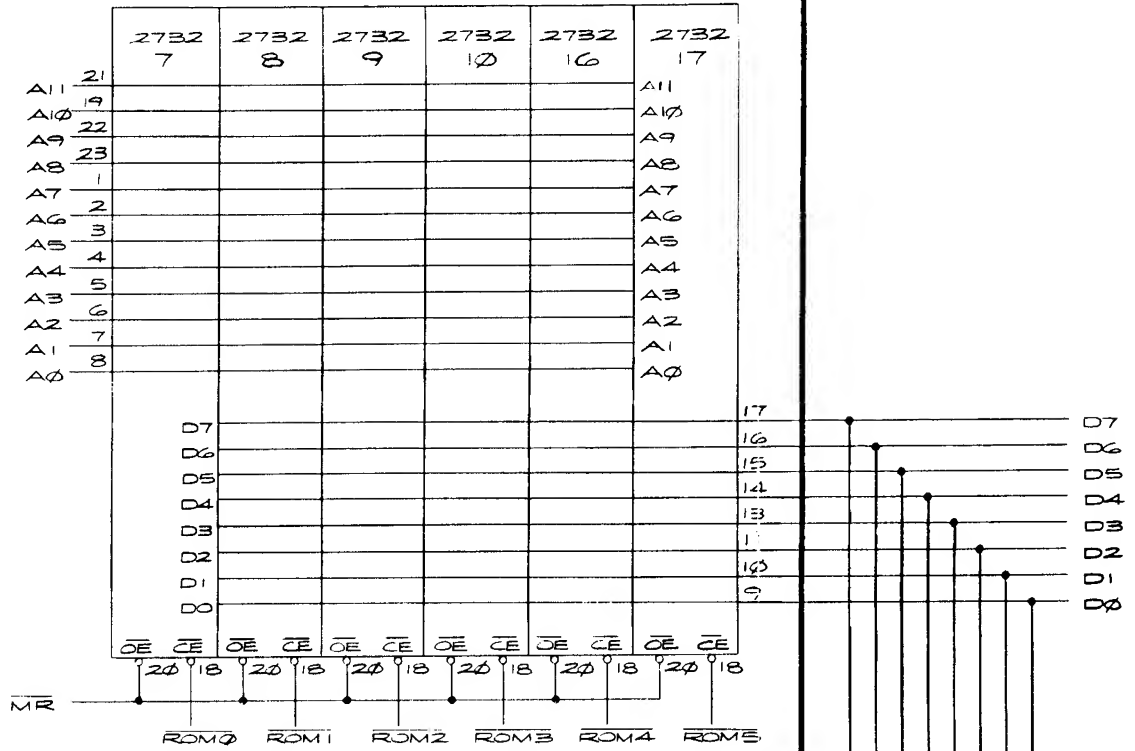
Kangaroo CPU PCB Schematic Diagram

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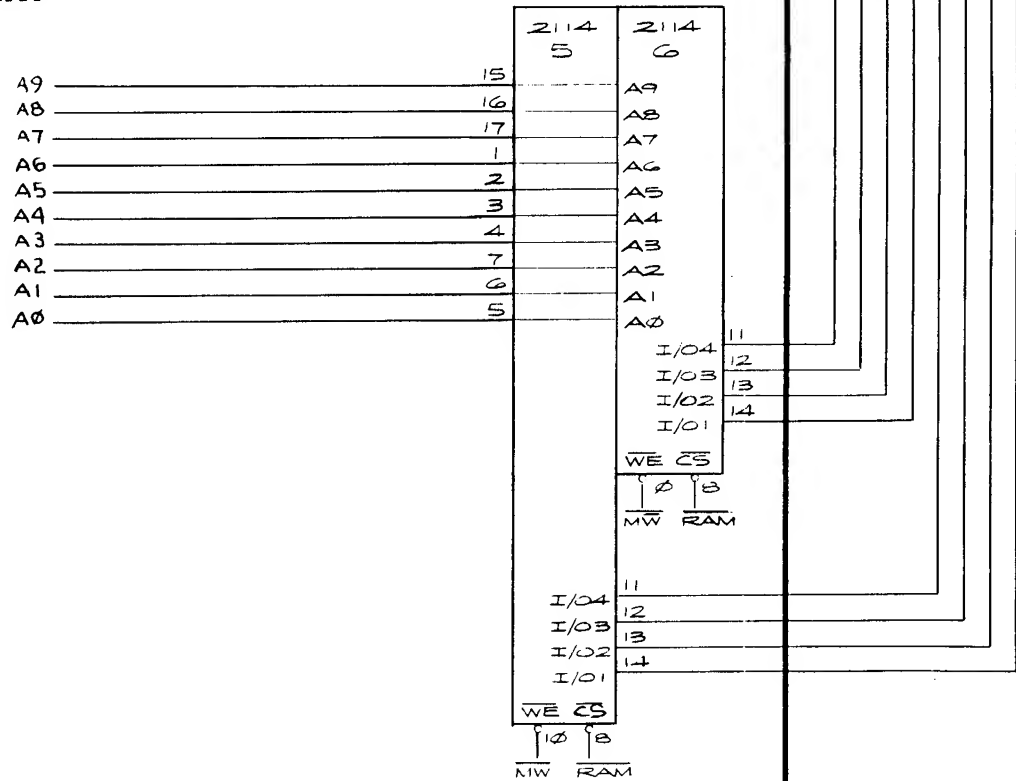
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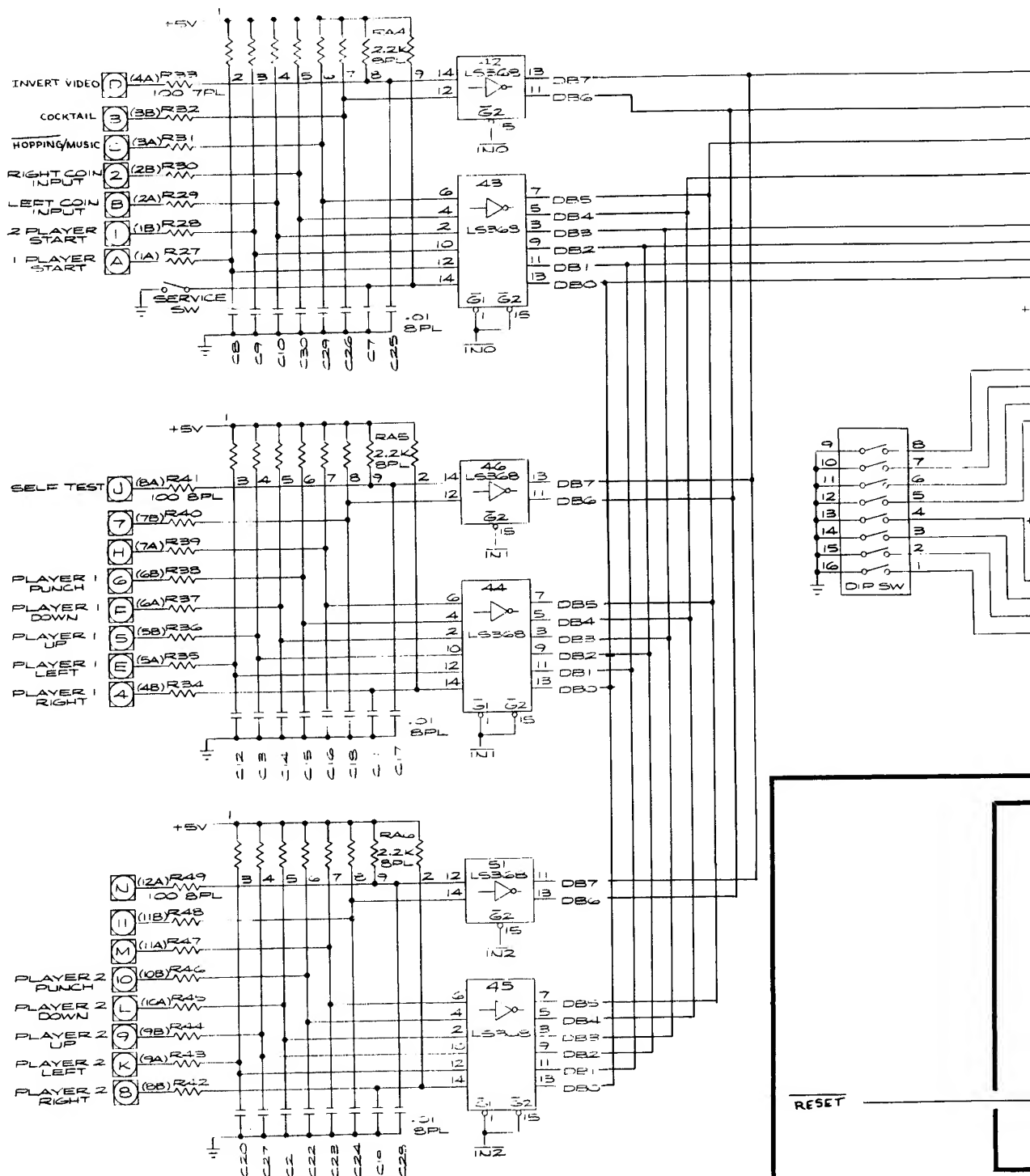
Program ROM

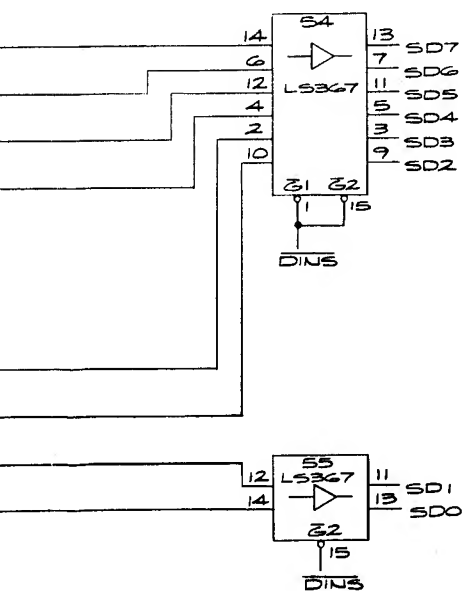
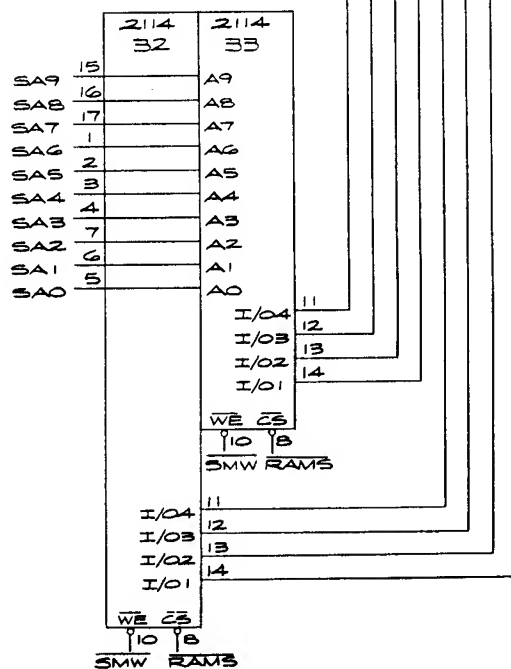
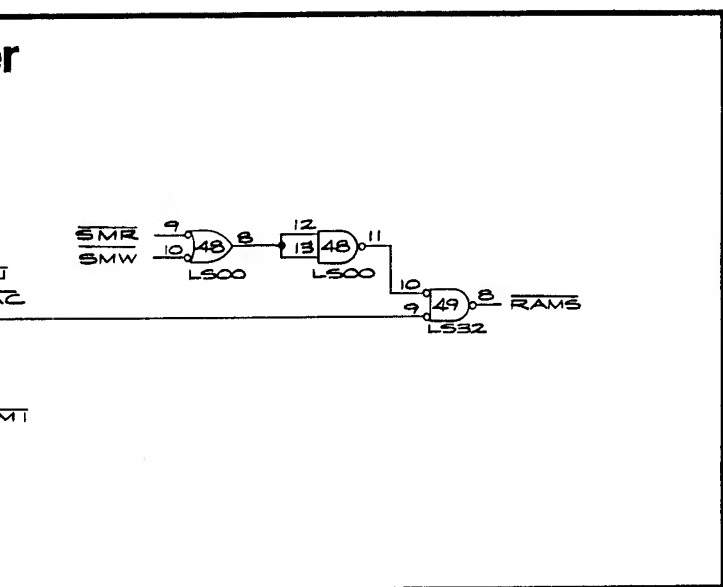
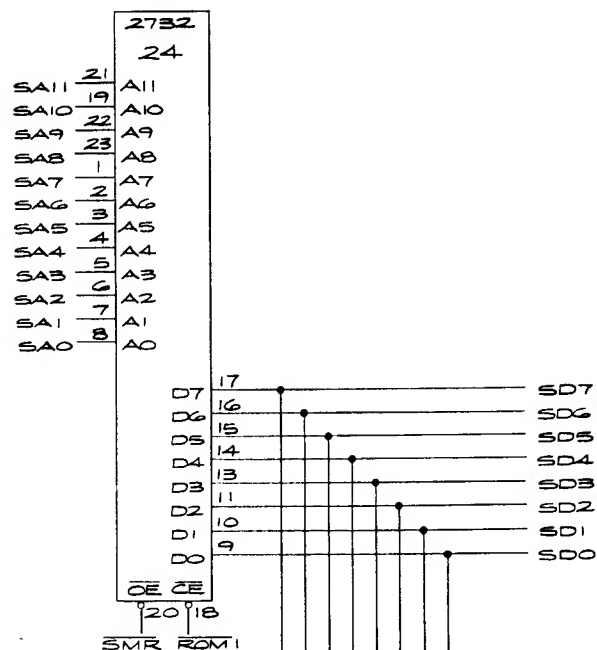
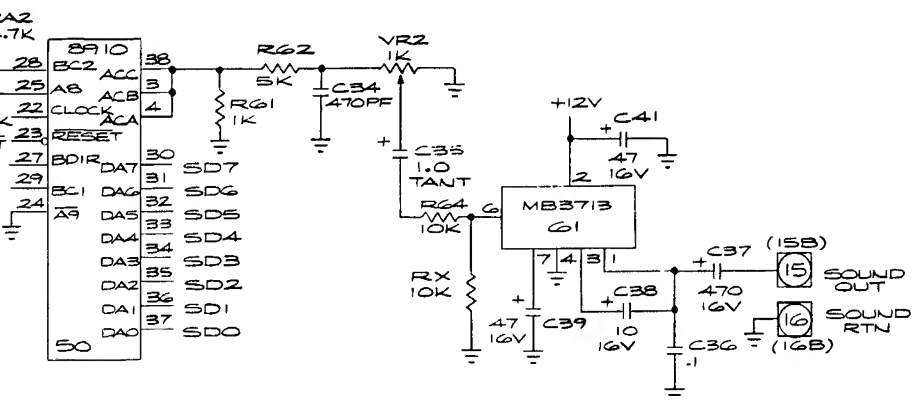


RAM



Inputs





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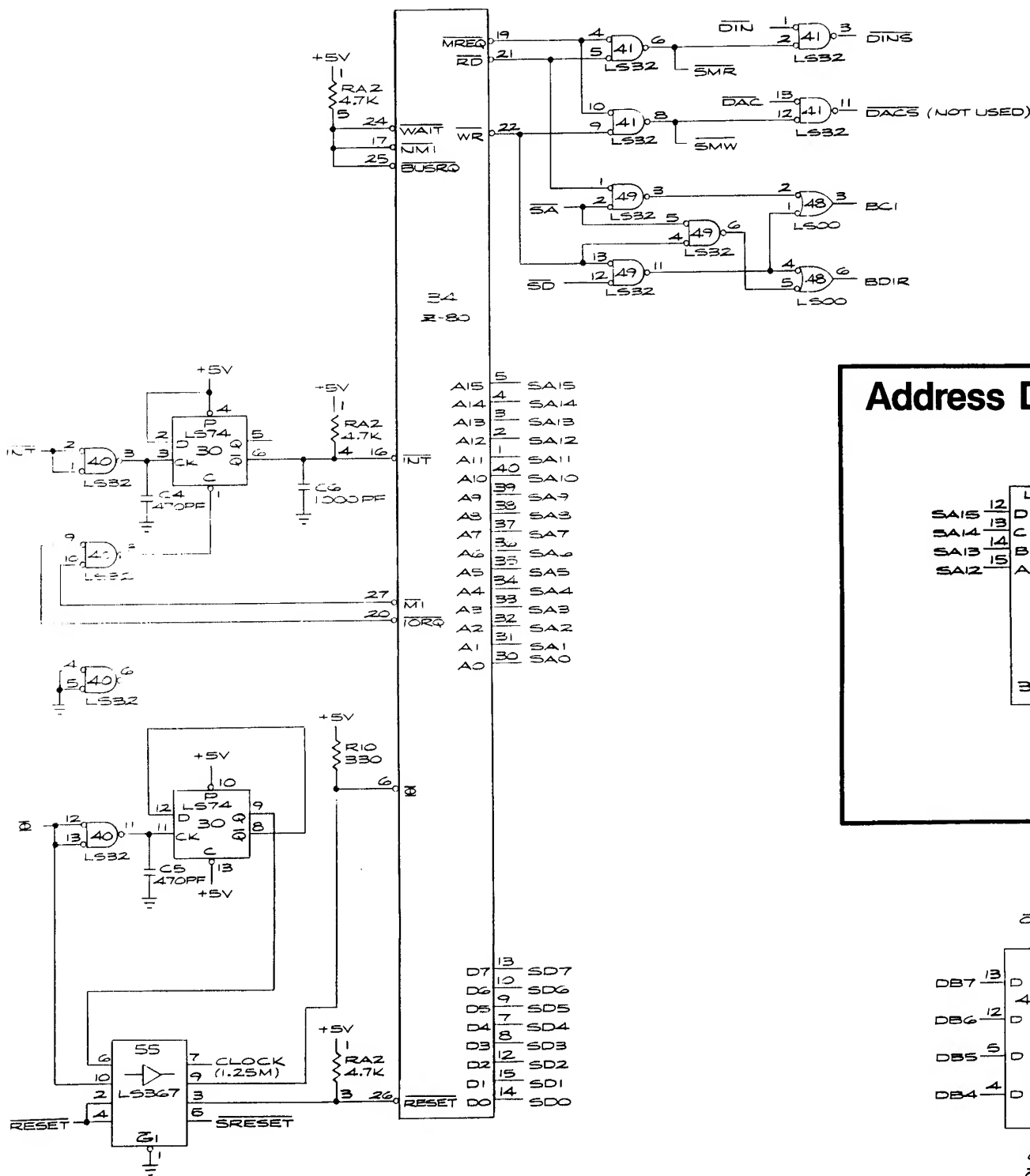
Kangaroo CPU PCB Schematic Diagram

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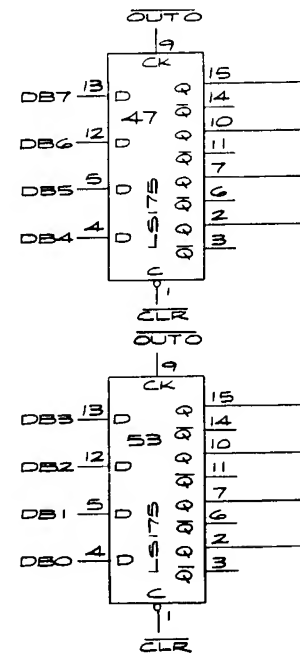
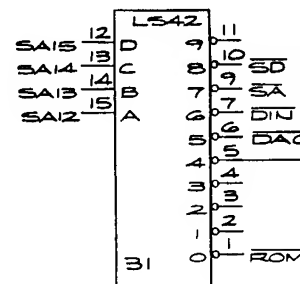
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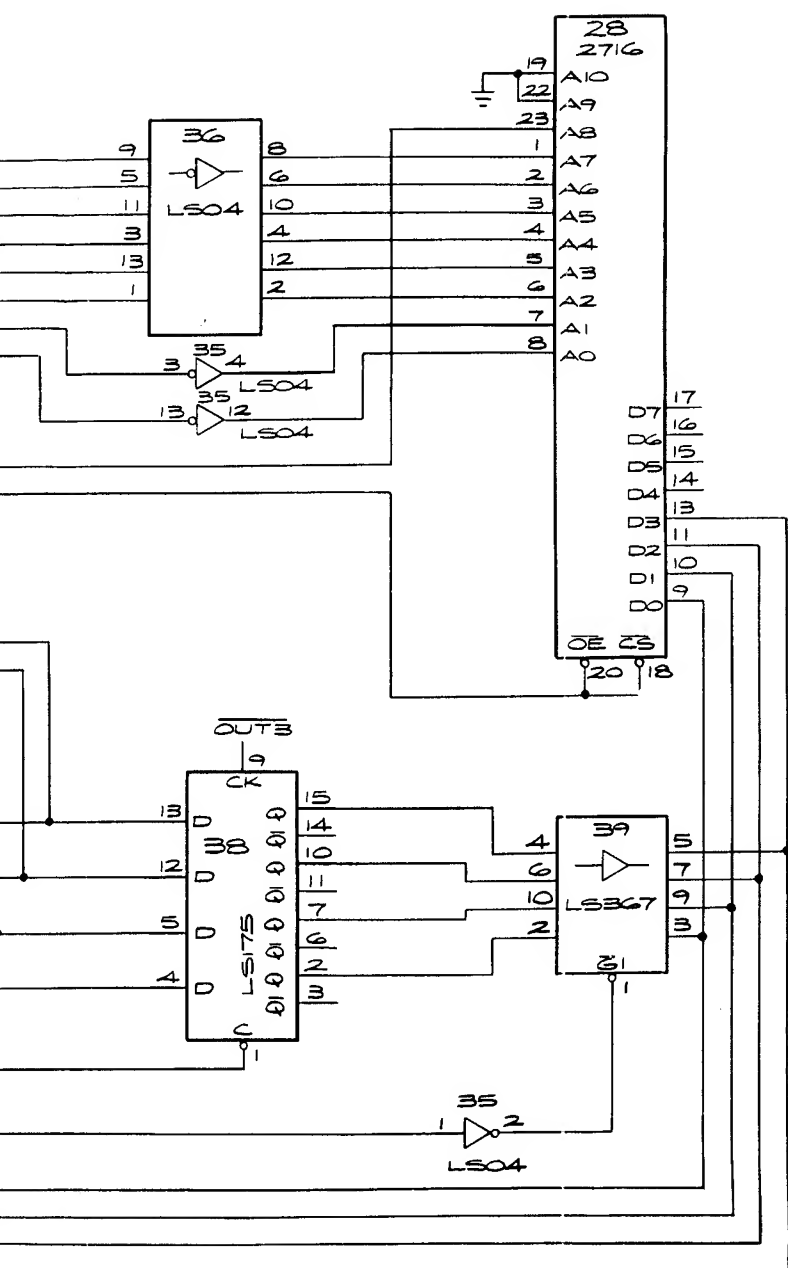
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Sound Microprocessor



Address Decoder





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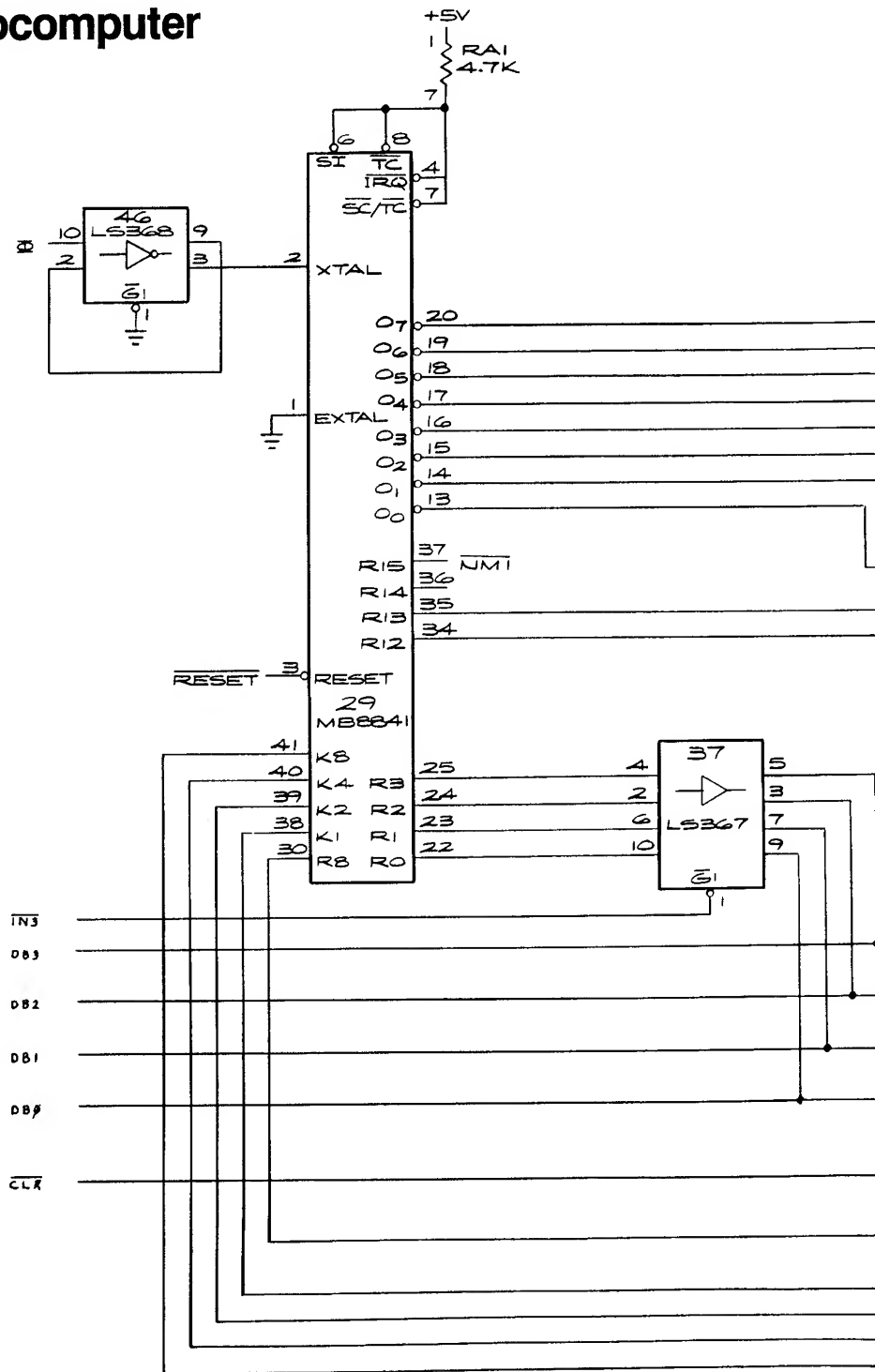
Kangaroo CPU PCB Schematic Diagram

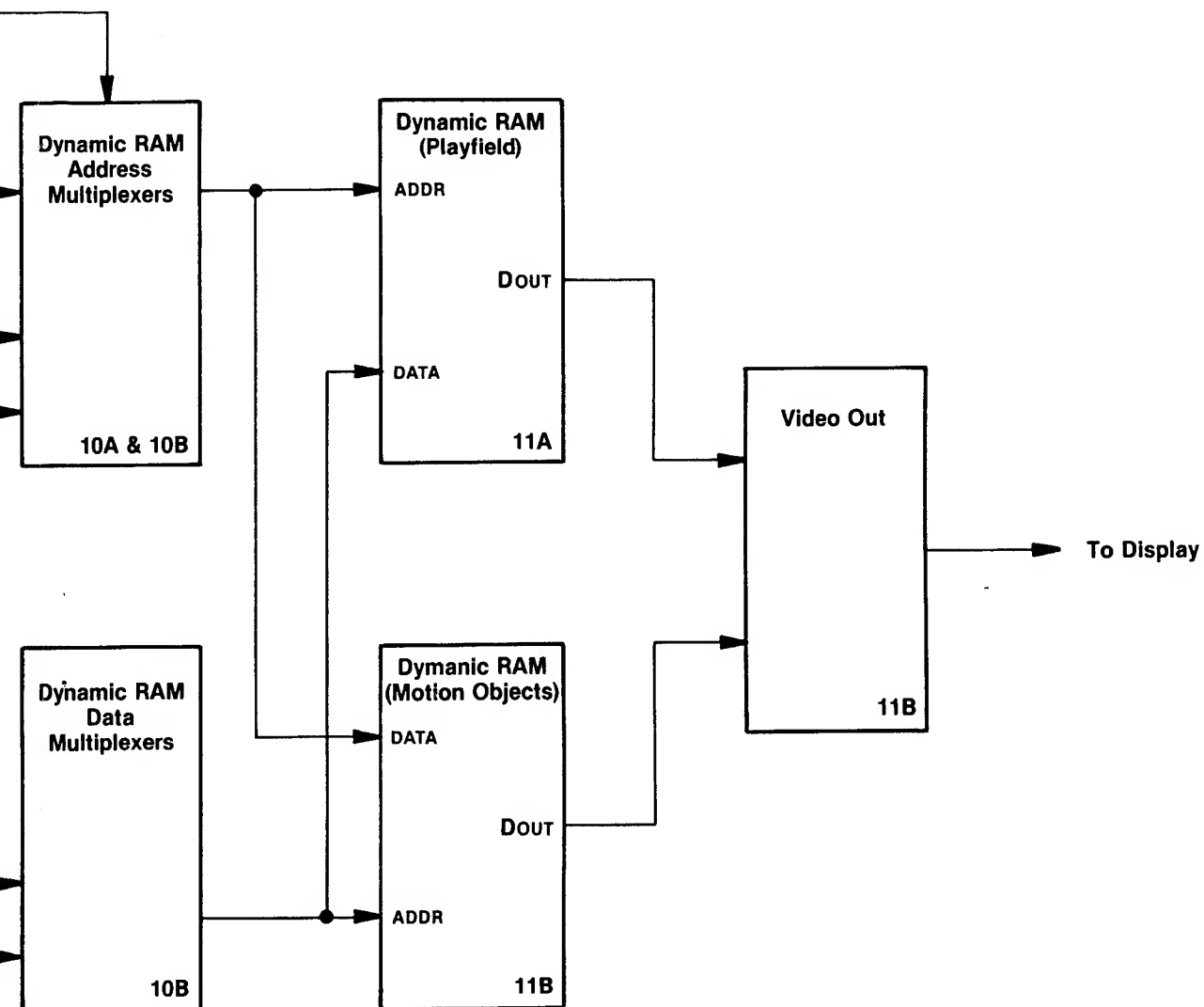
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Custom Microcomputer





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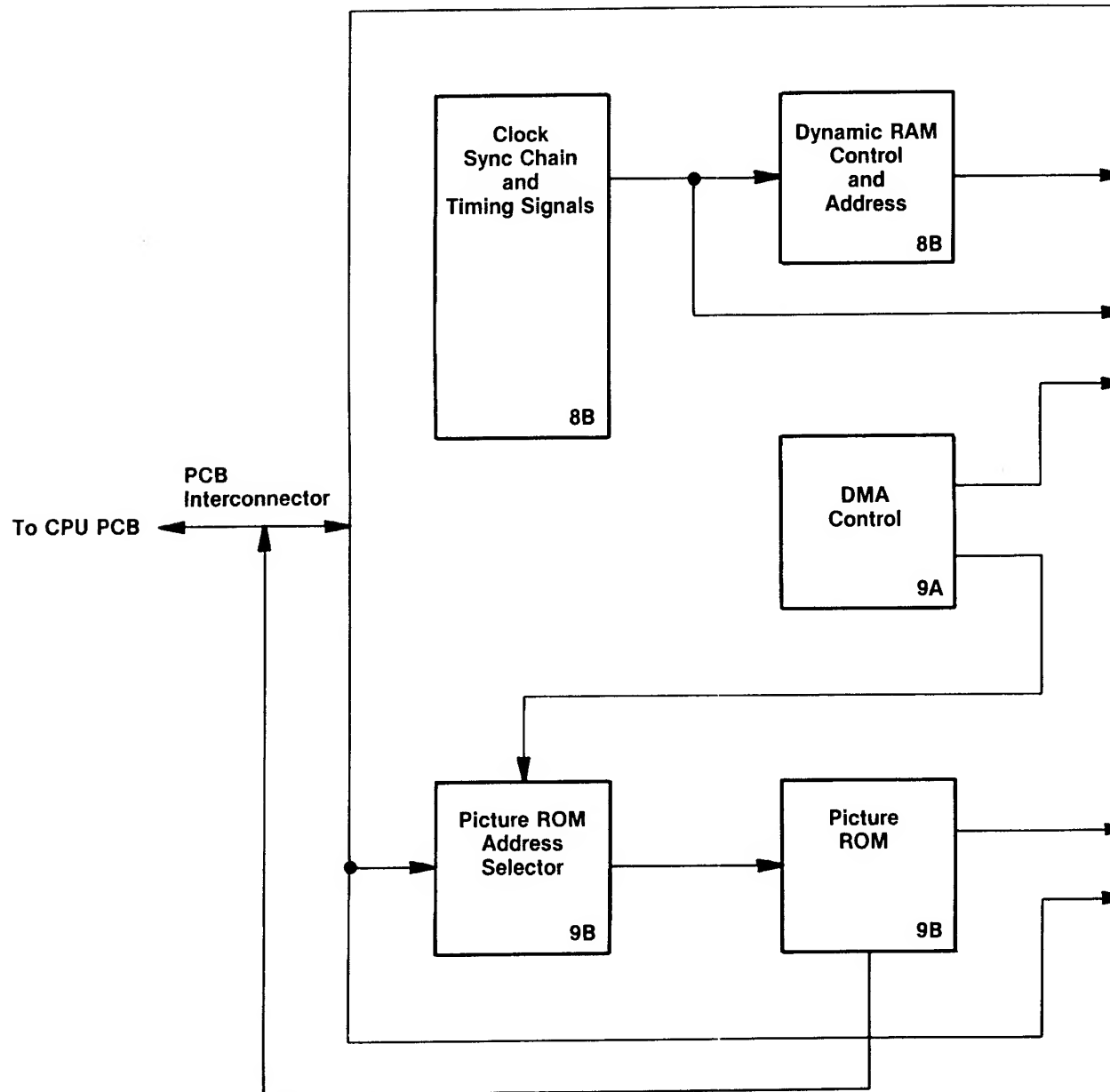
Kangaroo Video PCB Schematic Diagram

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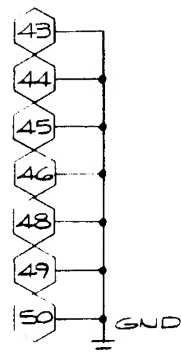
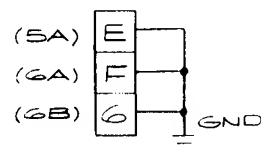
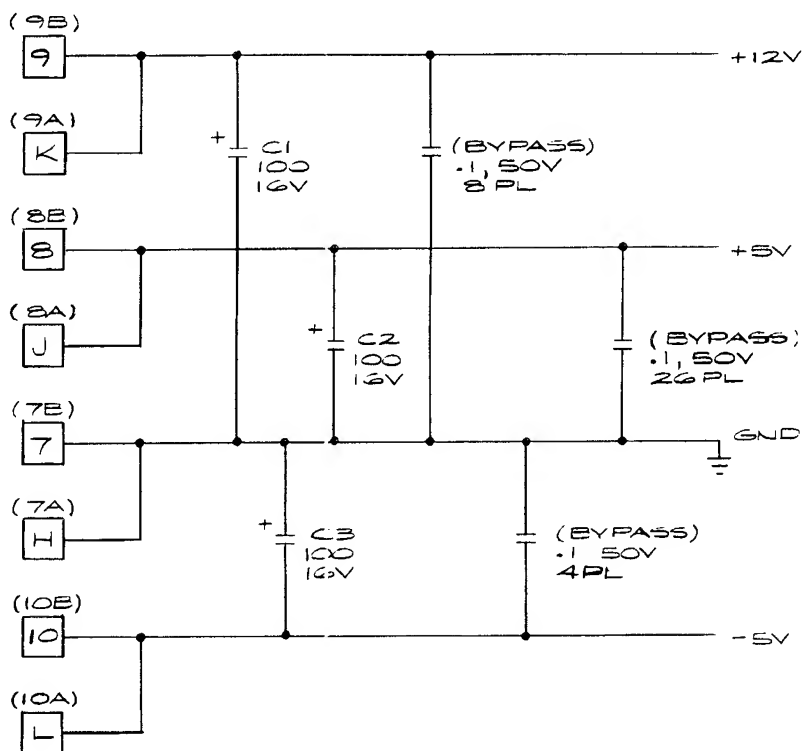
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Block Diagram (Video PCB)



Video Power Input



NOTES:

1. = CONNECTOR CN1
2. = CONNECTOR CN4



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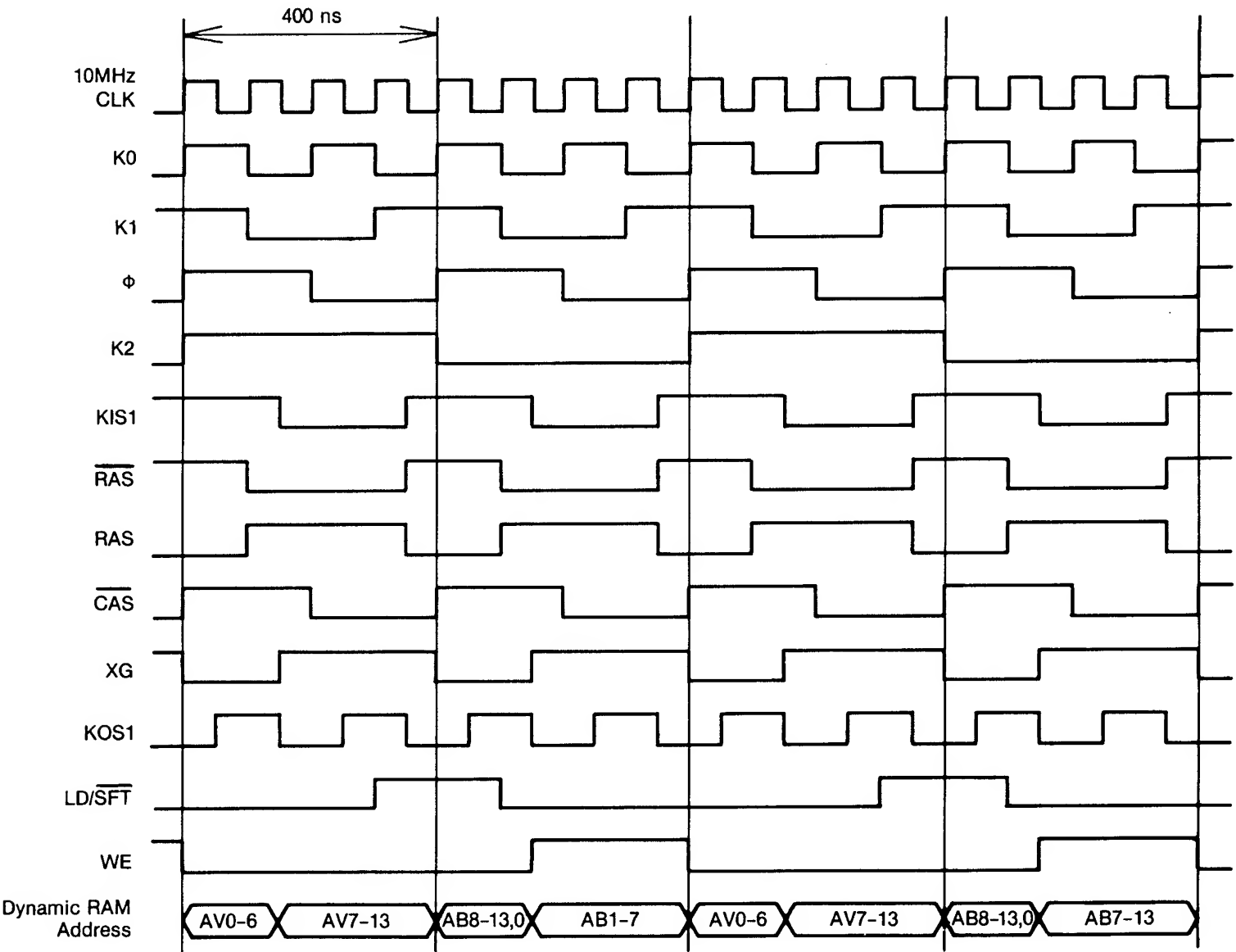
Kangaroo Video PCB Schematic Diagram

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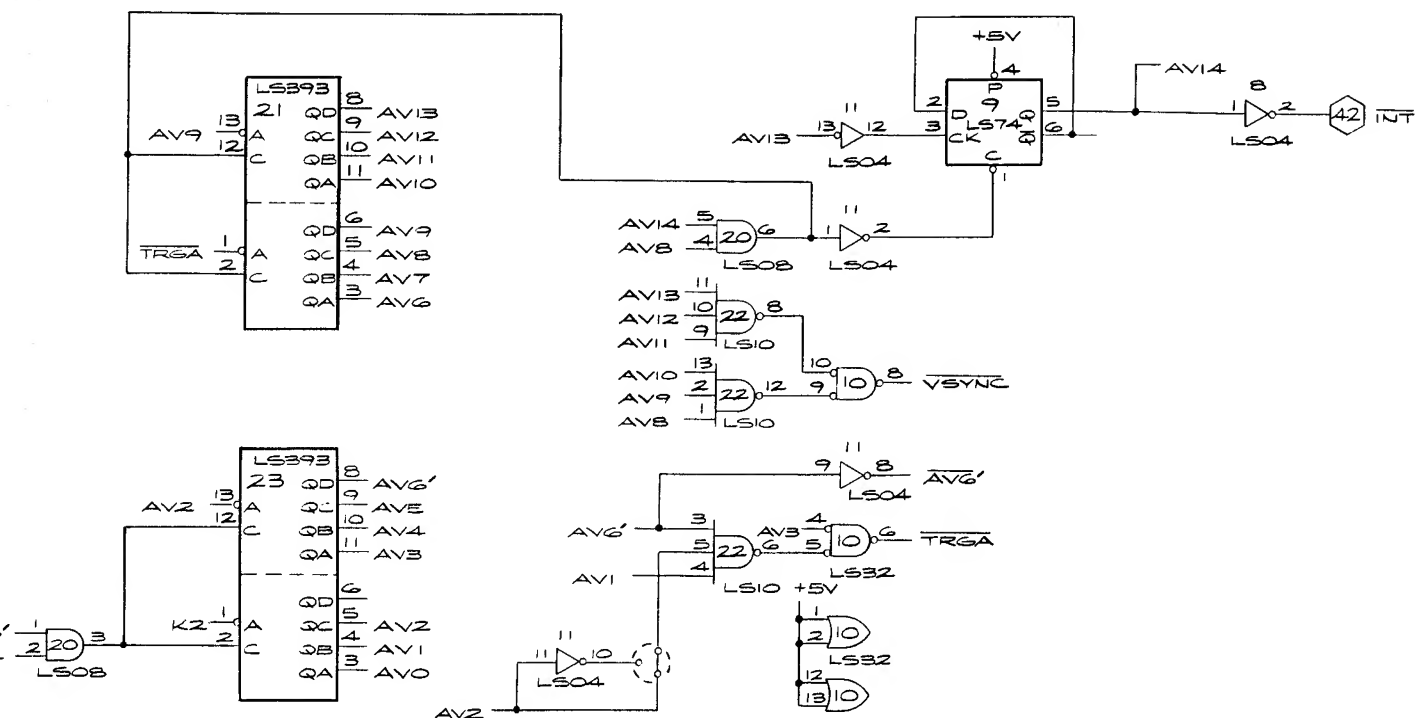
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SP-204 Sheet 8A
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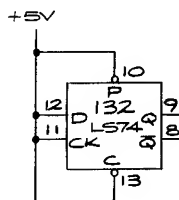
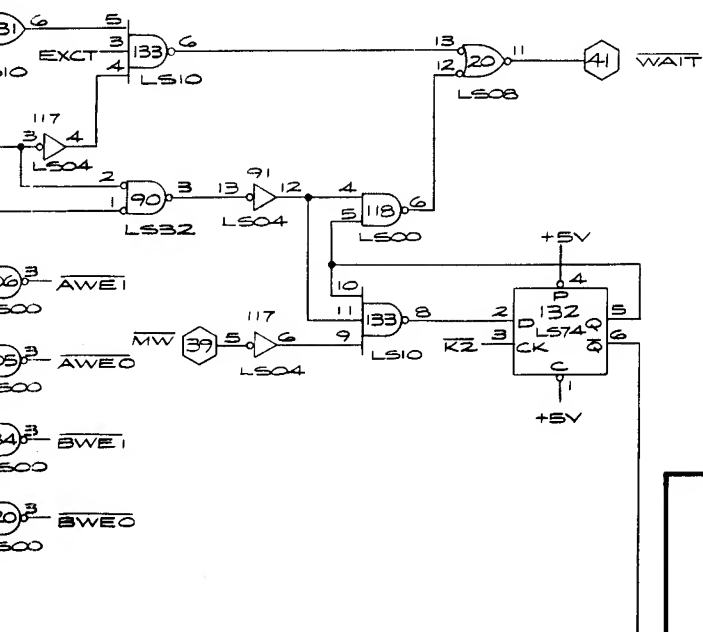
Dynamic RAM Timing Diagram (Video PCB)



and Timing Signals



Address Decoding



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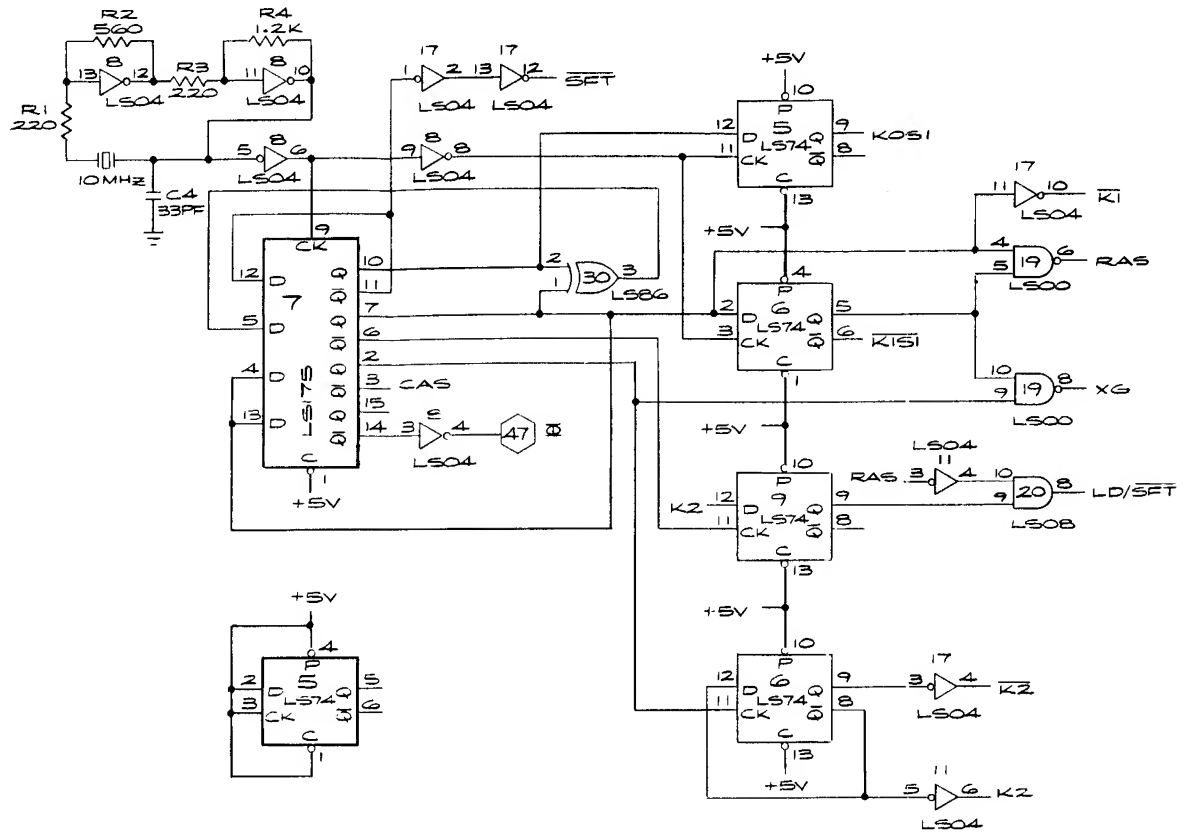
Kangaroo Video PCB Schematic Diagram

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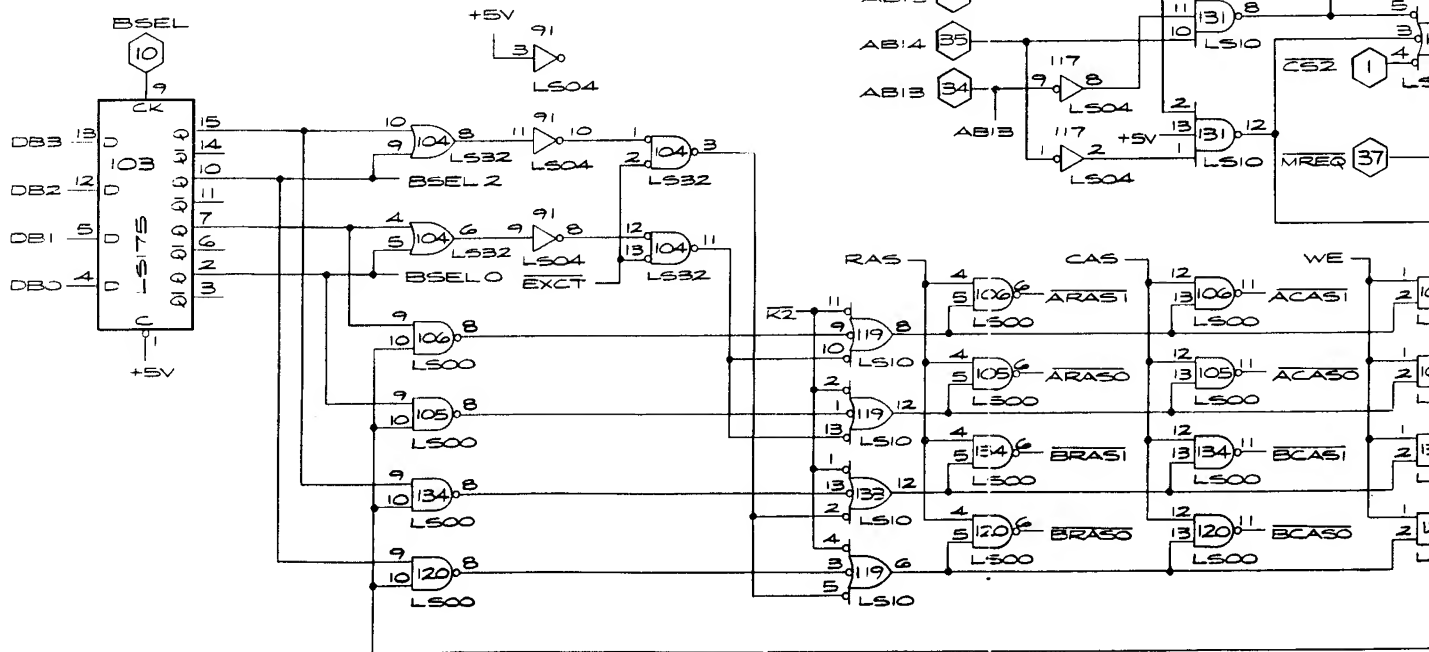
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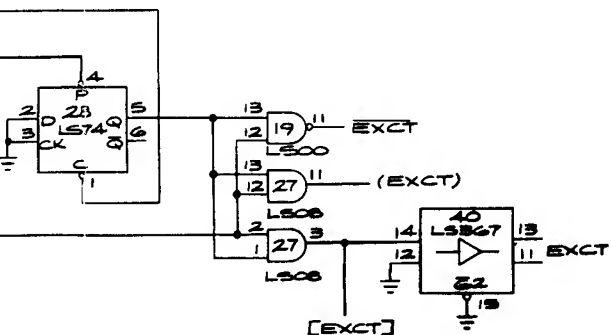
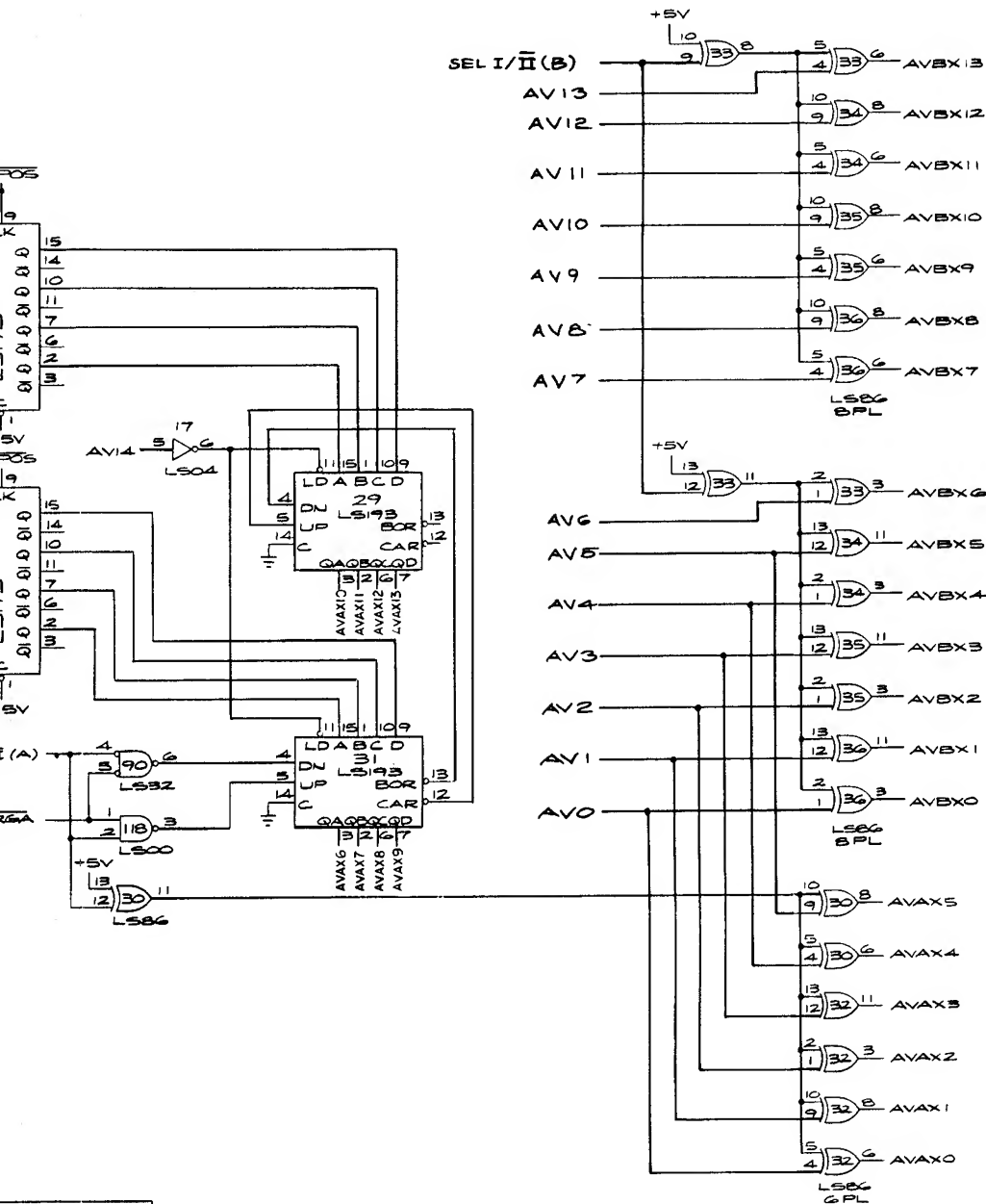
Clock, Sync Chain, a



Dynamic RAM Control



Dynamic RAM Video Address and Flip



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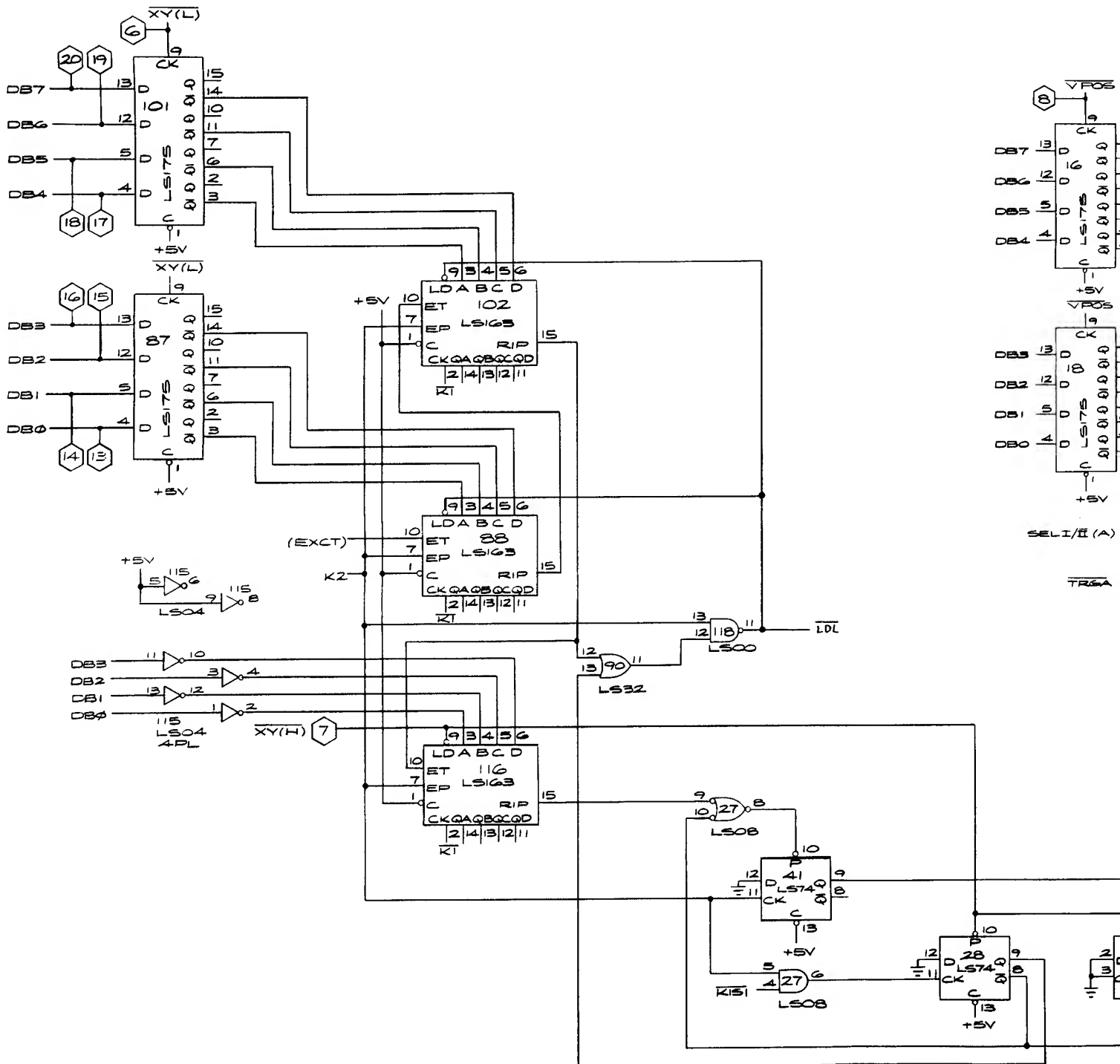
Kangaroo Video PCB Schematic Diagram

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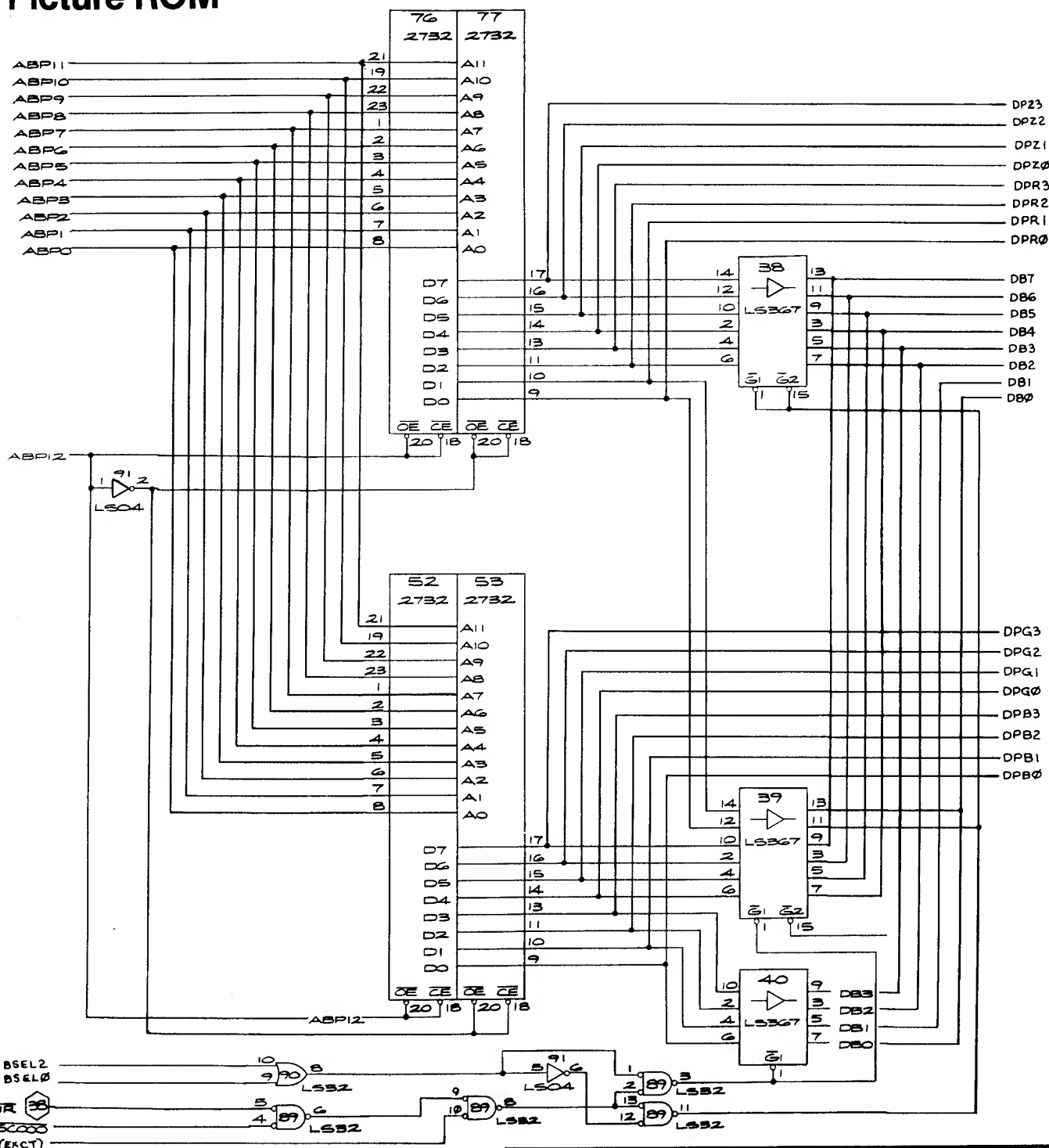
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DMA Control



Picture ROM



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Kangaroo Video PCB Schematic Diagram

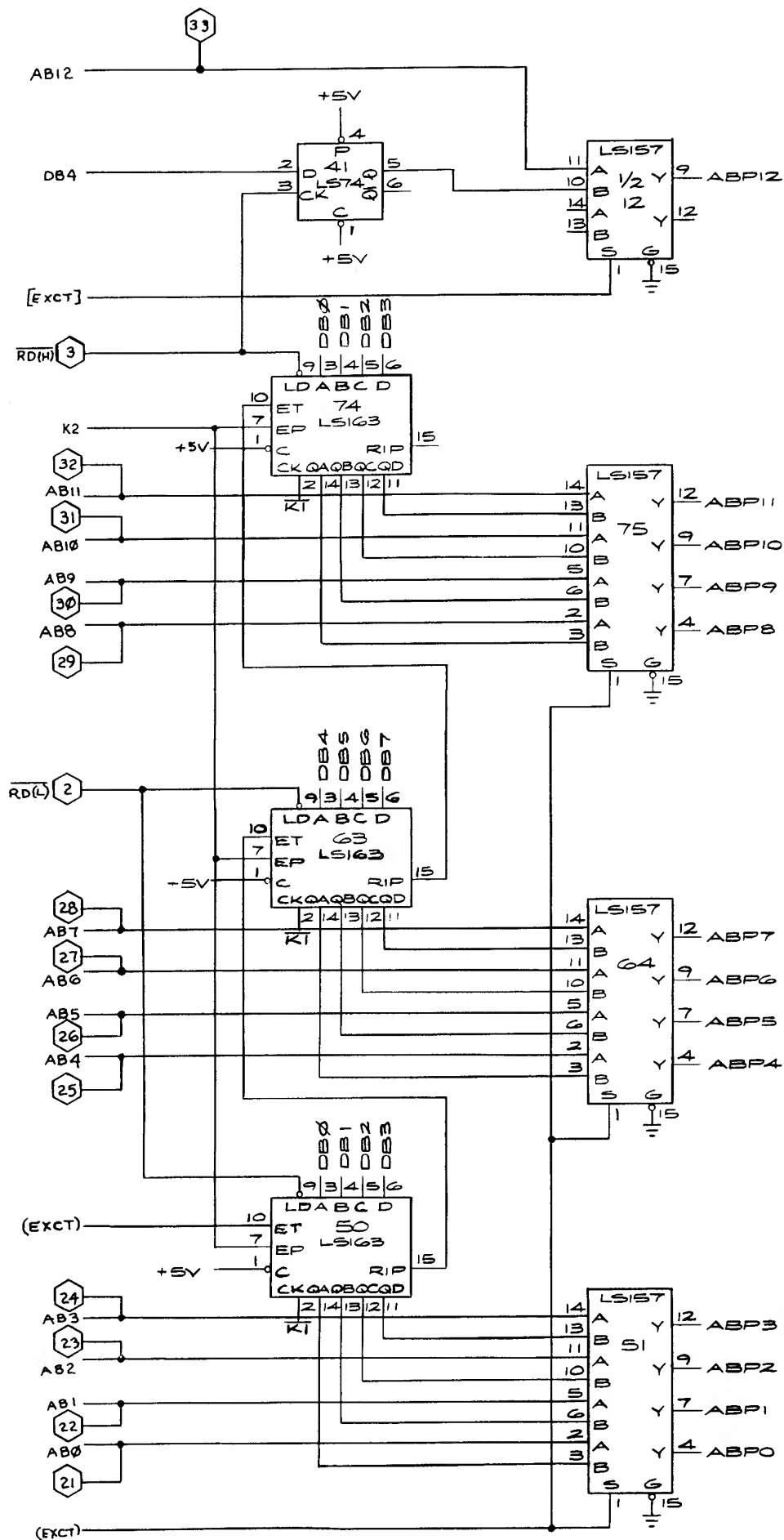
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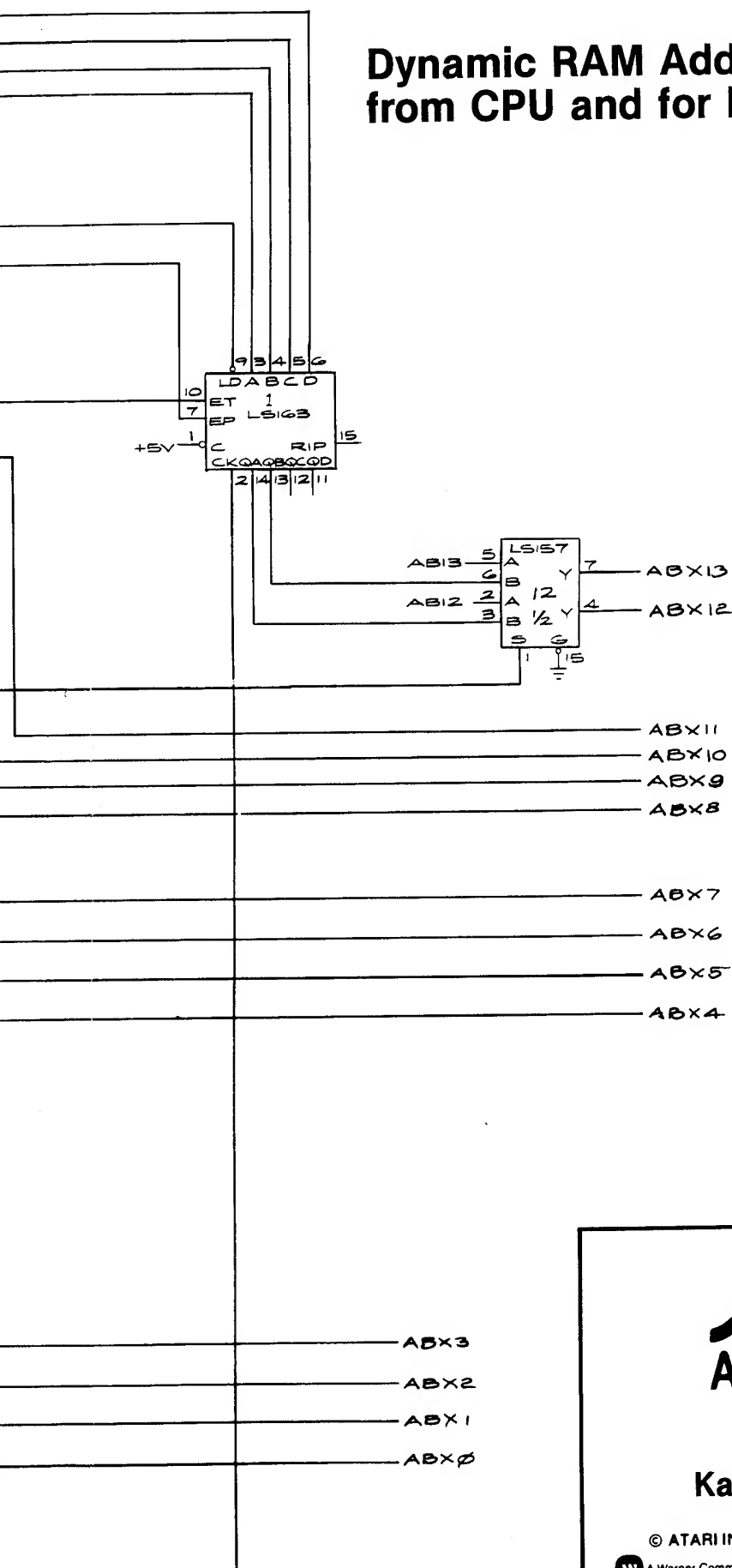
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SP-204 Sheet 9B
 3rd printing

Picture ROM Address Selector



Dynamic RAM Address from CPU and for DMA



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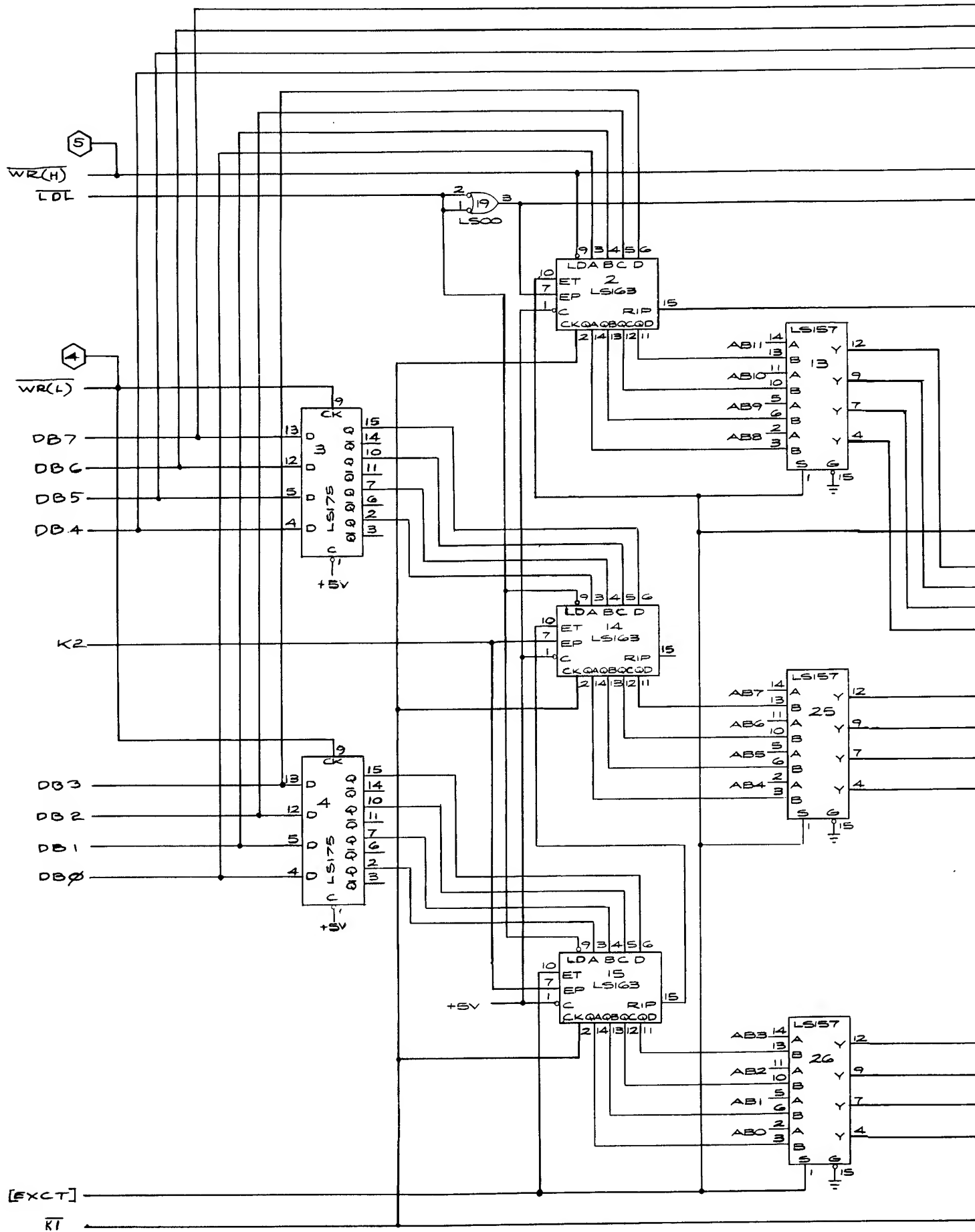
Kangaroo Video PCB Schematic Diagram

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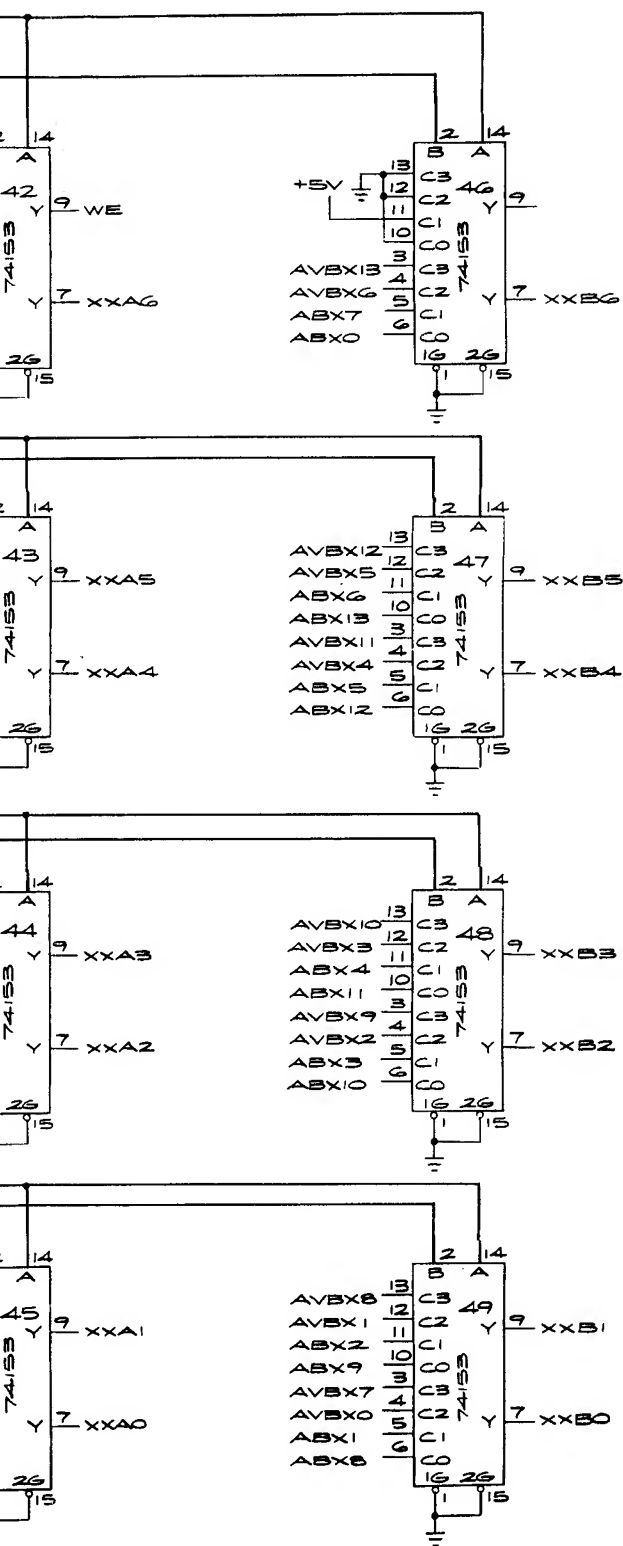


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Address Selector



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Kangaroo Video PCB Schematic Diagram

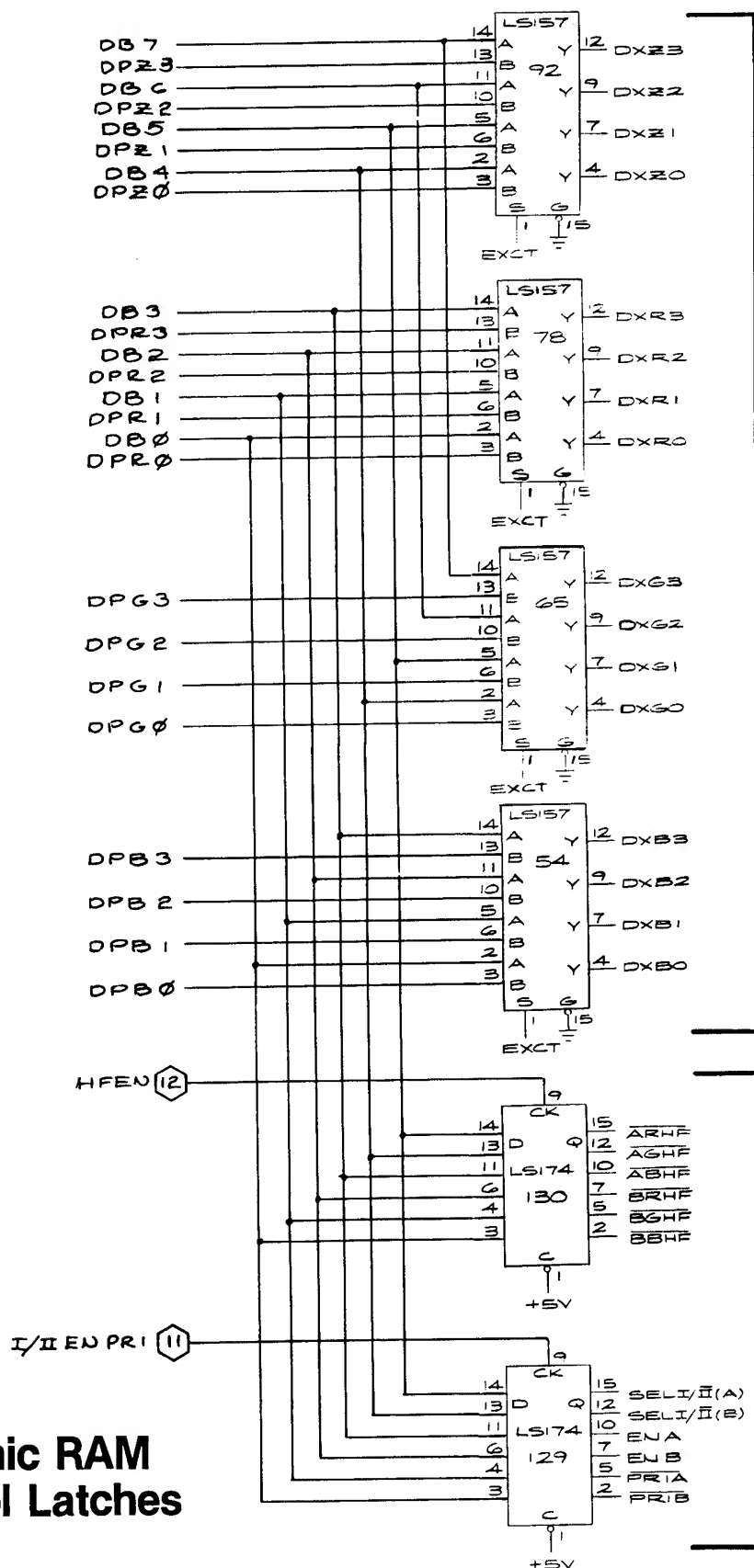
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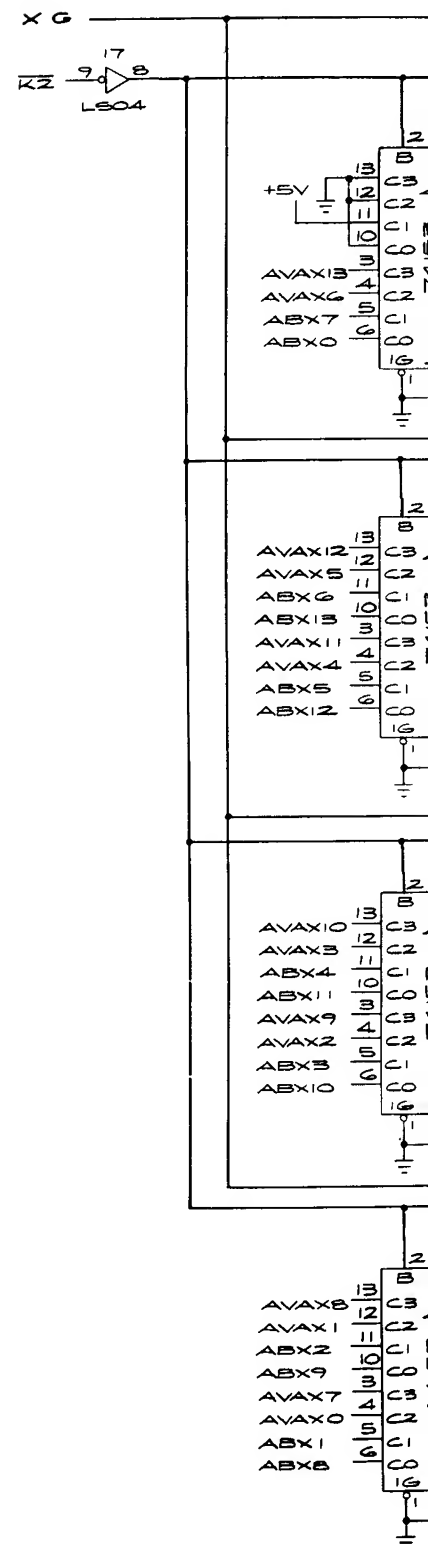
SP-204 Sheet 10B
3rd printing

Dynamic RAM Data Selector

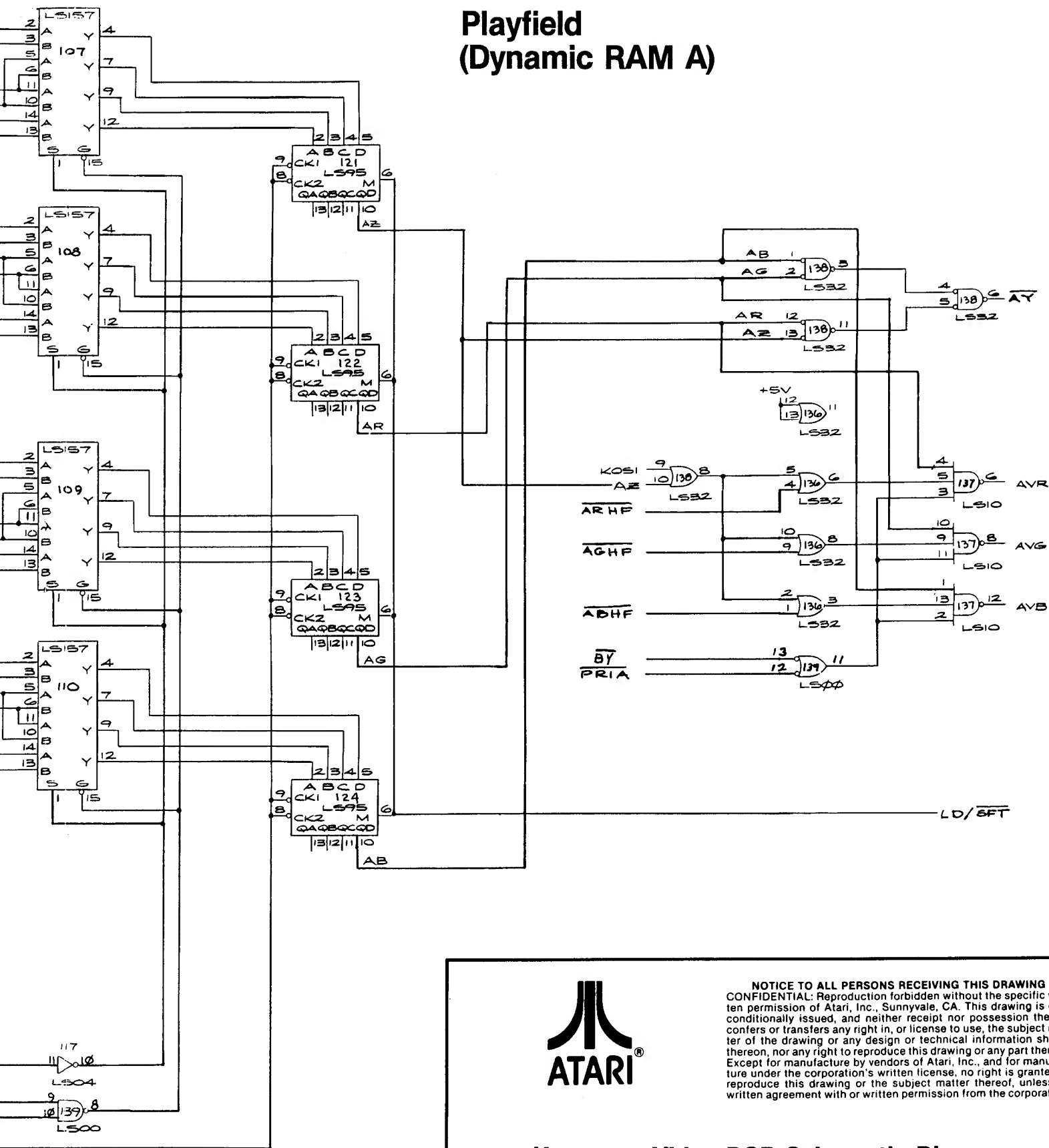
Dynamic RAM



Dynamic RAM Control Latches



Playfield (Dynamic RAM A)



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ACASO

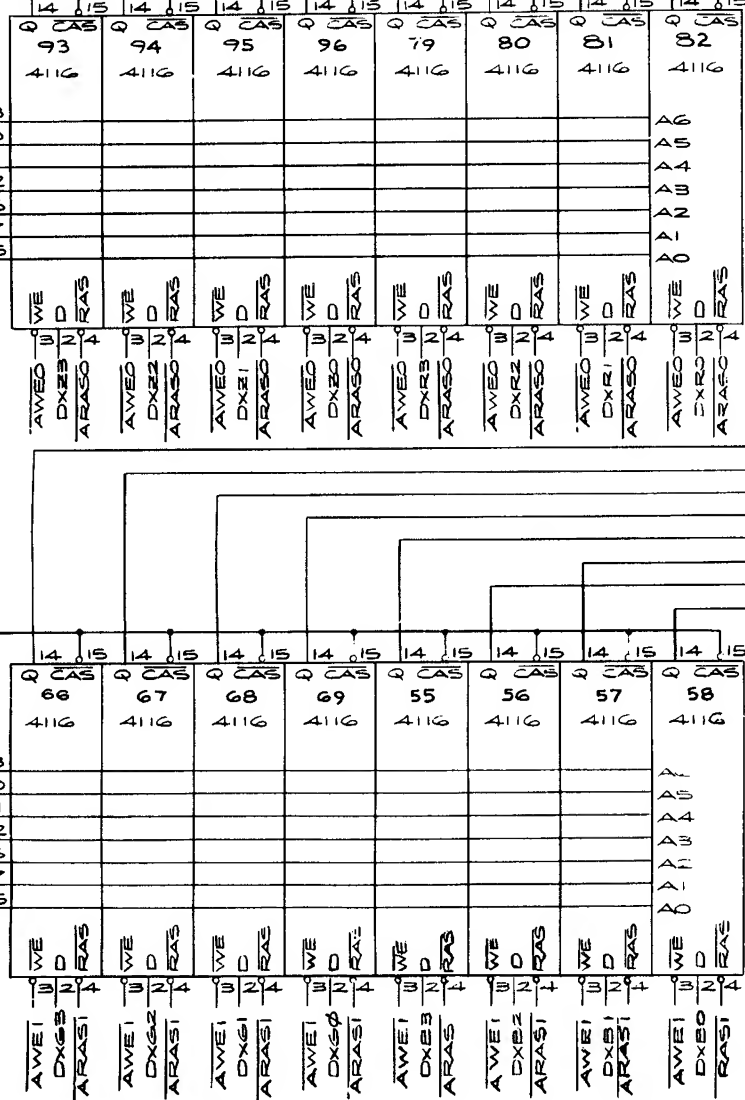
XXXXA6
XXXXA5
XXXXA4
XXXXA3
XXXXA2
XXXXA1
XXXXQ

ACASI

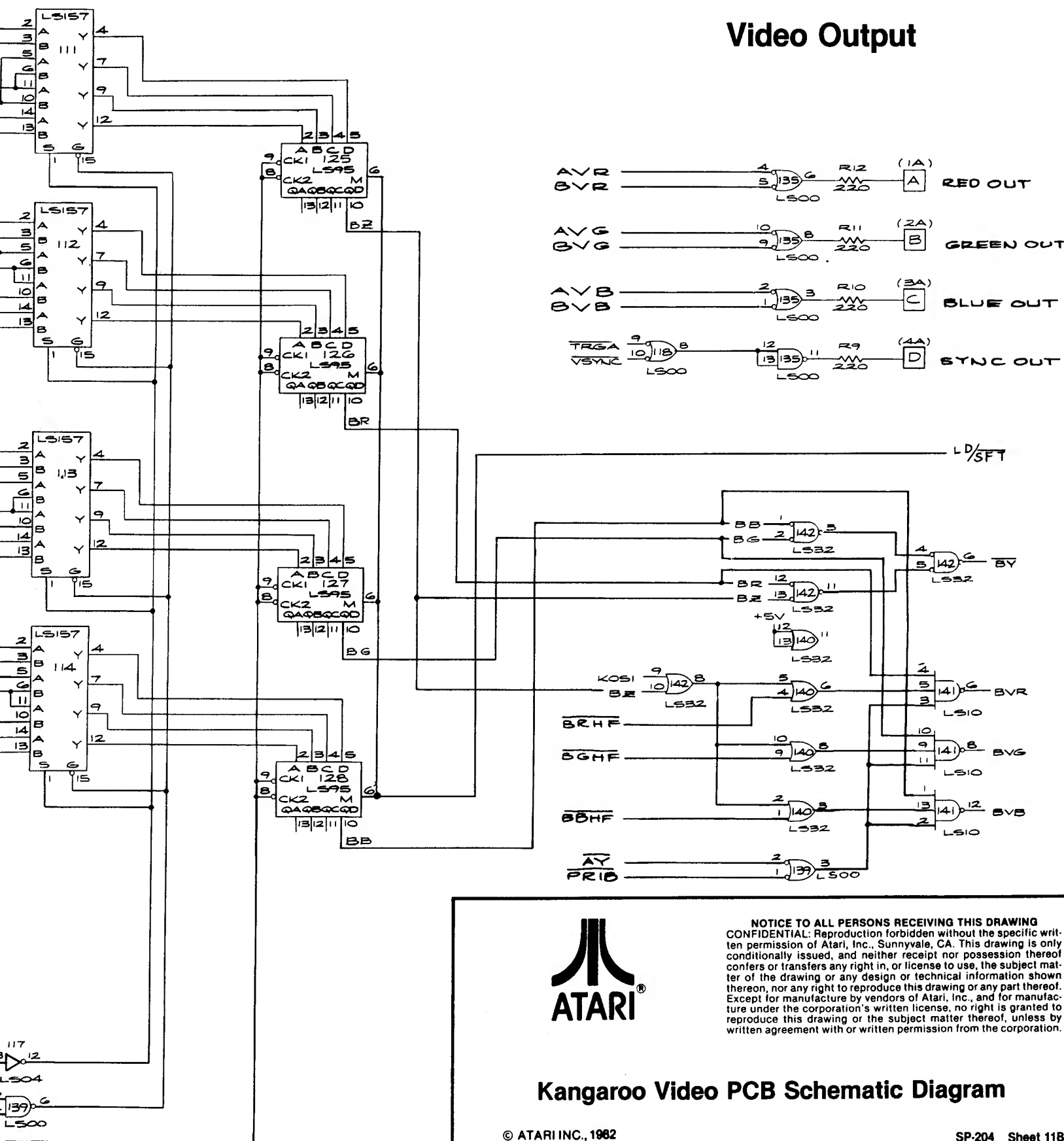
SEL I/II (A)

AV6
ENA

3FT



Video Output



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Motion Object (Dynamic RAM B)

