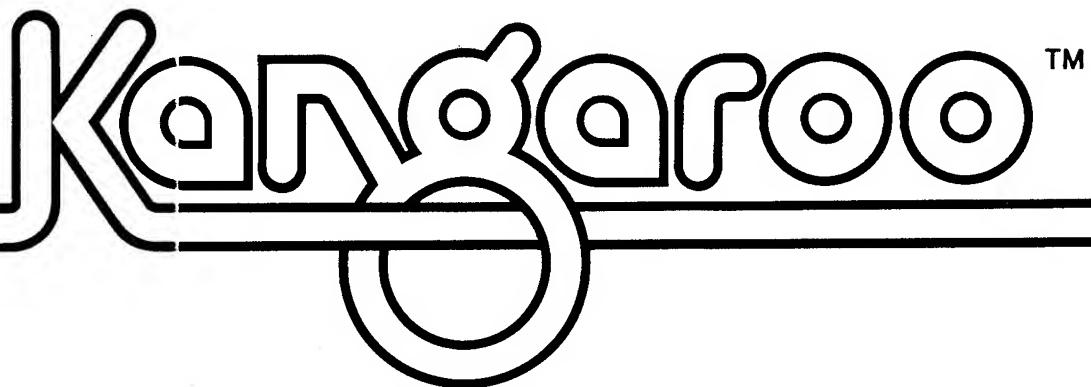


Schematic Package Supplement to



Operation, Maintenance and Service Manual

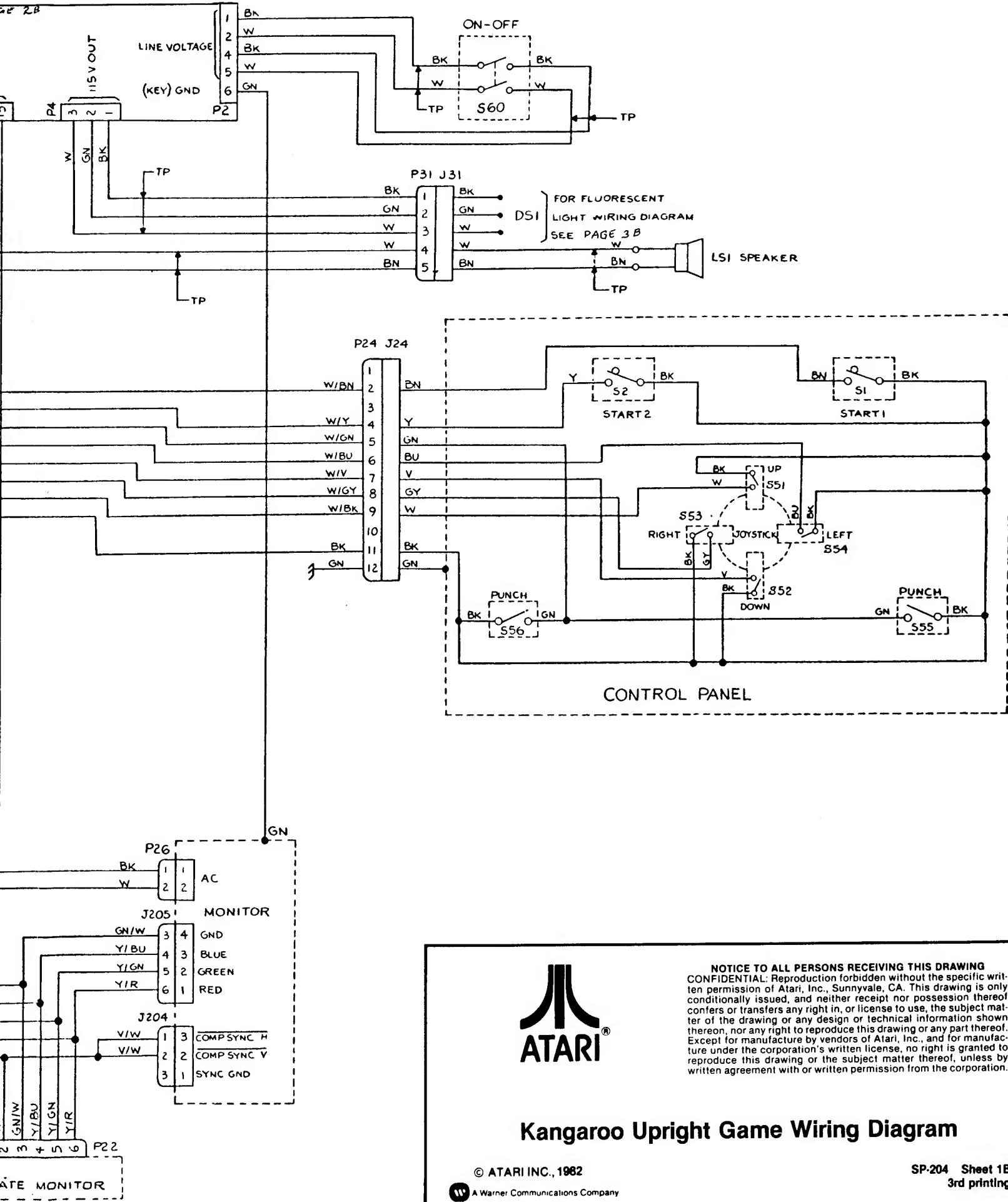
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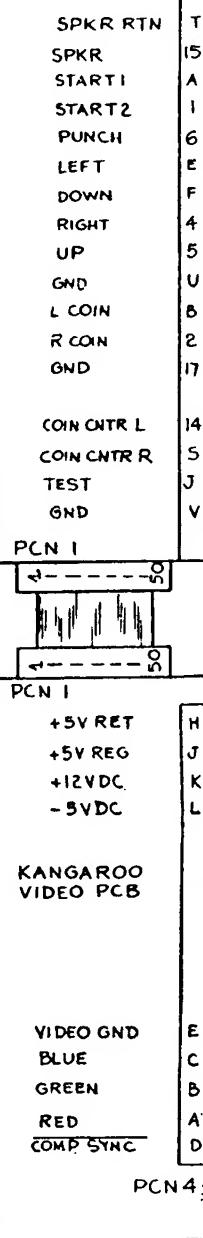
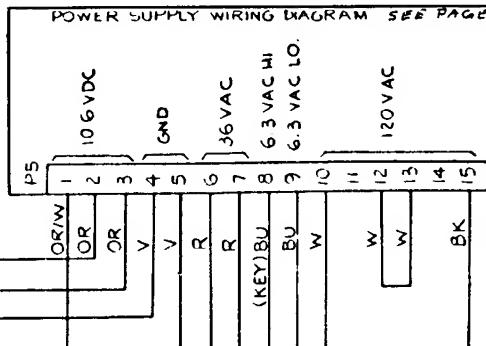
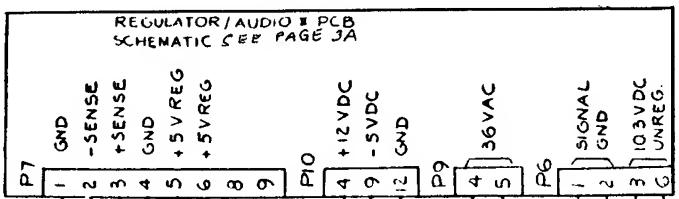
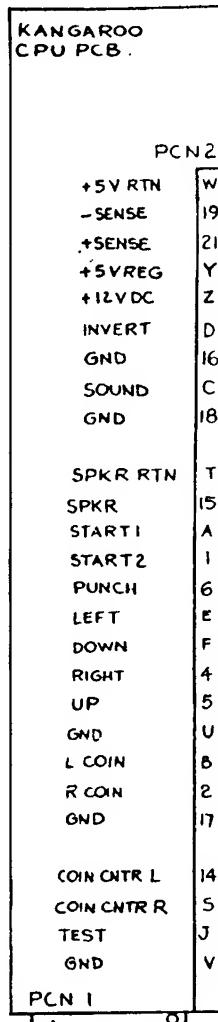
This staple temporarily holds the schematic package together. Remove the staple before using the schematics.



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- Sheet 2A Ireland-Built Kangaroo Game Wiring Diagram (038451-01 A)
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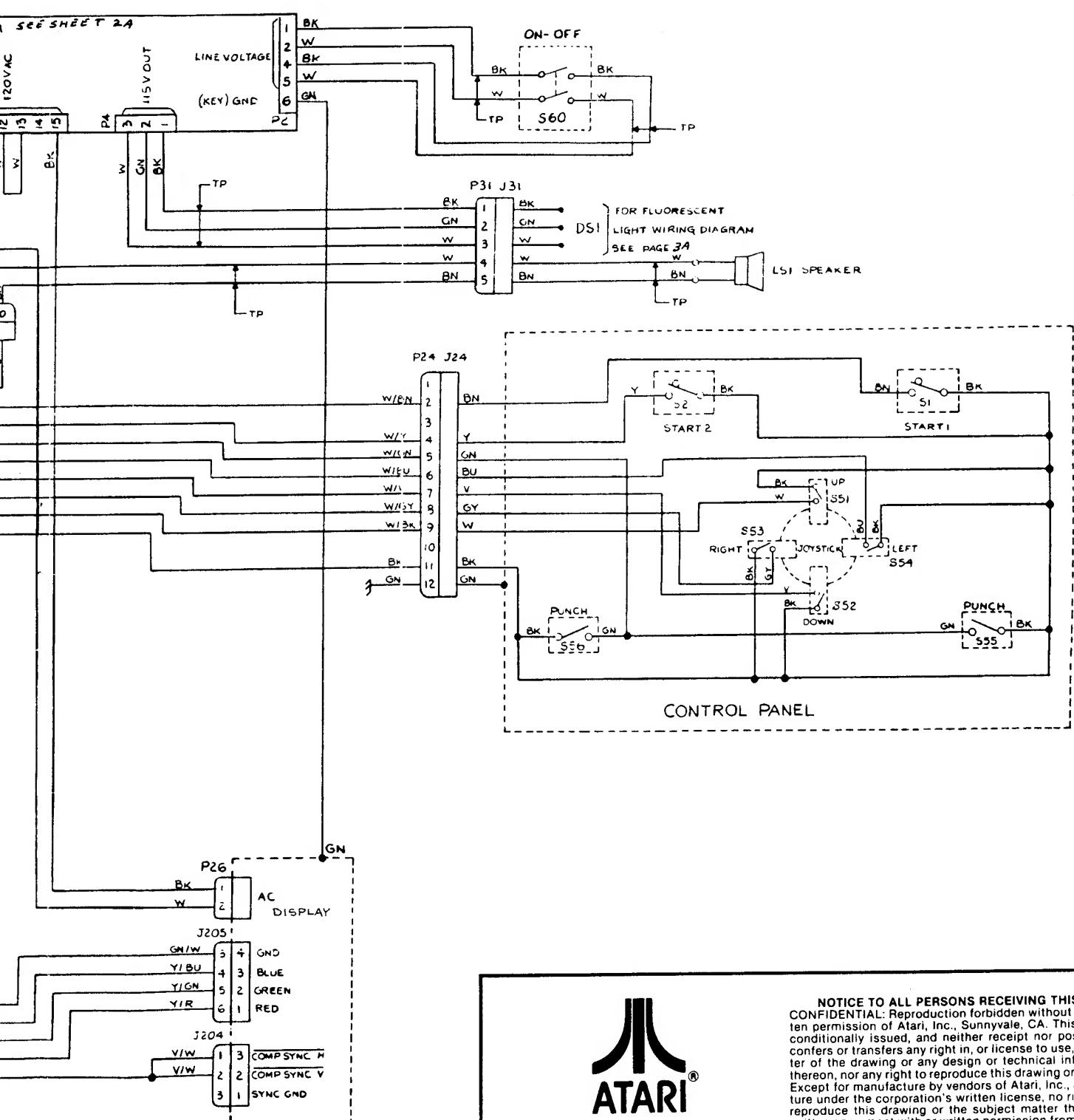




FOR COMPONENT WIRING
DIAGRAM SEE PAGE 3B

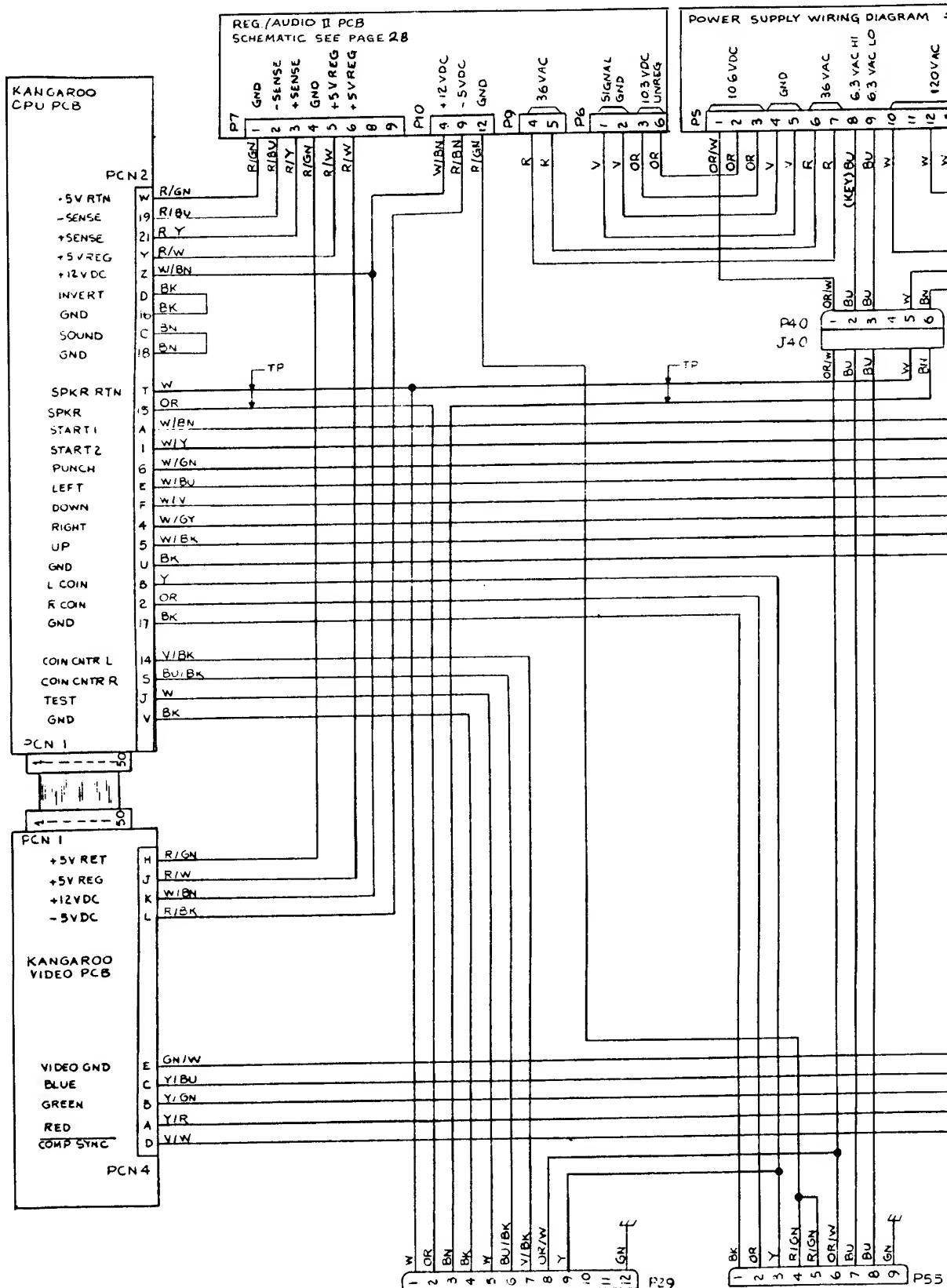
P29 P55 FOR COIN DOOR WIRING
DIAGRAM SEE PAGE 3B

ALTERNAT



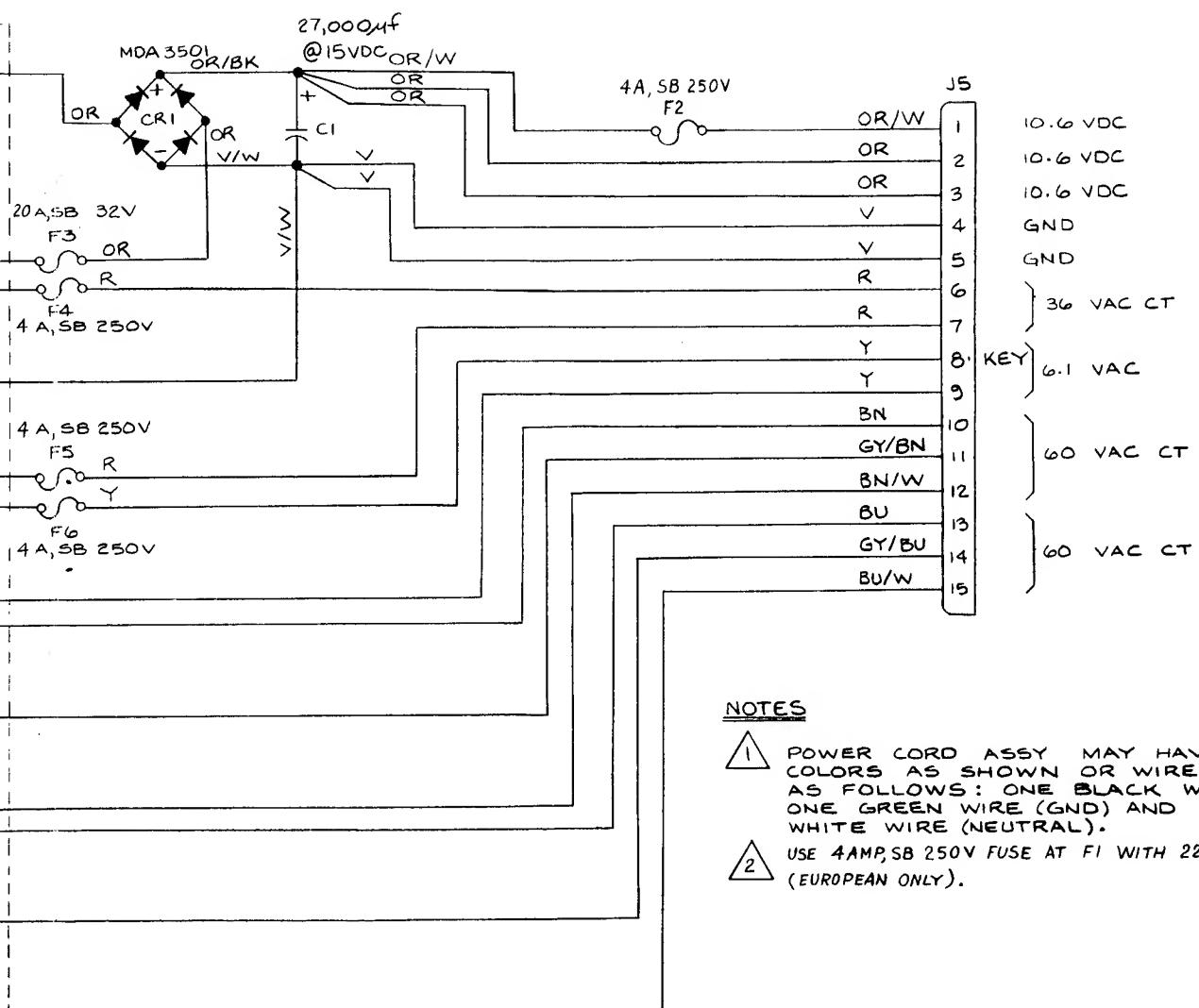
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Ireland-Built Kangaroo Game Wiring Diagram



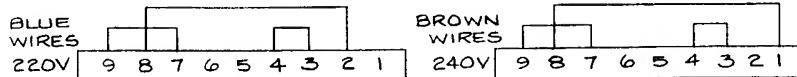
FOR COMPONENT WIRING
DIAGRAM SEE SHEET 3A

FOR COIN DOOR WIRING
DIAGRAM SEE SHEET 3A

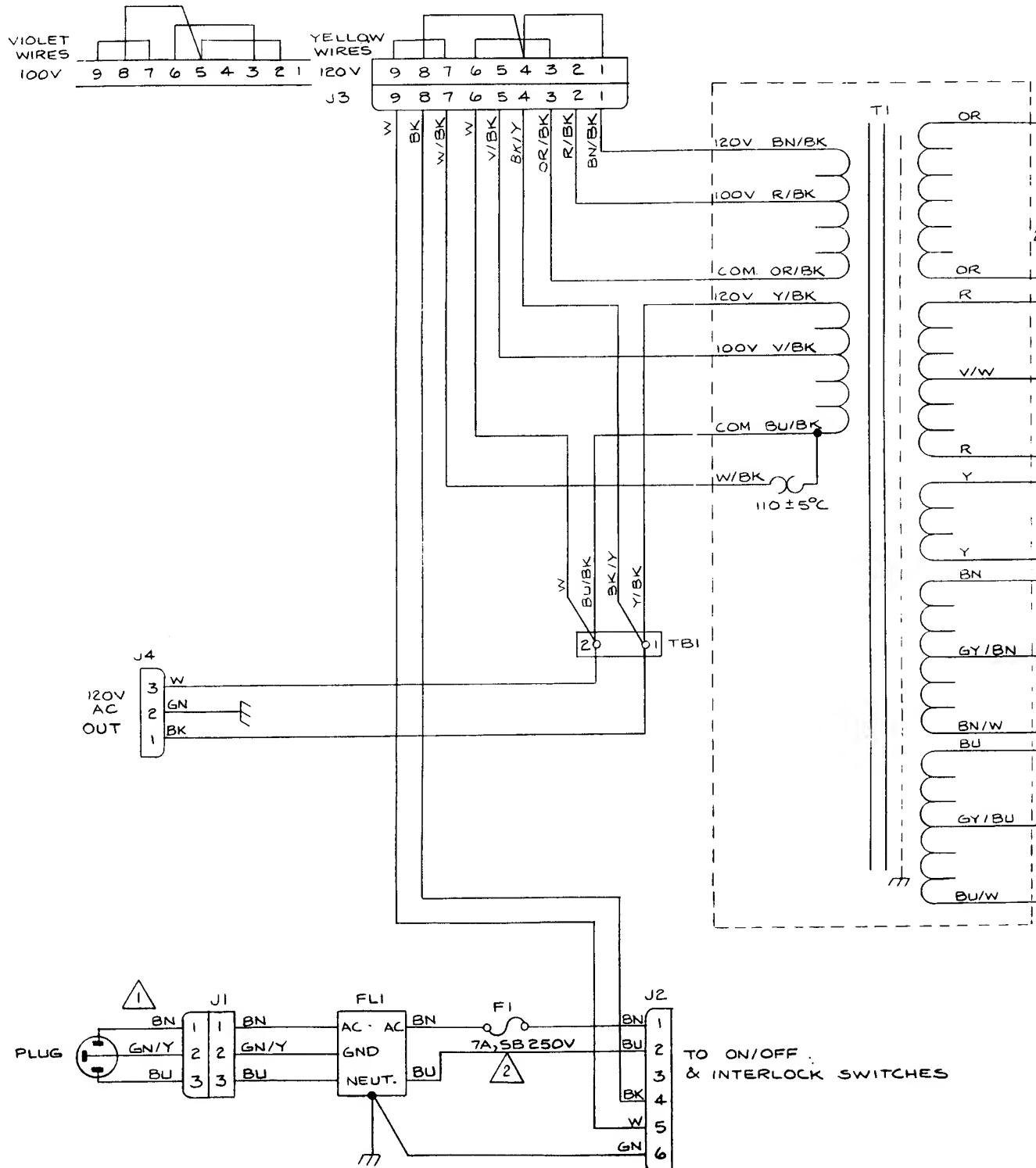


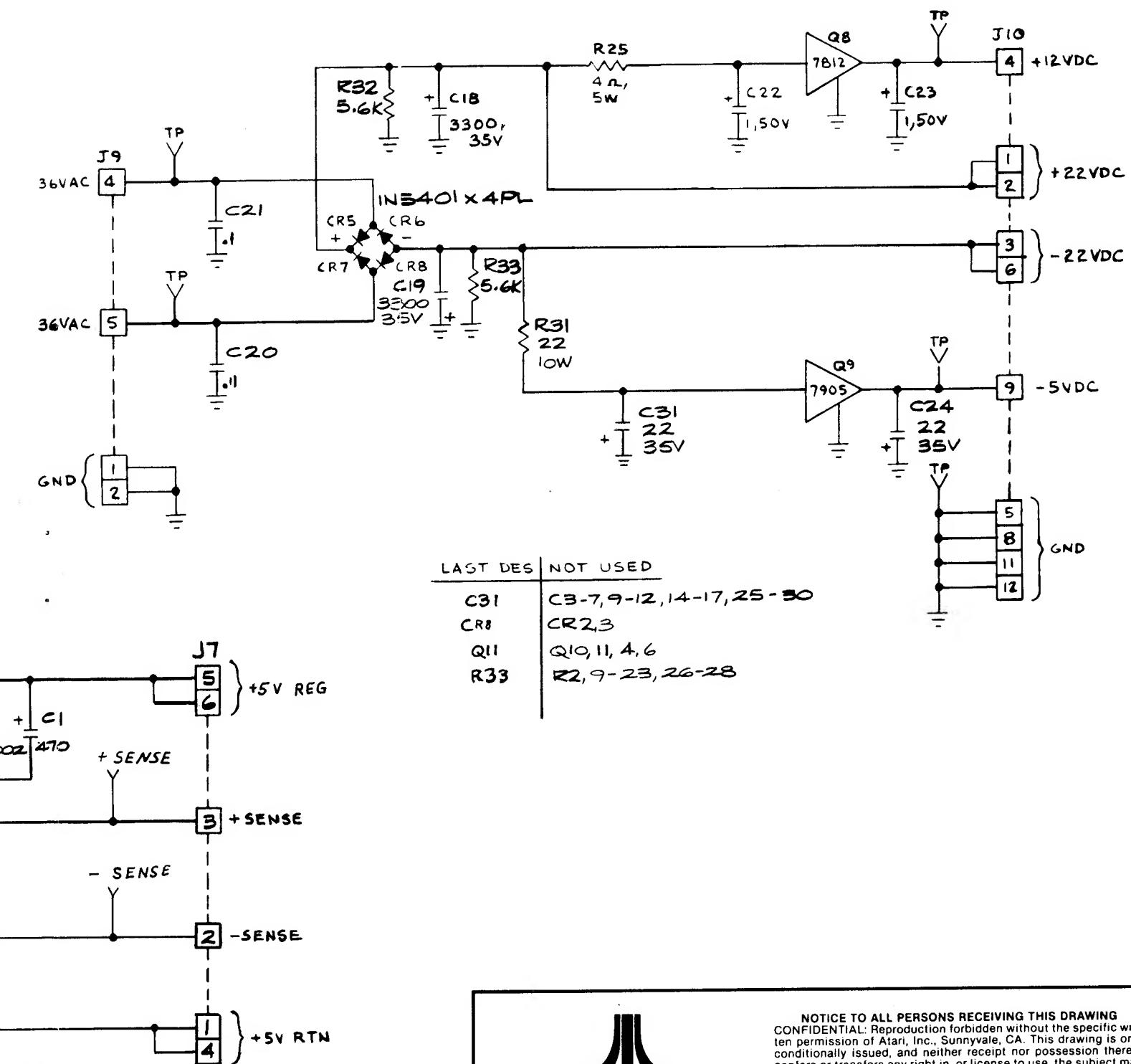
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Kangaroo Power Supply



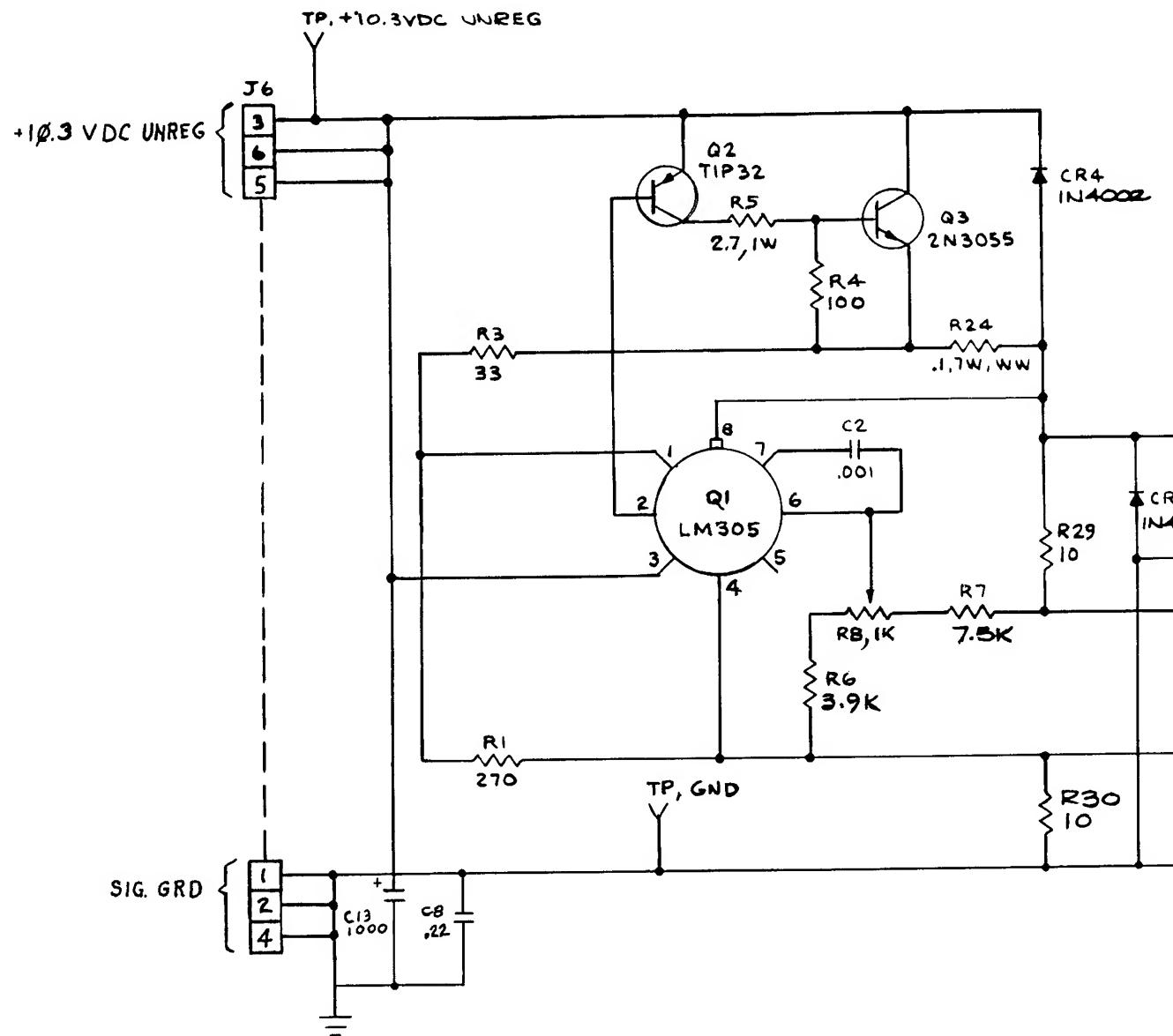
VOLTAGE SELECTION BLOCKS



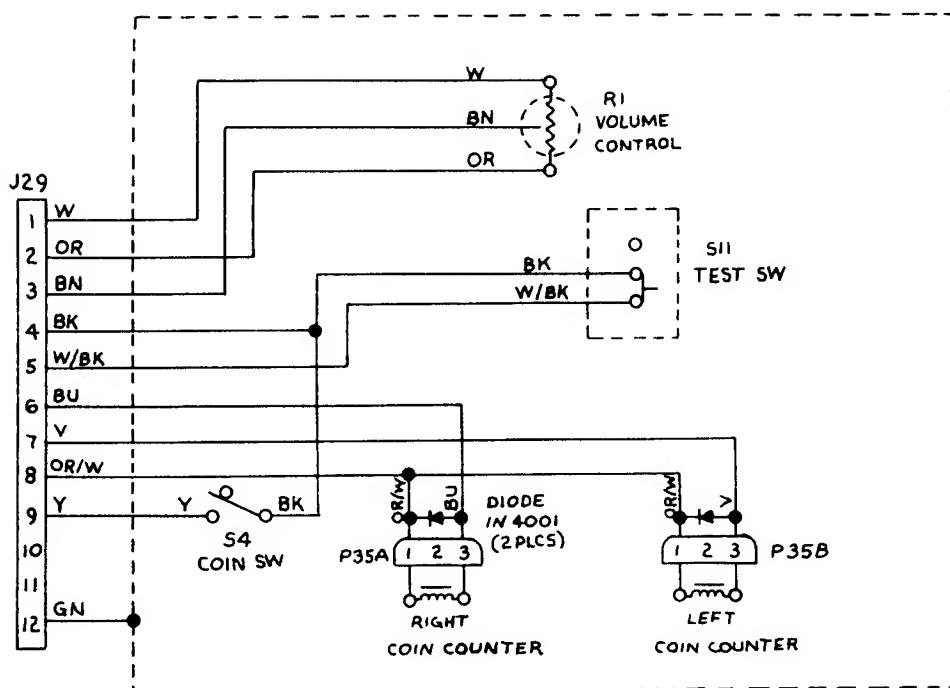


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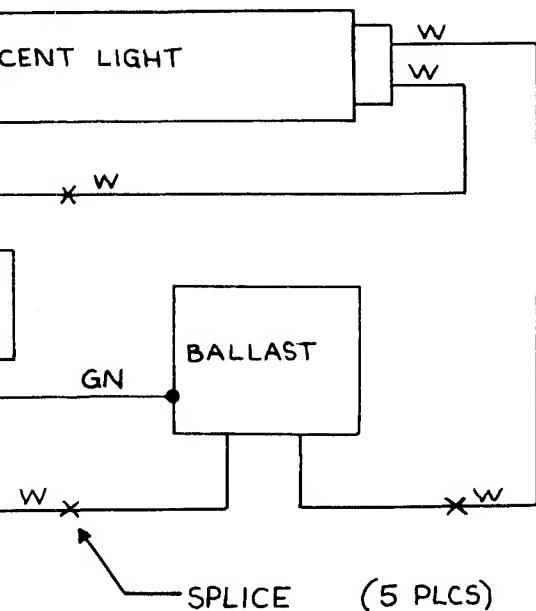
Kangaroo Reg./Audio II PCB Schematic Diagram



Utility Panel Wiring Diagram



Speaker Wiring Diagram

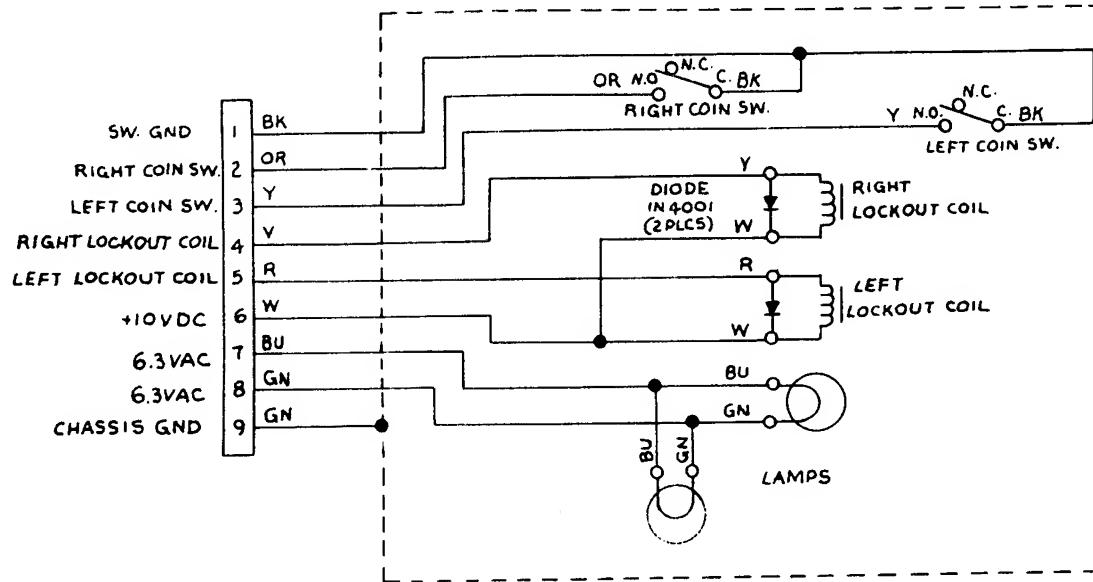


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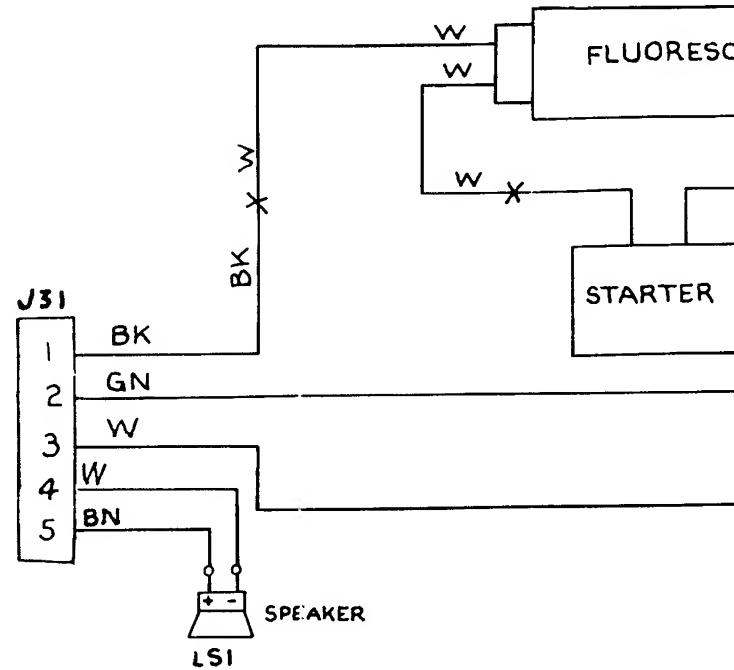


Kangaroo Game Wiring Interfaces

Coin Door Wiring Diagram

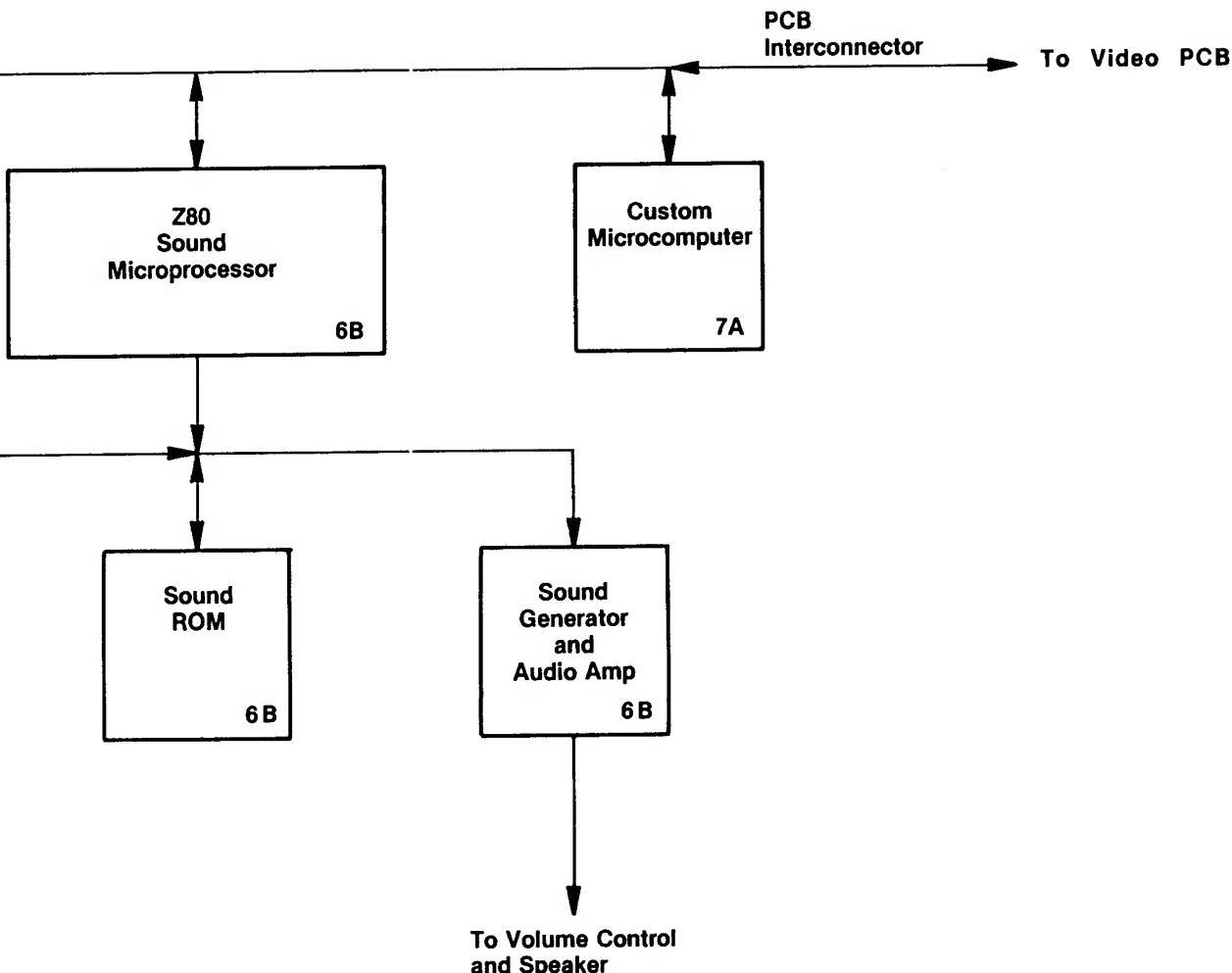


Fluorescent Light and



NOTE

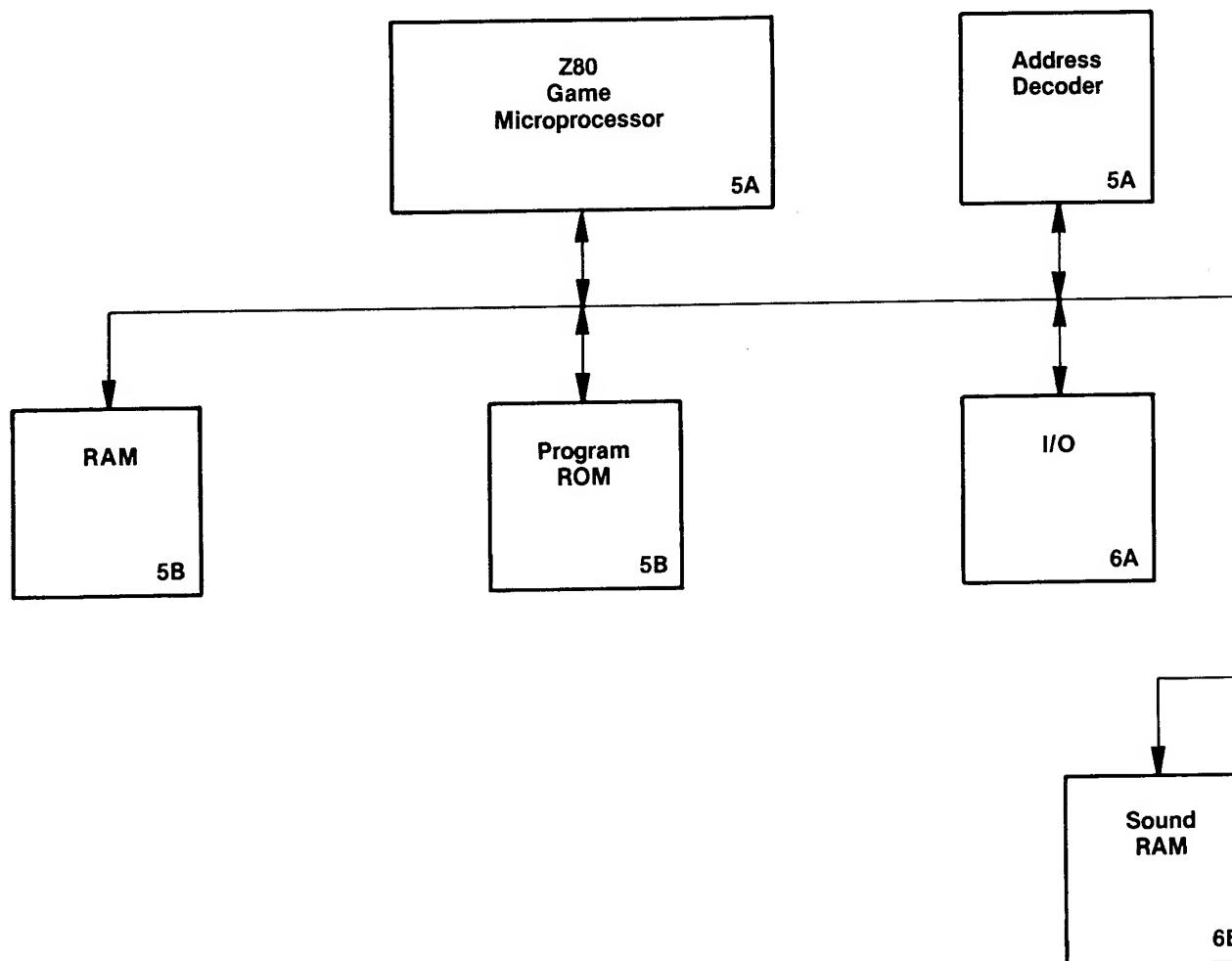
The service switch, located on the CPU PCB, allows you to enter credits without tripping the coin counter.



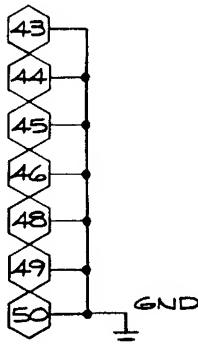
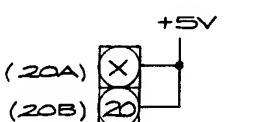
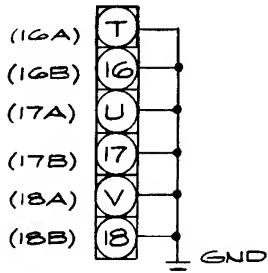
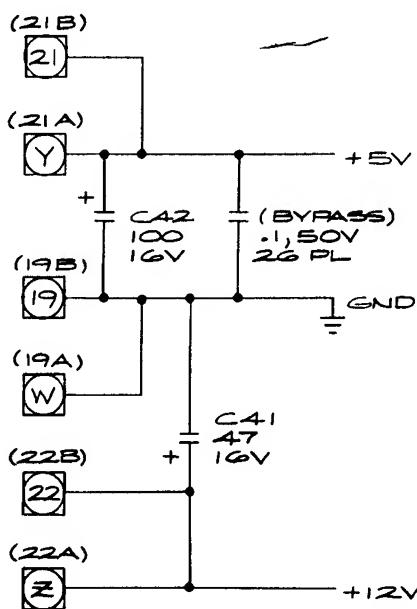
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Kangaroo CPU PCB Schematic Diagram

Block Diagram (CPU PCB)



CPU Power Input



NOTES:

1. = CONNECTOR CN2
2. = CONNECTOR CN1

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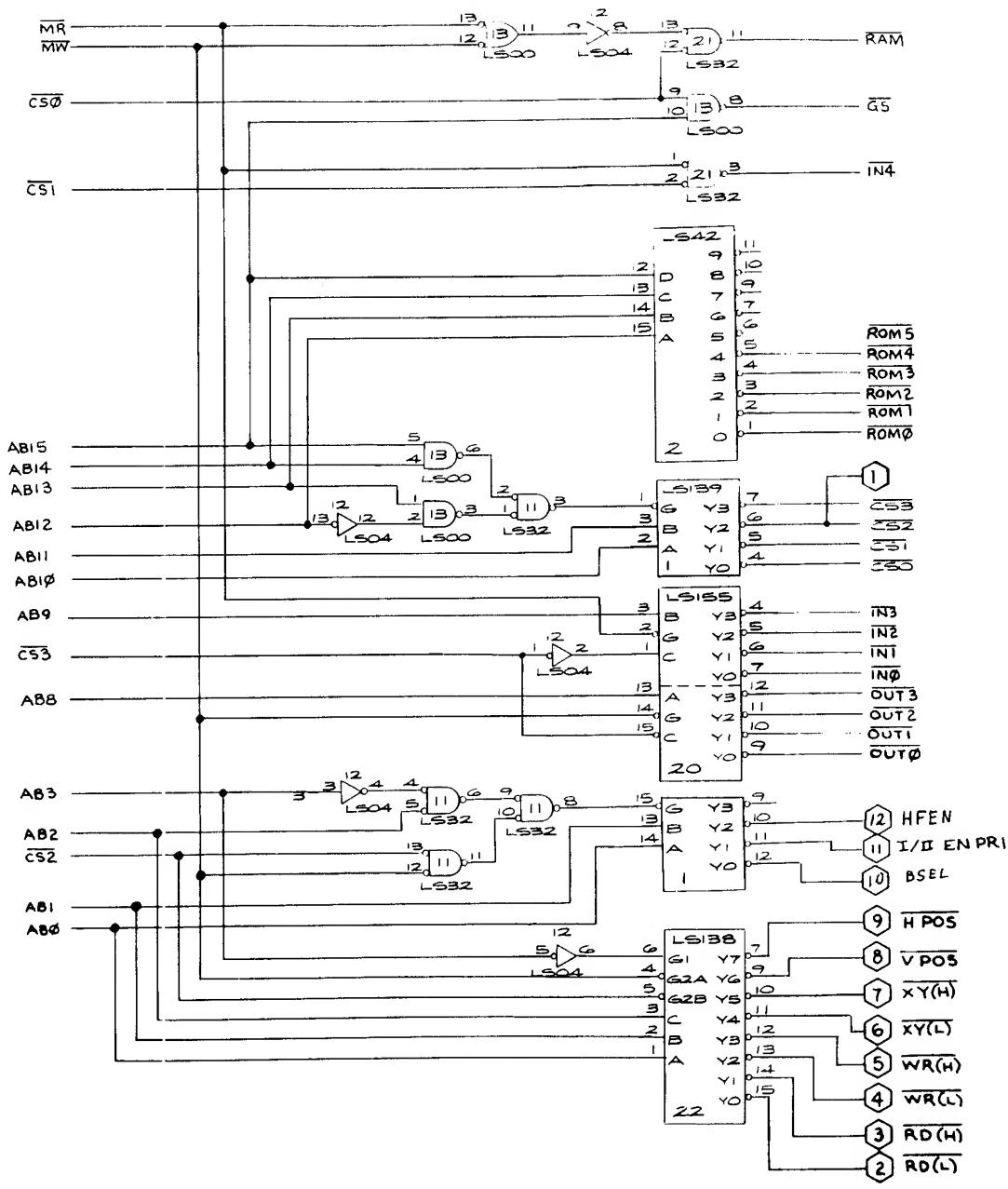


Kangaroo CPU PCB Schematic Diagram

Memory Map

HEXA-DECIMAL ADDRESS	R/W	DATA D7 D6 D5 D4 D3 D2 D1 D0	FUNCTION
Game Microprocessor Memory Space (IC15)			
0000-5FFF	R	D D D D D D D D	Z80 24K Program ROM
E000-E3FF	R/W	D D D D D D D D	1K Working RAM
E400	R	D D D D D D D D	Option Switch
E800	W	D D D D D D D D	Low Byte] Start Address of Data in Picture
E801	W	D D D D D D D D	High Byte] ROM for DMA
E802	W	D D D D D D D D	Low Byte] Start Address in Bit Map RAM (where
E803	W	D D D D D D D D	High Byte] picture is to be written) During DMA
E804	W	D D D D D D D D	Low Byte] Picture Size for DMA
E805	W	D D D D D D D D	High Byte] and DMA Start
E806	W	D D D D D D D D	Vertical Start Address in Bit Map
E807	W	D D D D D D D D	Horizontal Start Address in Bit Map
E808	W	D D D D D D D D	Bank Select Latch
E809	W	D D D D D D D D	A & B Bit Map Control Latch (A = playfield, B = motion)
E80A	W	D D D D D D D D	Color-Shading Latch
EC00	W	D D D D D D D D	Sound DATA to Sound Microprocessor
EC00	R	D D D D D D D D	Utility Coin Switch
EC00	R	D D D D D D D D	1 Player Start
EC00	R	D D D D D D D D	2 Player Start
EC00	R	D D D D D D D D	Left Coin Input
EC00	R	D D D D D D D D	Right Coin Input
ED00	W	D D D D D D D D	Coin Counter 1
ED00	W	D D D D D D D D	Coin Counter 2 (European games)
ED00	R	D D D D D D D D	Player 1 Right
ED00	R	D D D D D D D D	Player 1 Left
ED00	R	D D D D D D D D	Player 1 Up
ED00	R	D D D D D D D D	Player 1 Down
ED00	R	D D D D D D D D	Player 1 Punch
EE00	R	D D D D D D D D	Player 2 Right
EE00	R	D D D D D D D D	Player 2 Left
EE00	R	D D D D D D D D	Player 2 Up
EE00	R	D D D D D D D D	Player 2 Down
EE00	R	D D D D D D D D	Player 2 Punch
EFXX	W	D D D D D D D D	Output to Custom Microcomputer
EFXX	R	D D D D D D D D	Input from Custom Microcomputer
Sound Microprocessor Memory Space (IC34)			
0000-0FFF	R	D D D D D D D D	4K Program ROM
4000-43FF	R/W	D D D D D D D D	1K Working RAM
6000	R	D D D D D D D D	Read DATA from Game Microprocessor
7000	W	D D D D D D D D	Write to Sound Chip (GI-AY-3-8910)
8000	R	D D D D D D D D	Read from Sound Chip

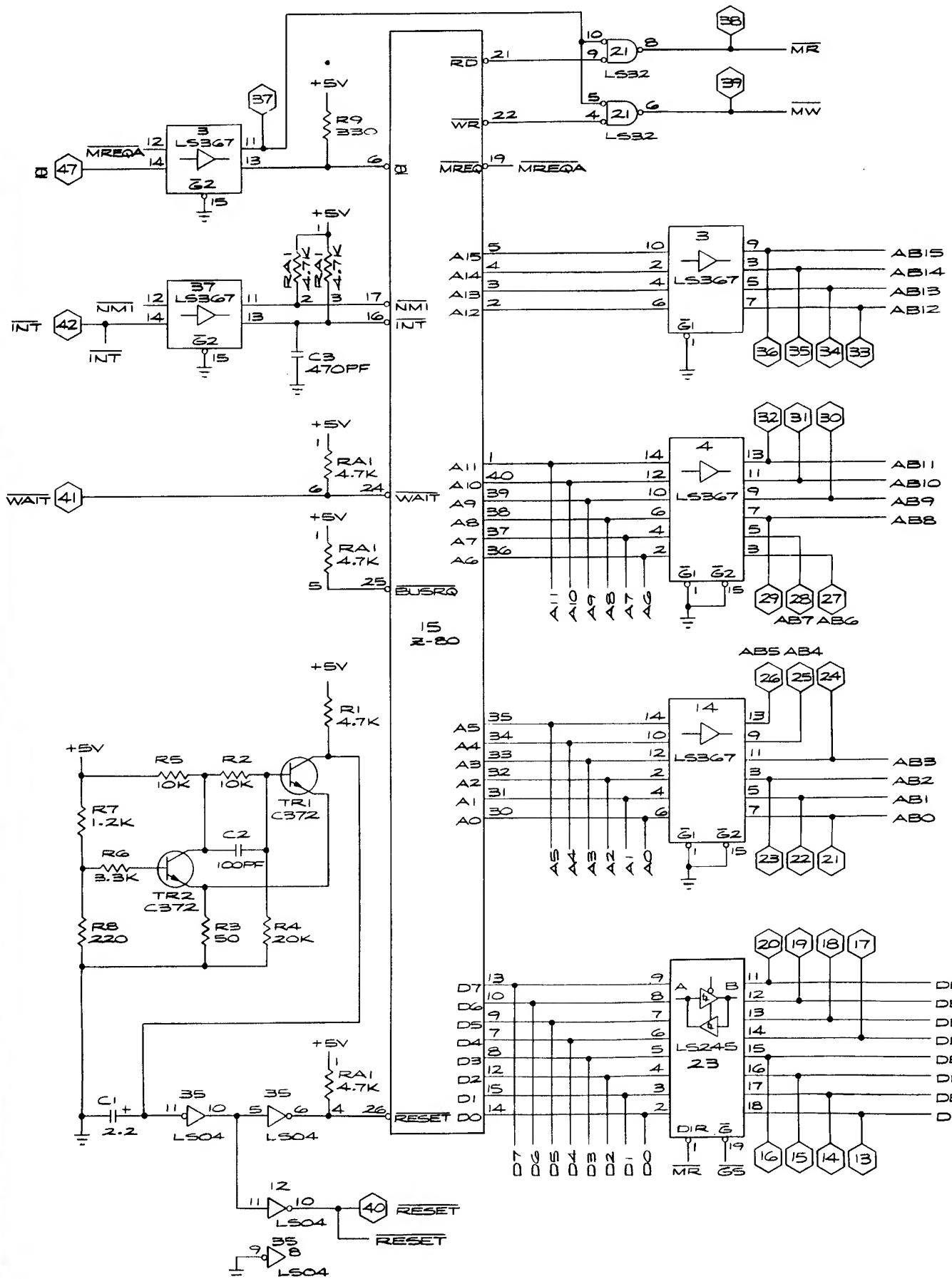
Address Decoder



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Kangaroo CPU PCB Schematic Diagram

Game Microprocessor





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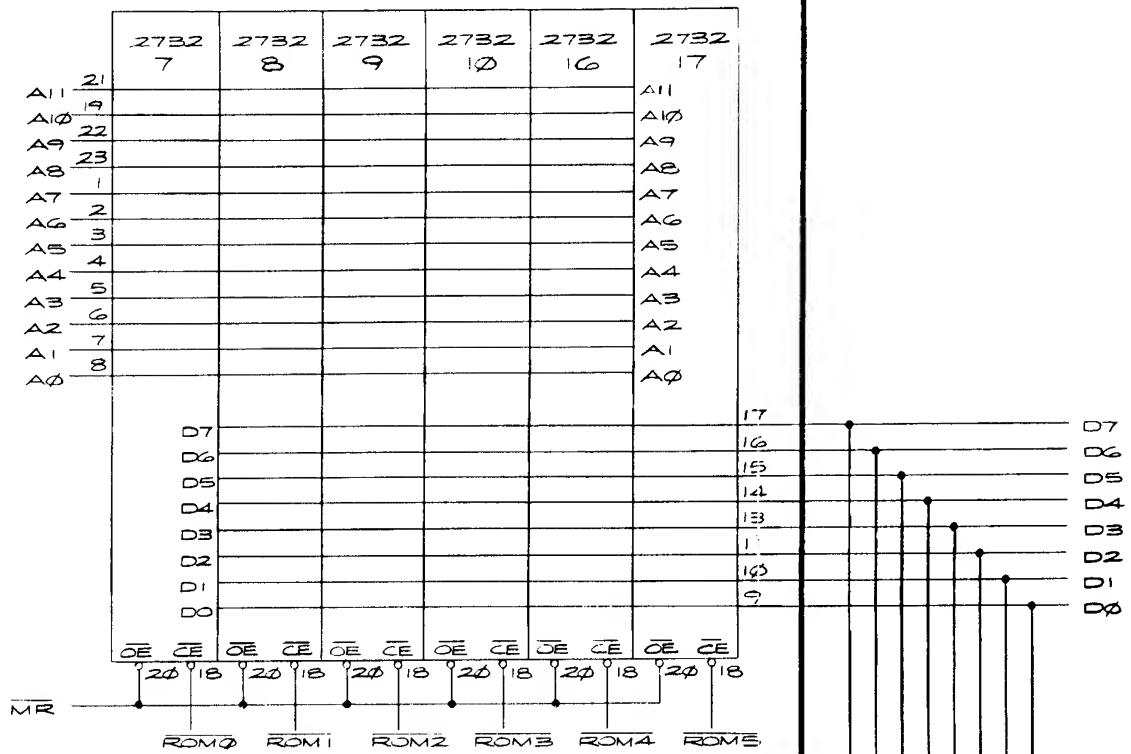
Kangaroo CPU PCB Schematic Diagram

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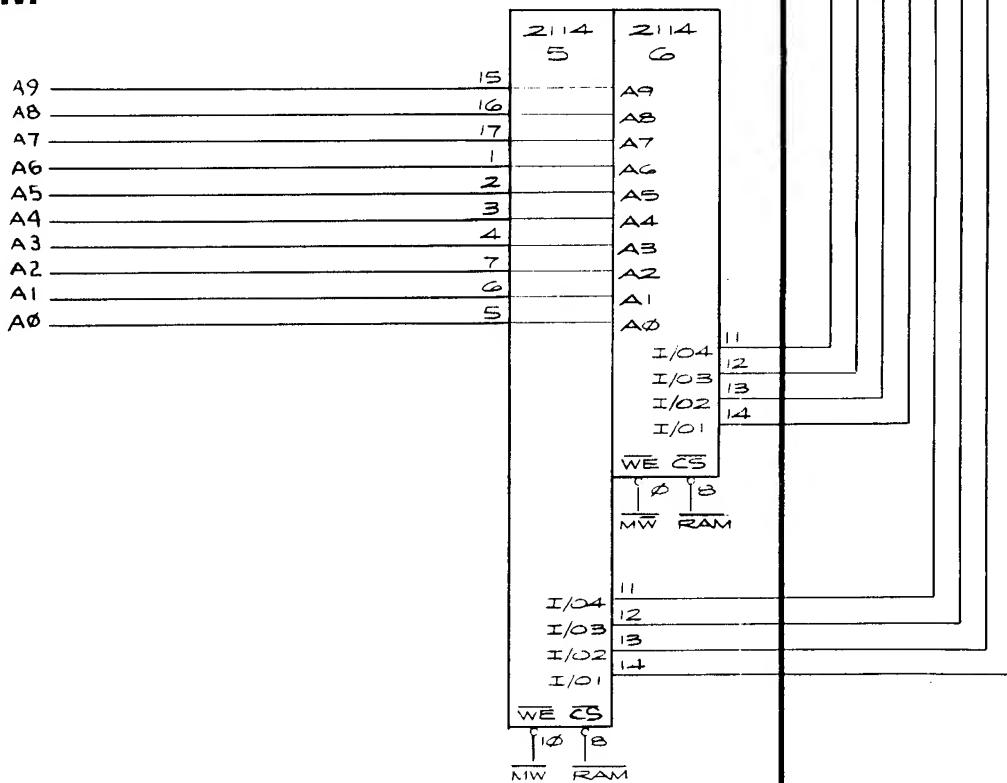
 A Warner Communications Company

SP-204 Sheet 5B
3rd printing

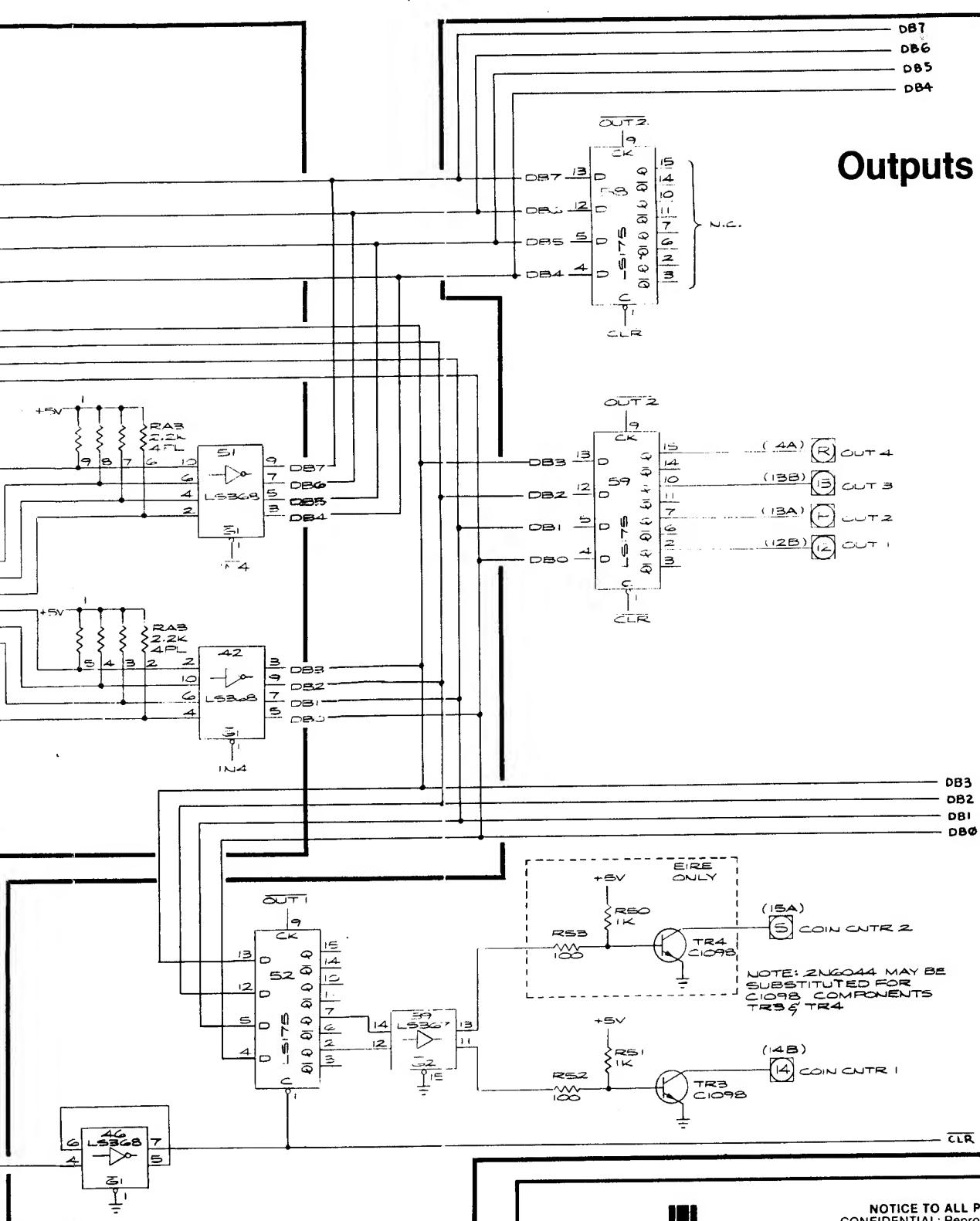
Program ROM



RAM



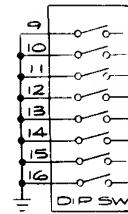
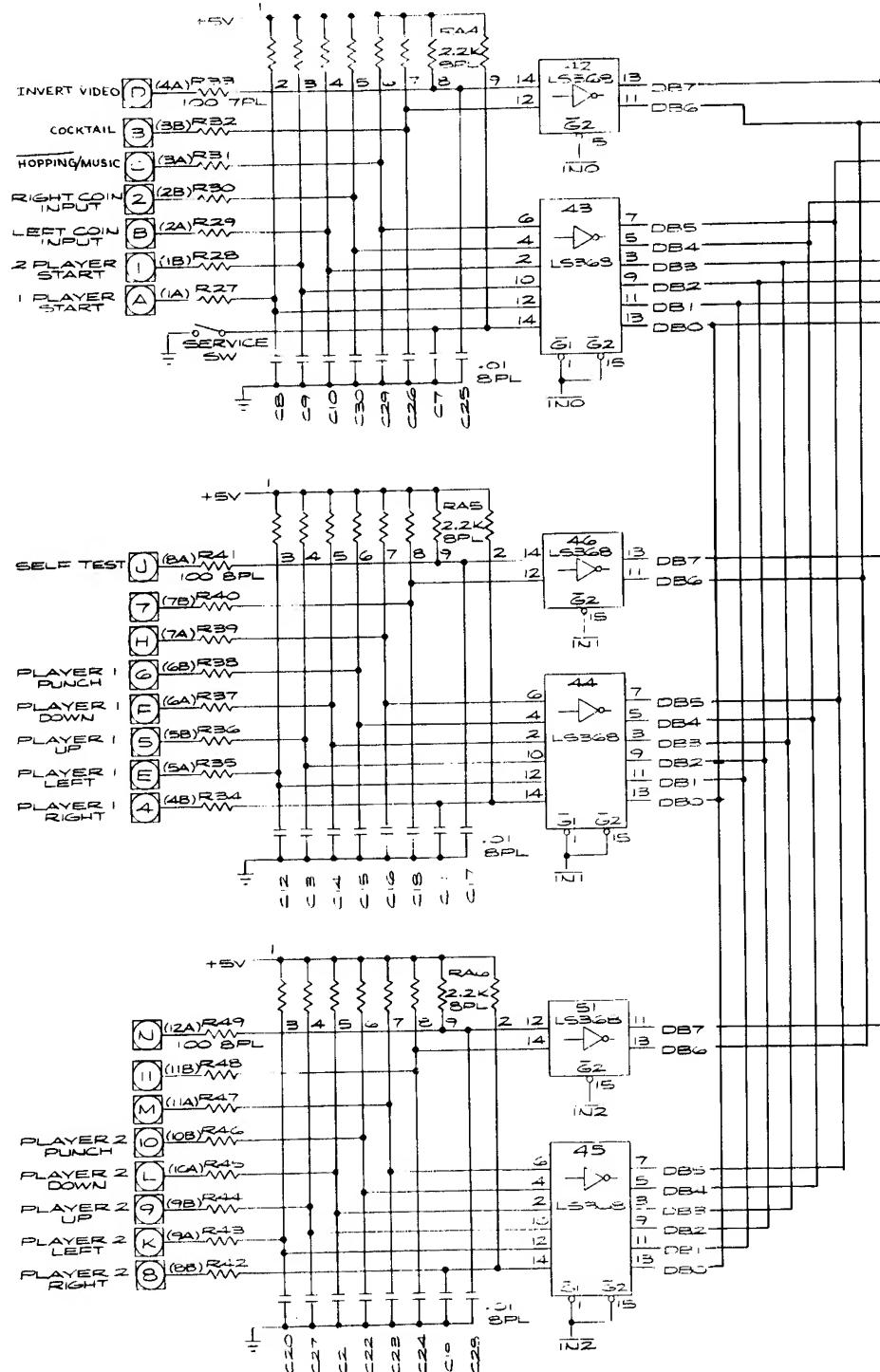
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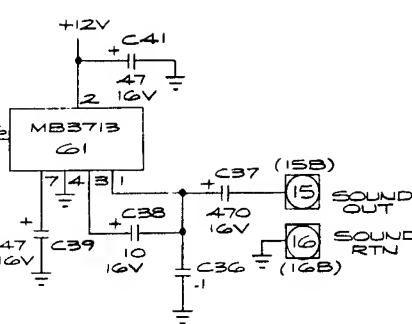
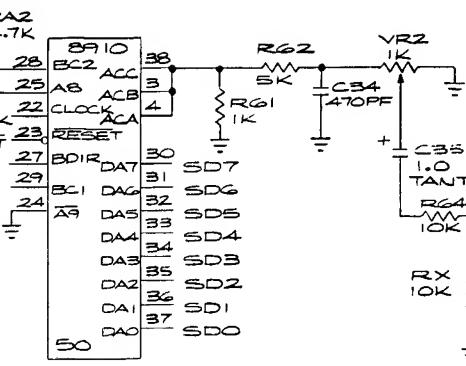
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Kangaroo CPU PCB Schematic Diagram

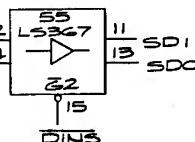
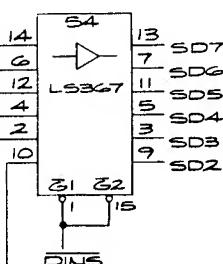
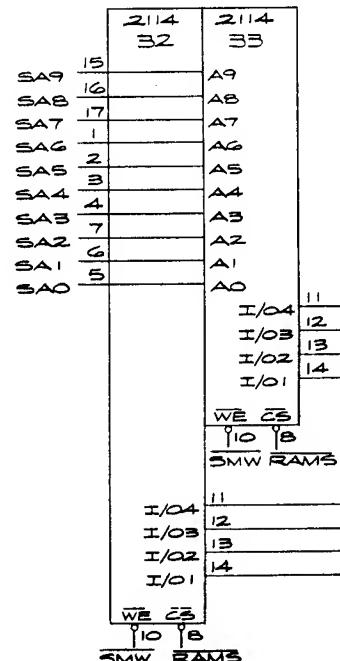
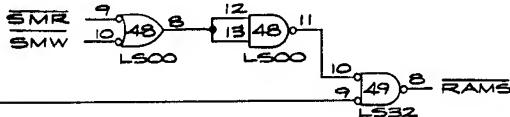
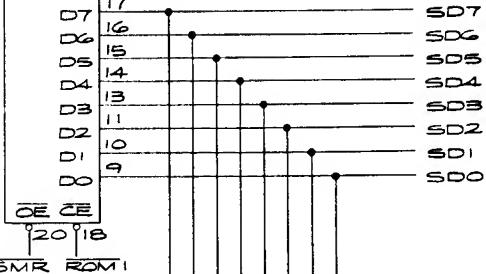
Inputs



RESET



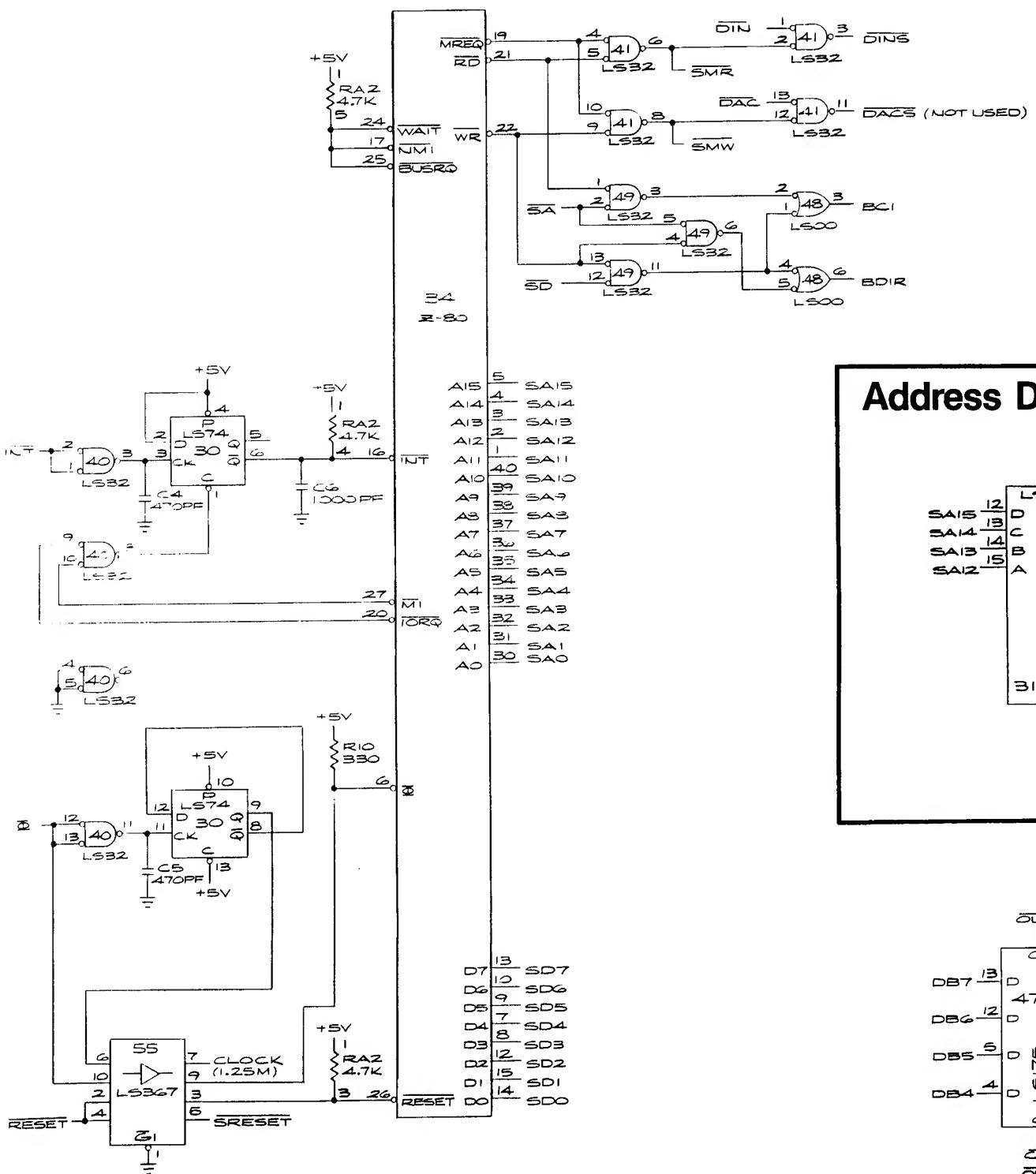
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SA11	21
SA10	19
SA9	22
SA8	23
SA7	1
SA6	7
SA5	2
SA4	4
SA3	3
SA2	5
SA1	6
SA0	7



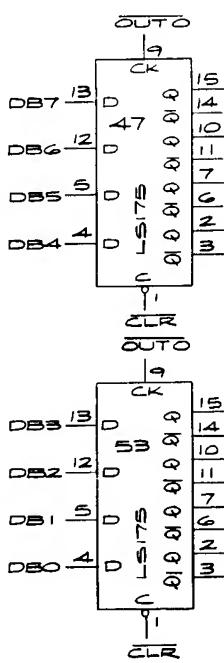
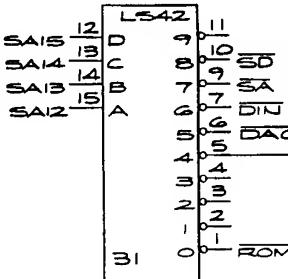
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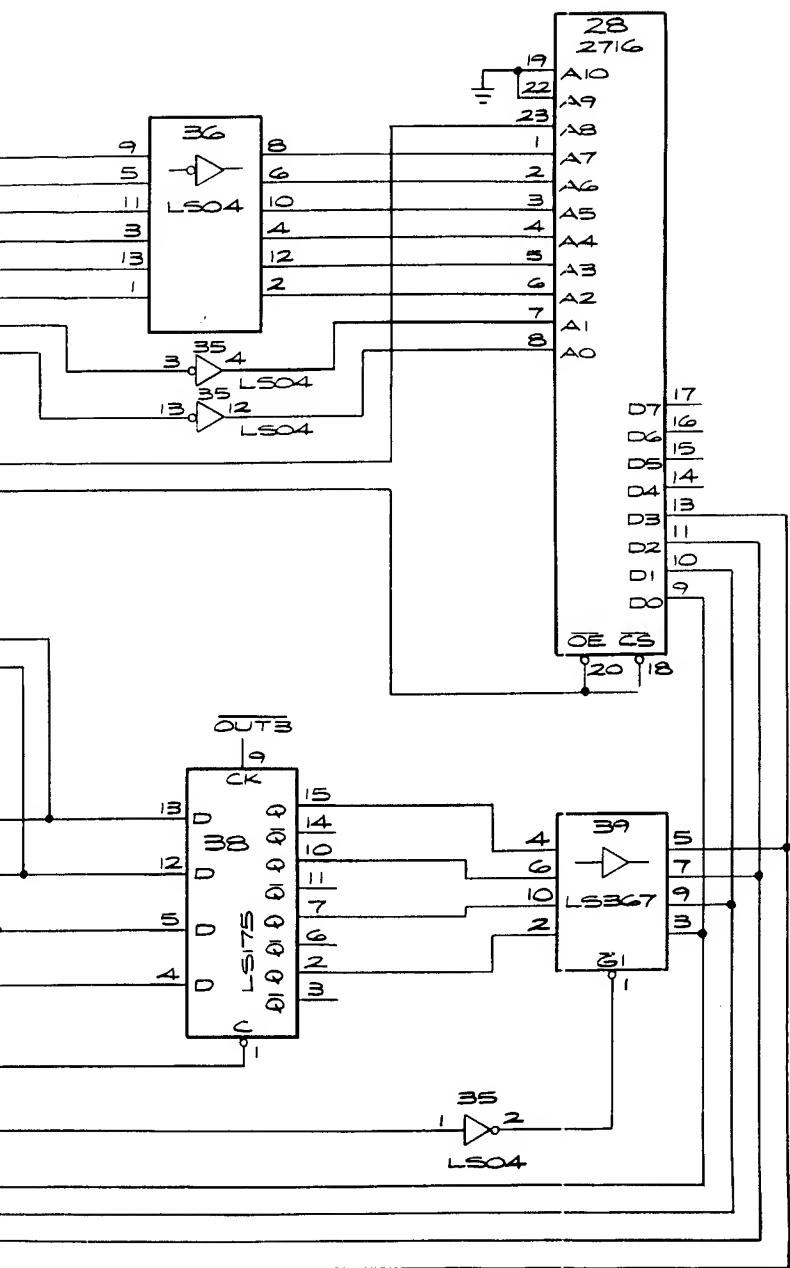
Kangaroo CPU PCB Schematic Diagram

Sound Microprocessor



Address Decoder

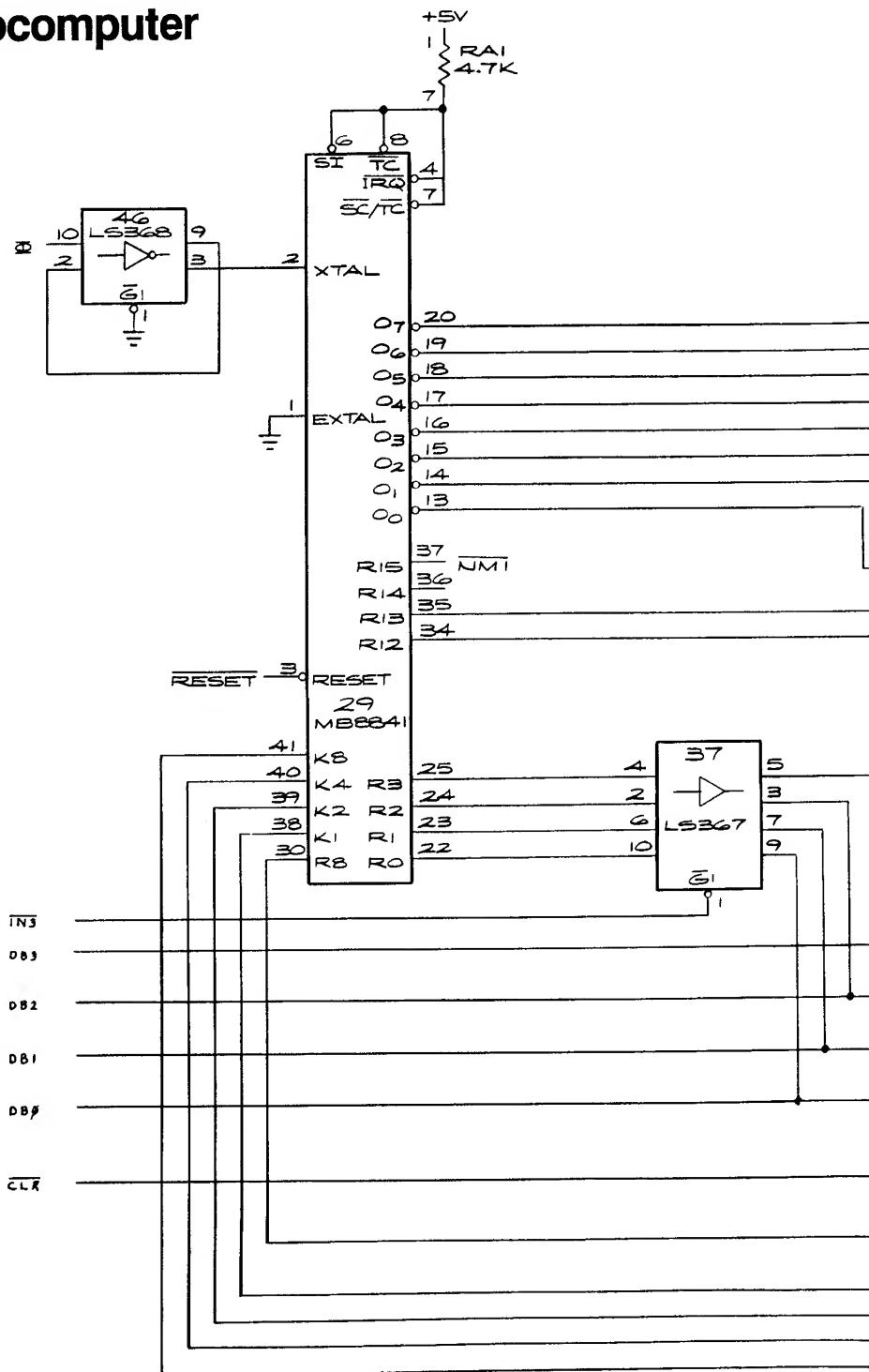


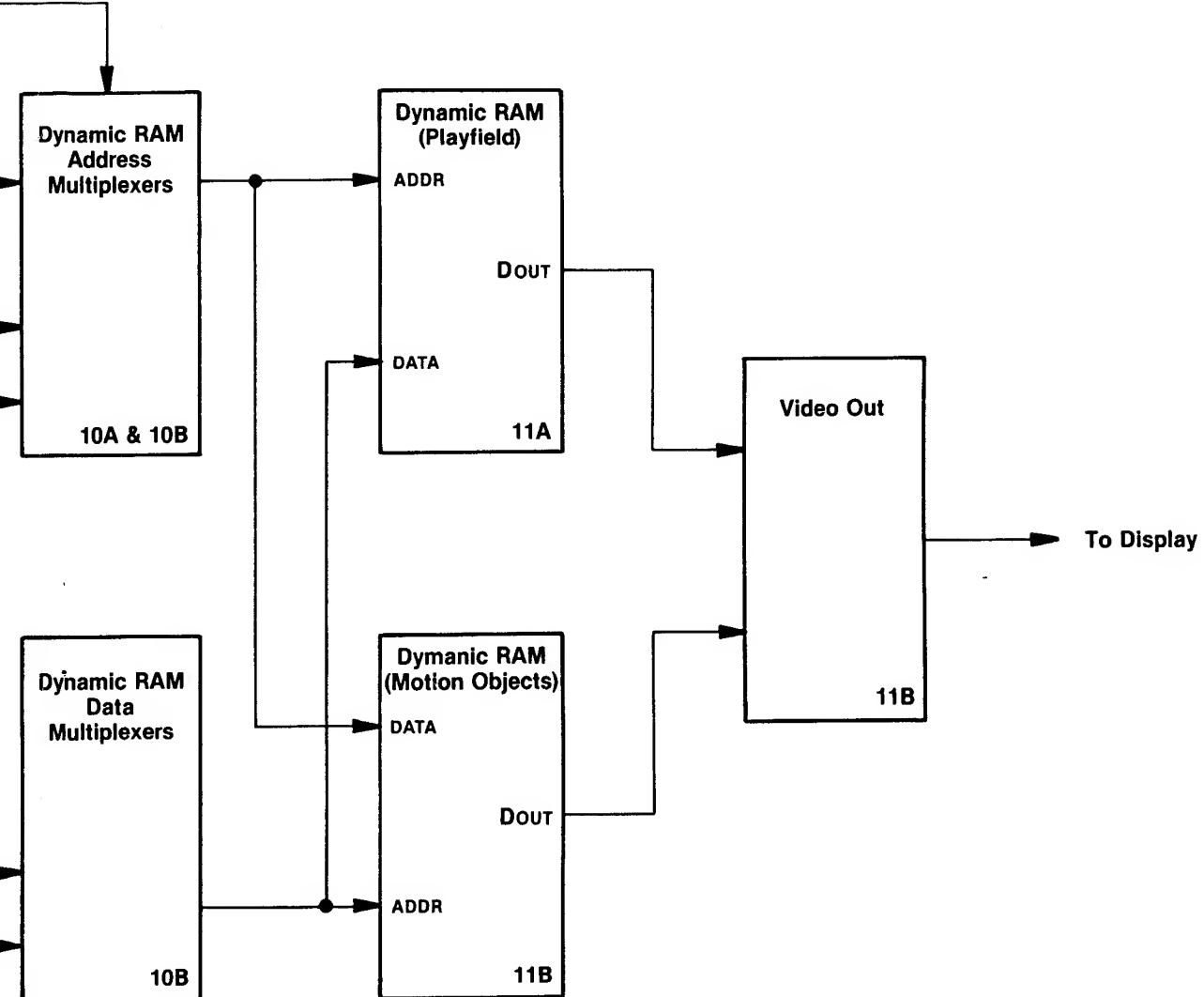


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Kangaroo CPU PCB Schematic Diagram

Custom Microcomputer

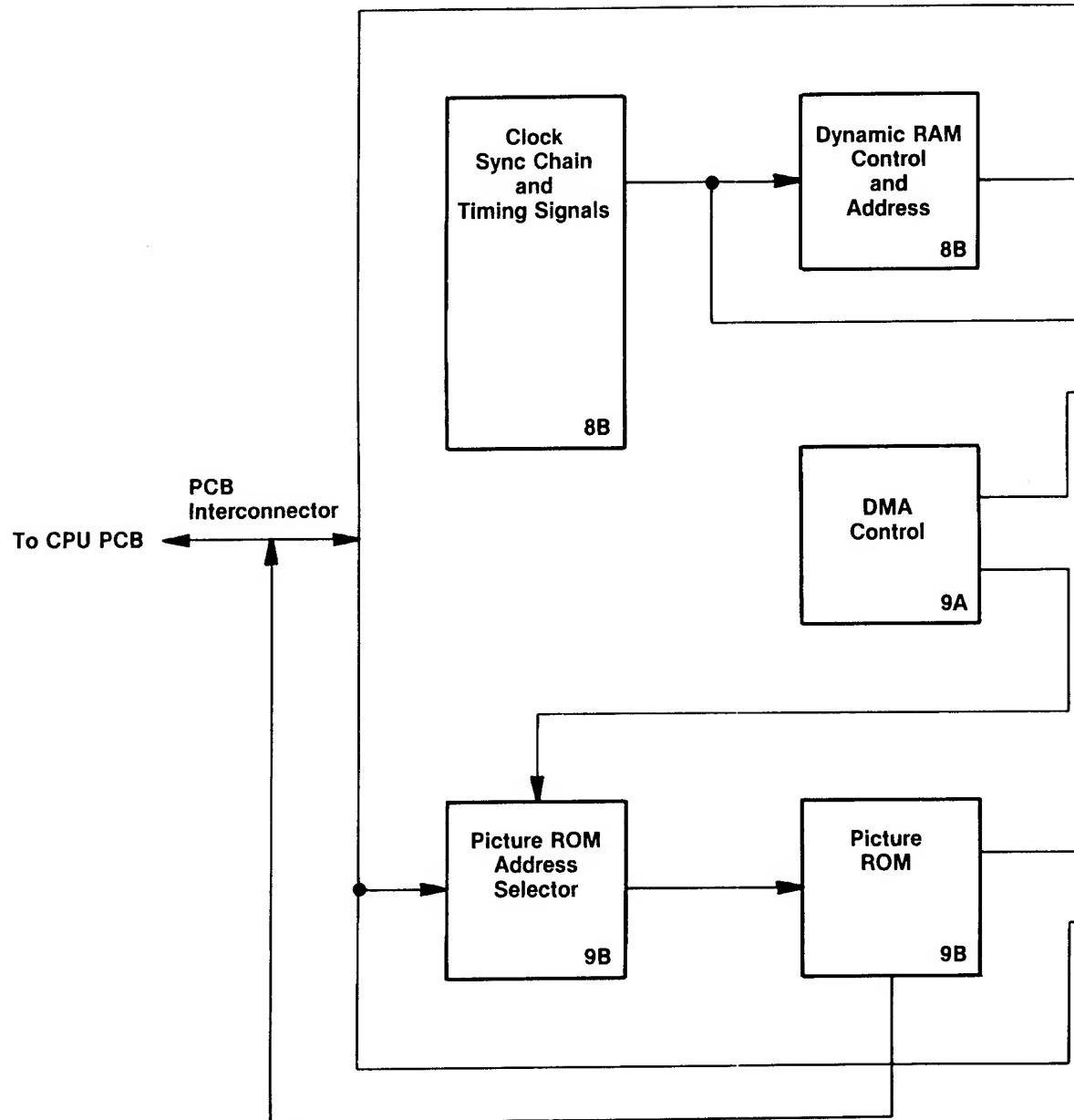




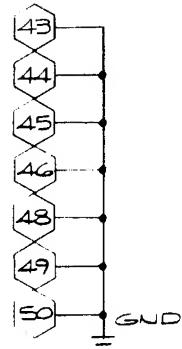
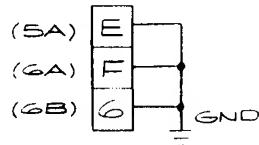
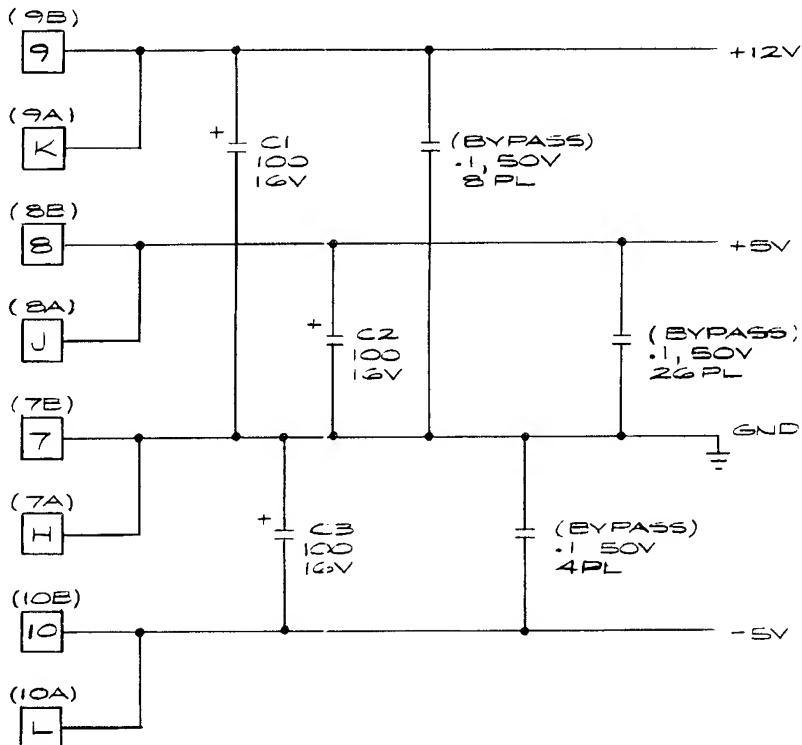
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Kangaroo Video PCB Schematic Diagram

Block Diagram (Video PCB)



Video Power Input



NOTES:

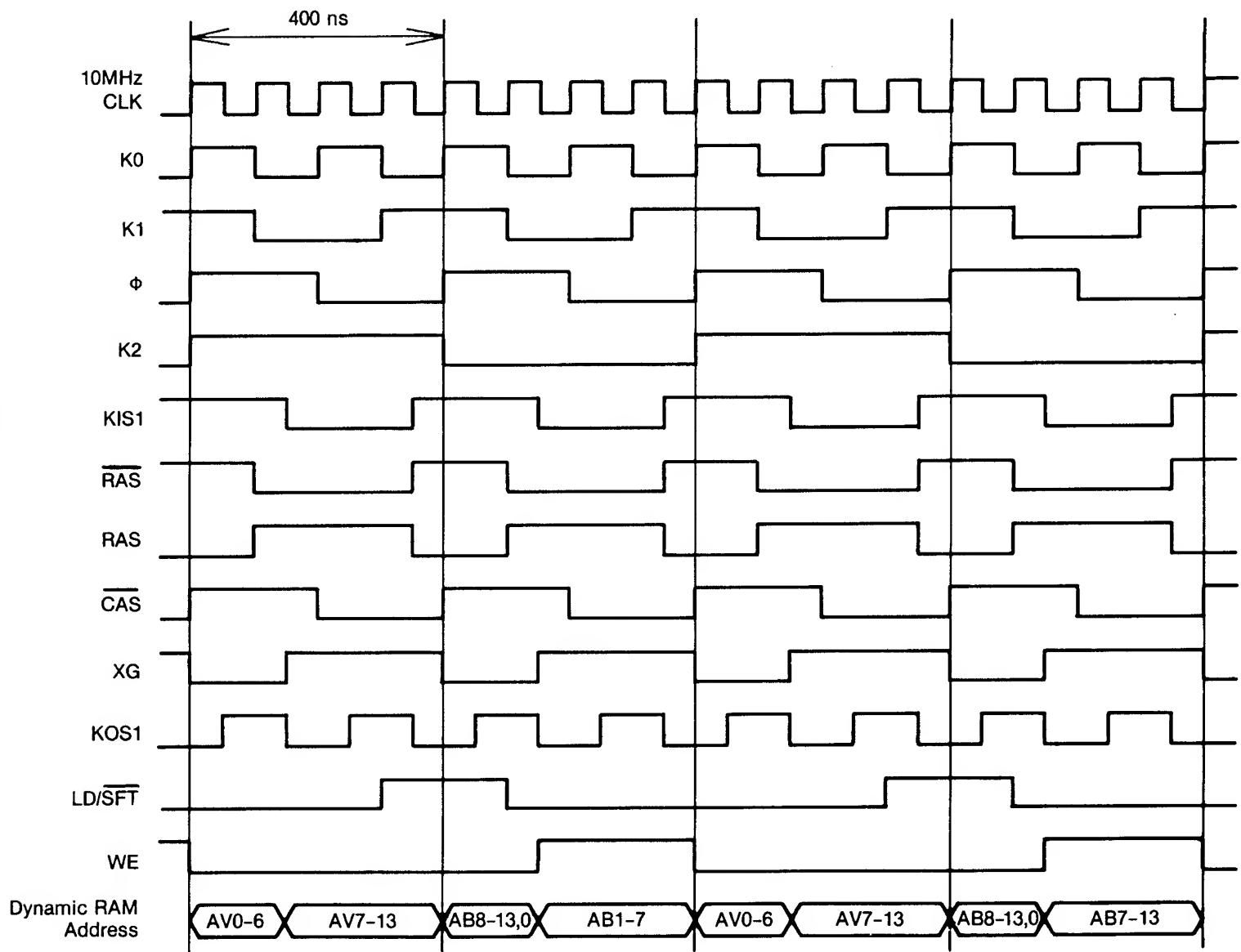
1. = CONNECTOR CN1
2. = CONNECTOR CN4



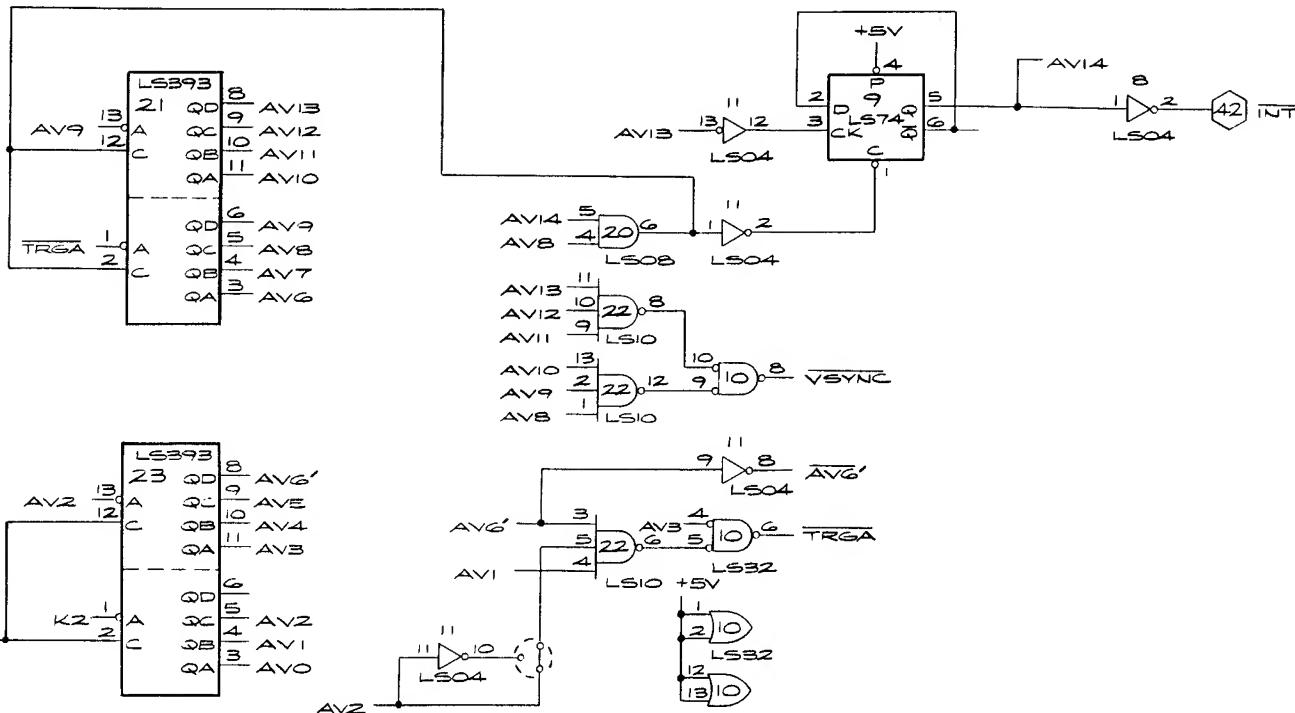
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Kangaroo Video PCB Schematic Diagram

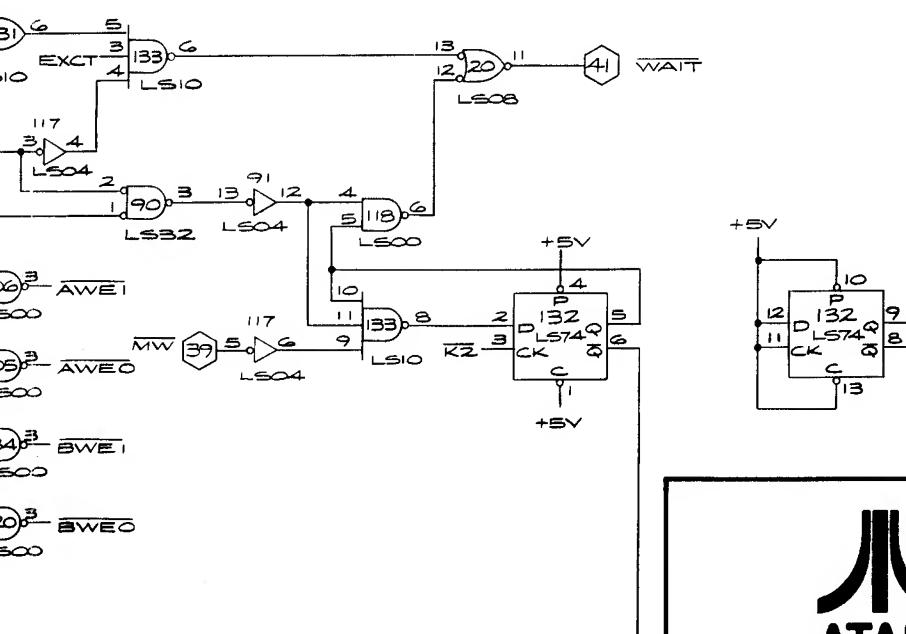
Dynamic RAM Timing Diagram (Video PCB)



Timing Signals



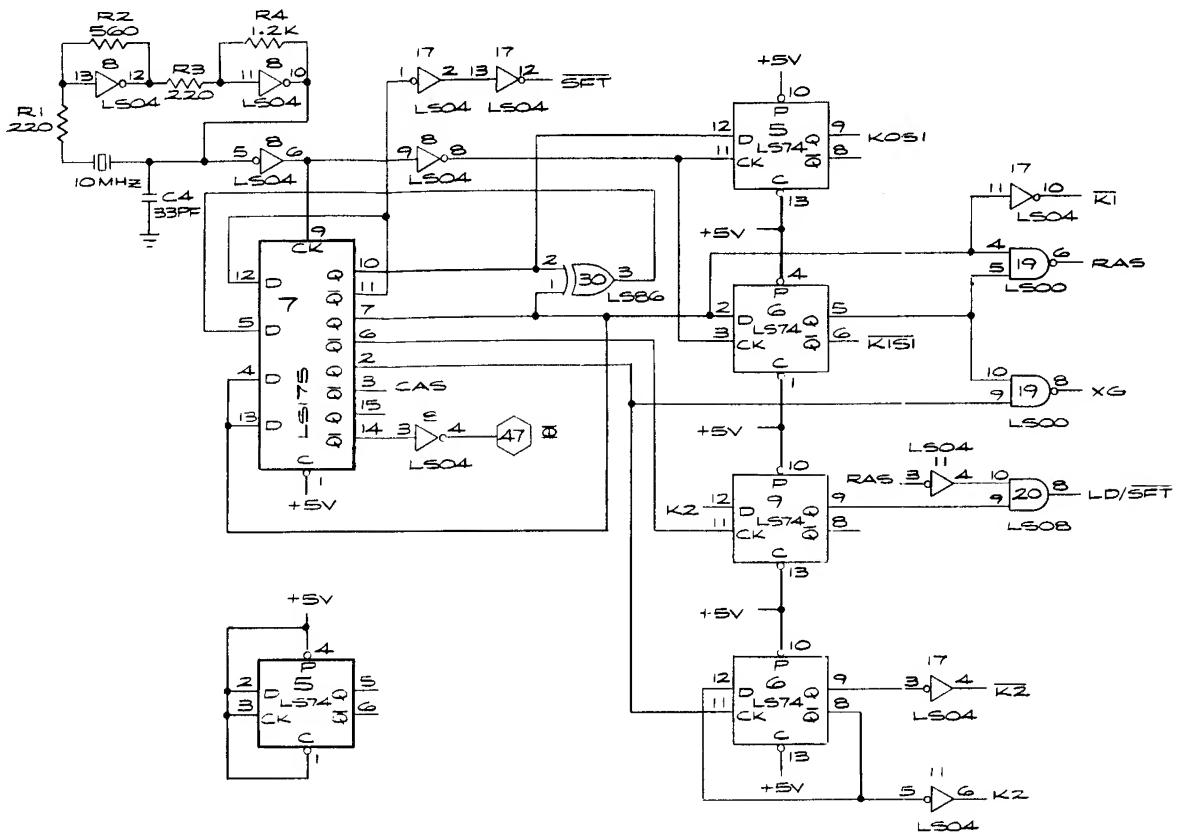
Address Decoding



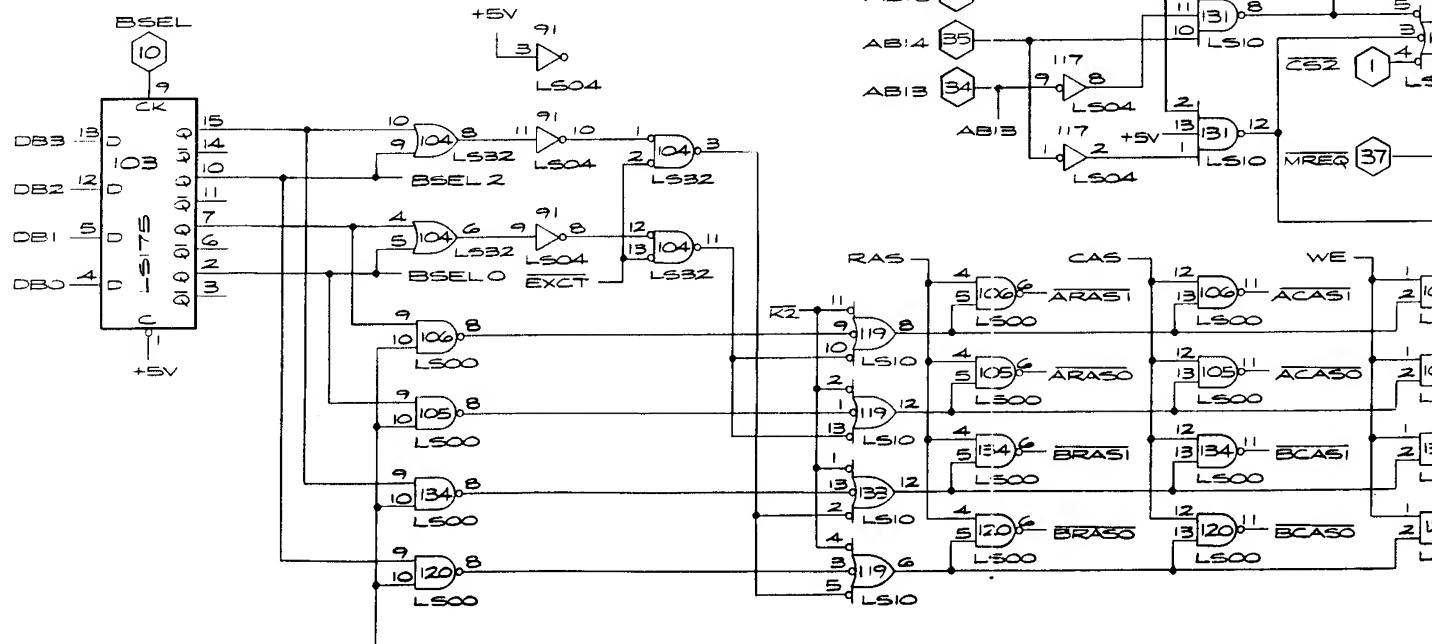
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Kangaroo Video PCB Schematic Diagram

Clock, Sync Chain, a



Dynamic RAM Control



Dynamic RAM Video Address and Flip

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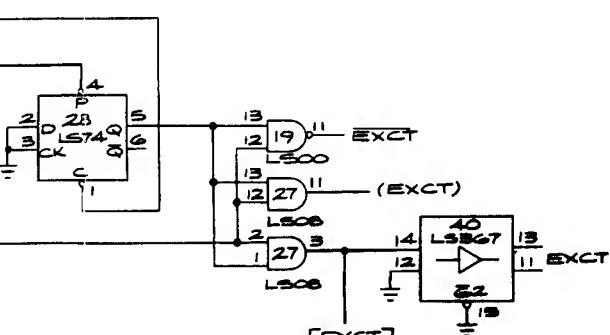
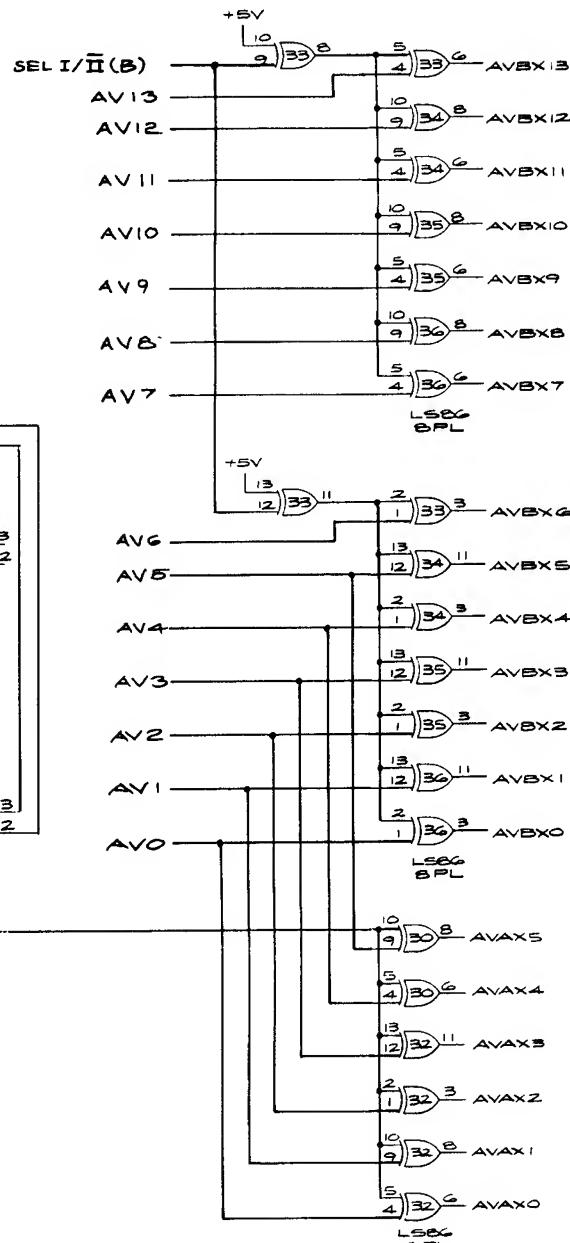
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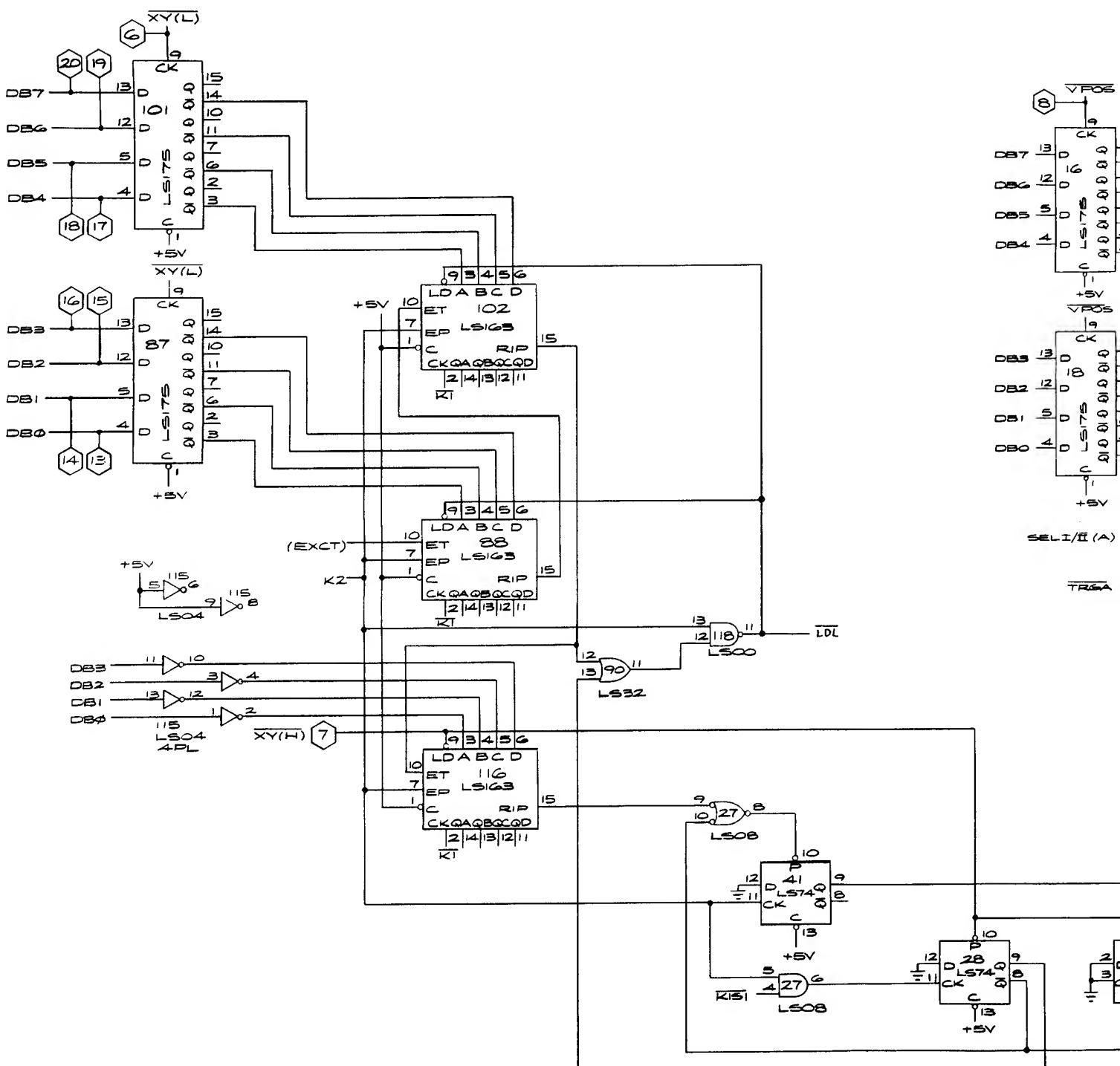
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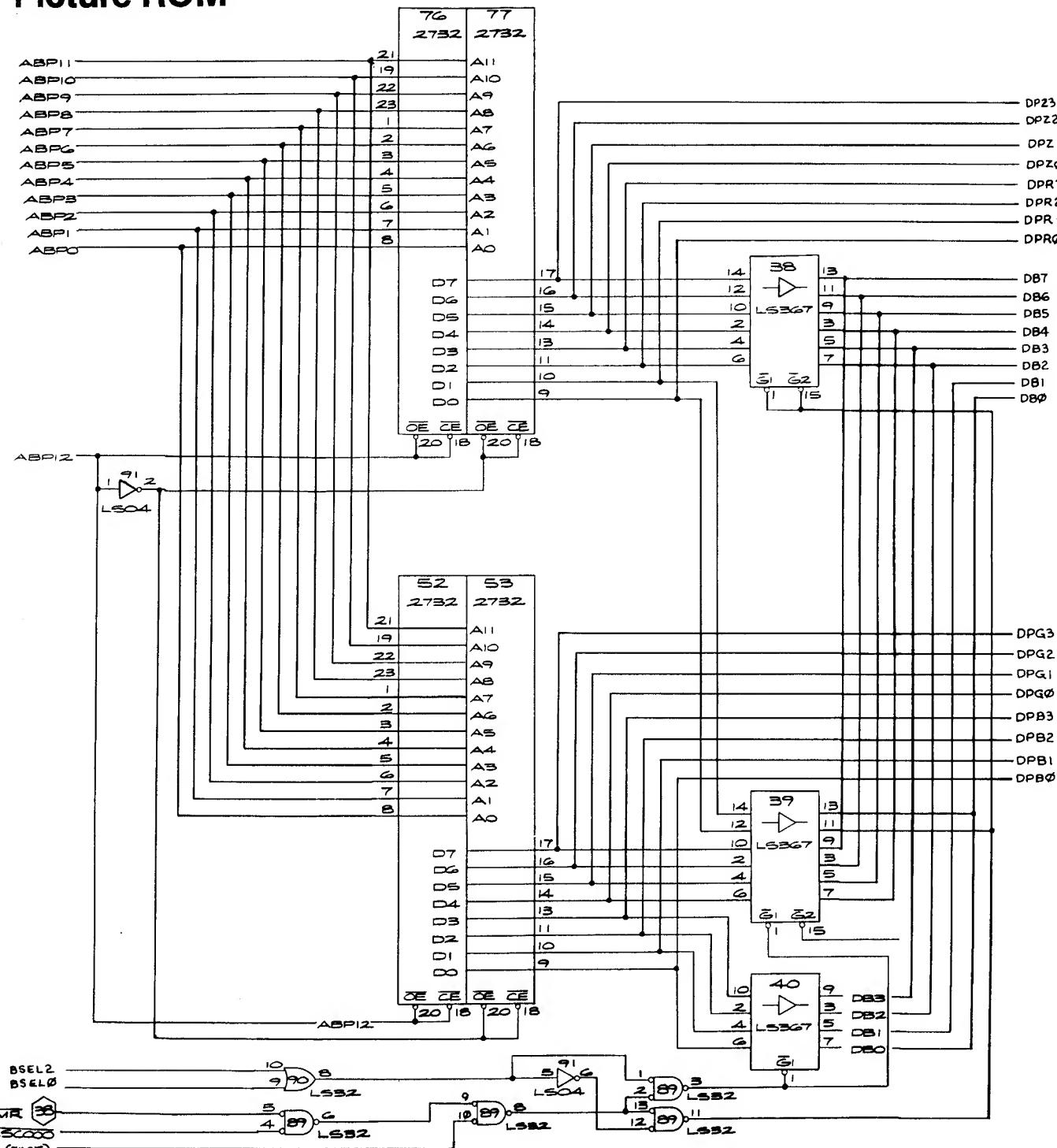
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Kangaroo Video PCB Schematic Diagram

DMA Control



Picture ROM

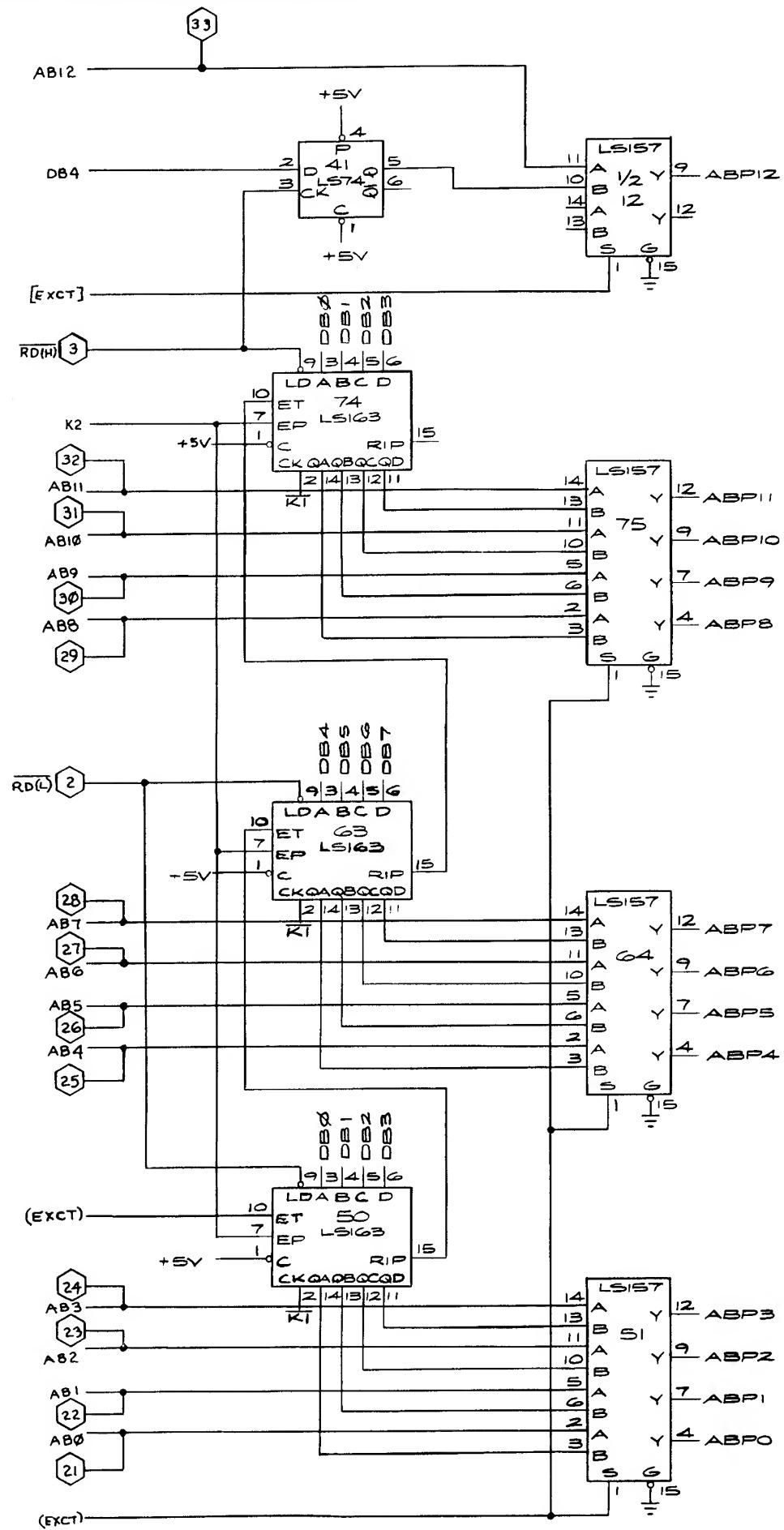


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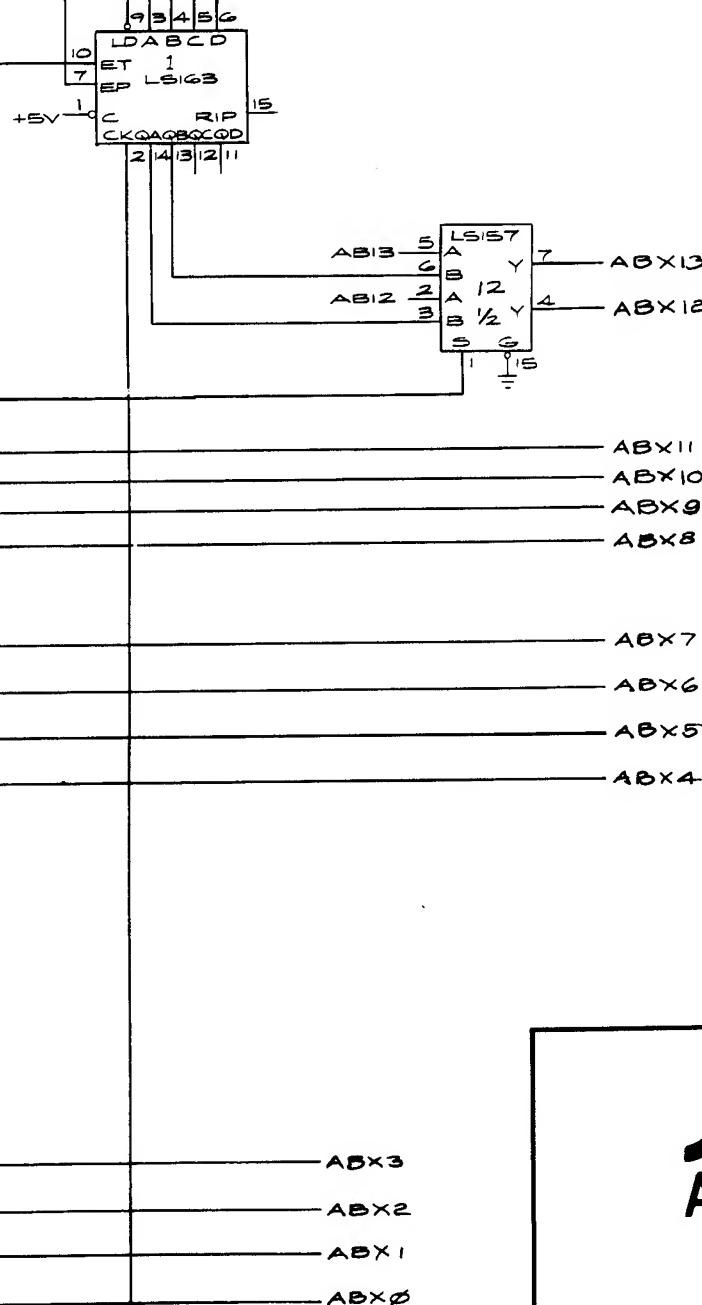


Kangaroo Video PCB Schematic Diagram

Picture ROM Address Selector

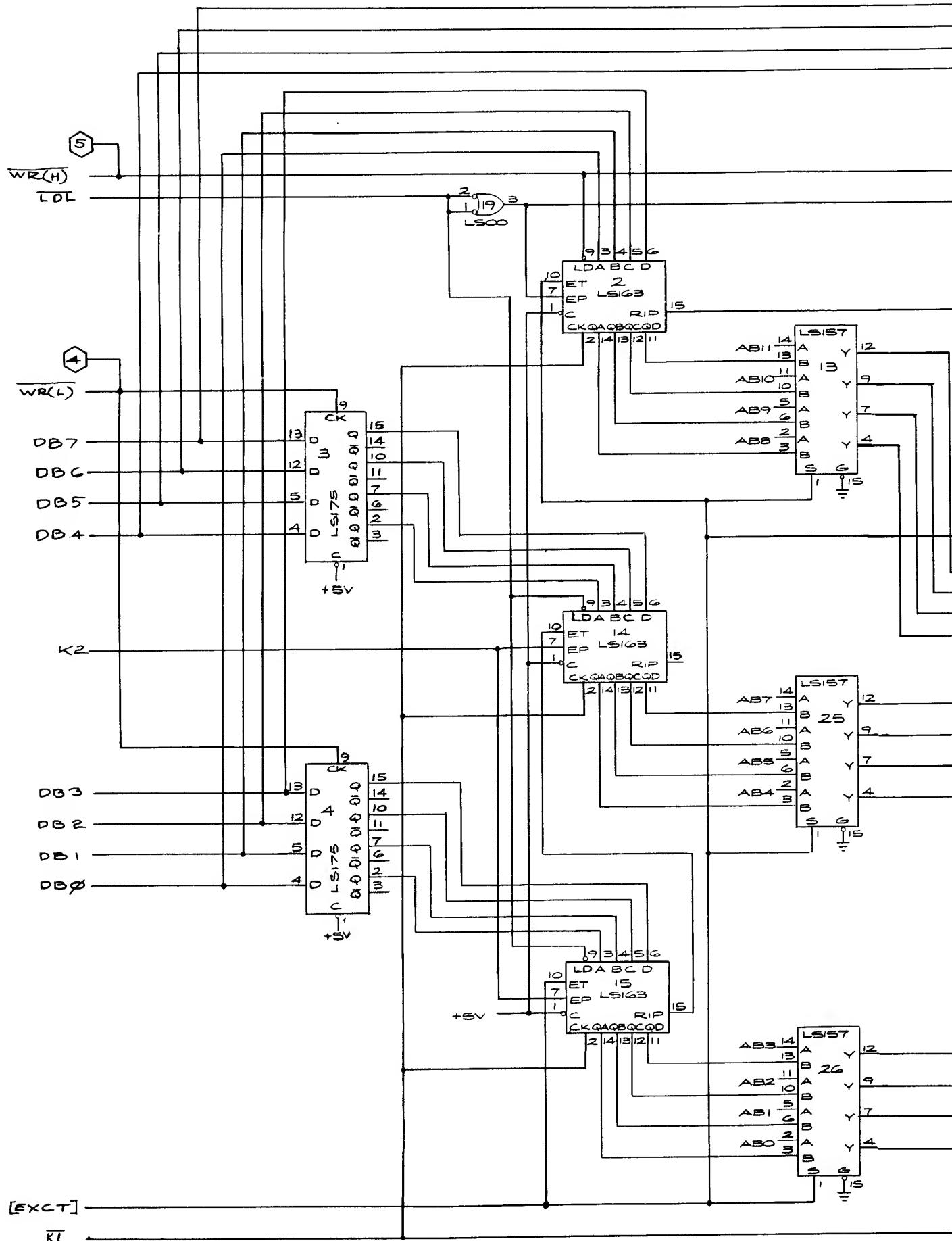


Dynamic RAM Address from CPU and for DMA

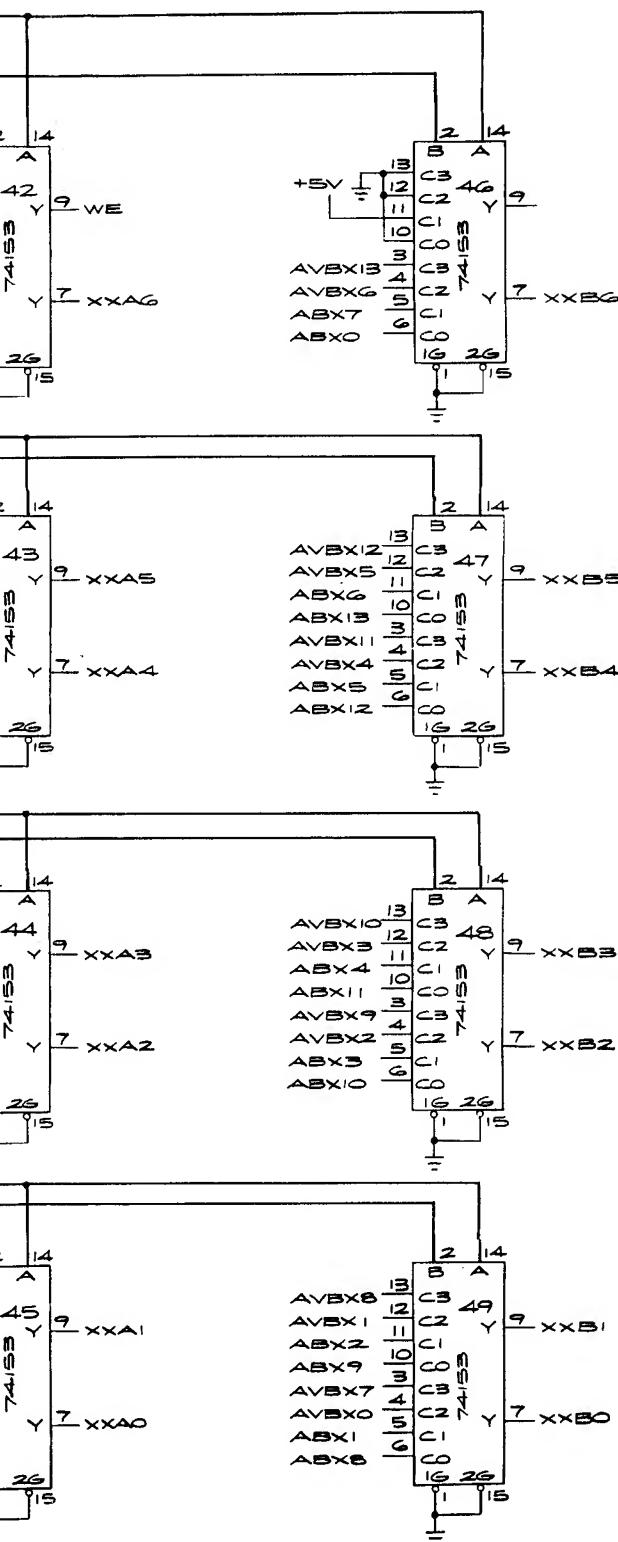


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Kangaroo Video PCB Schematic Diagram



Address Selector



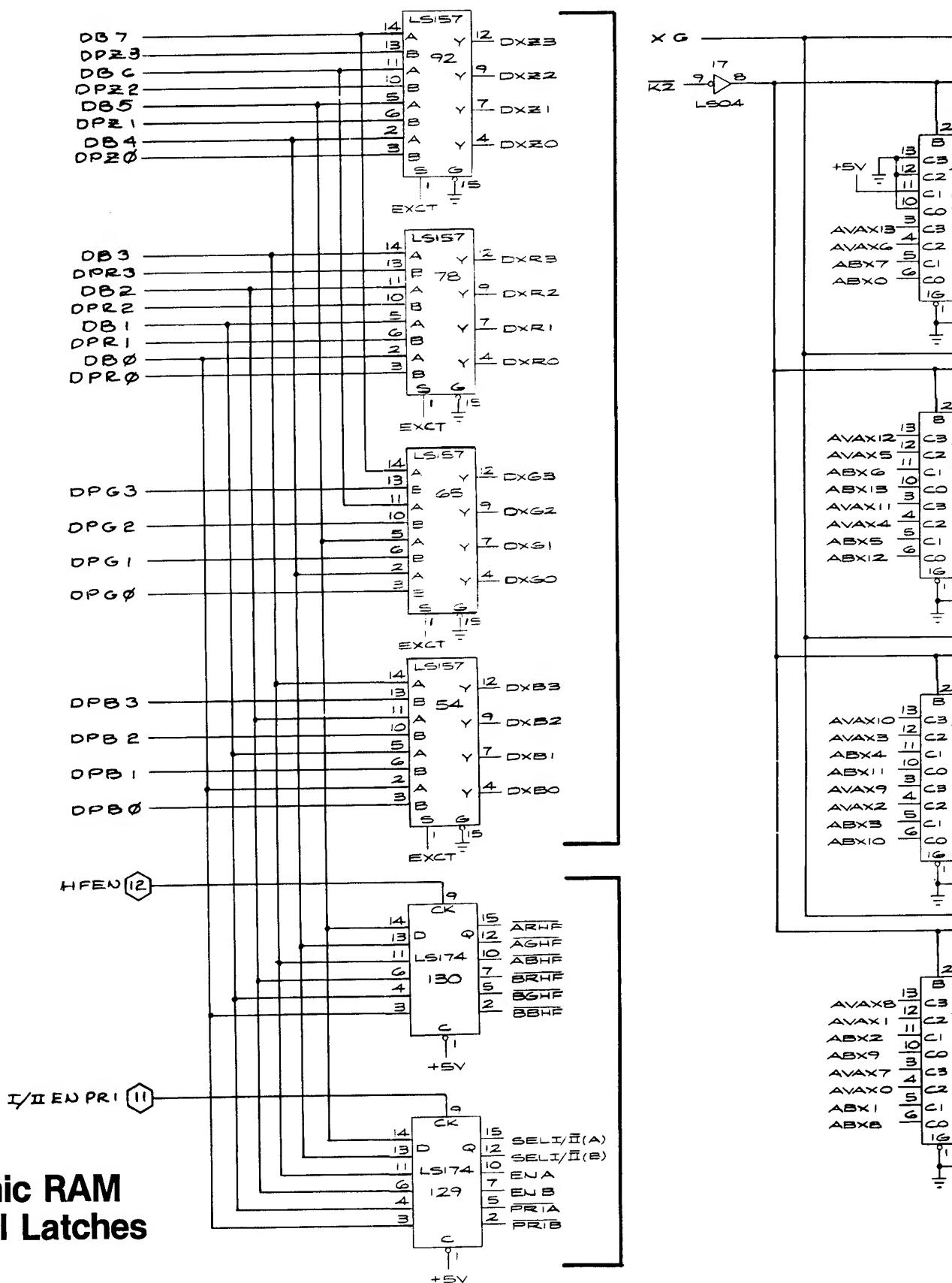
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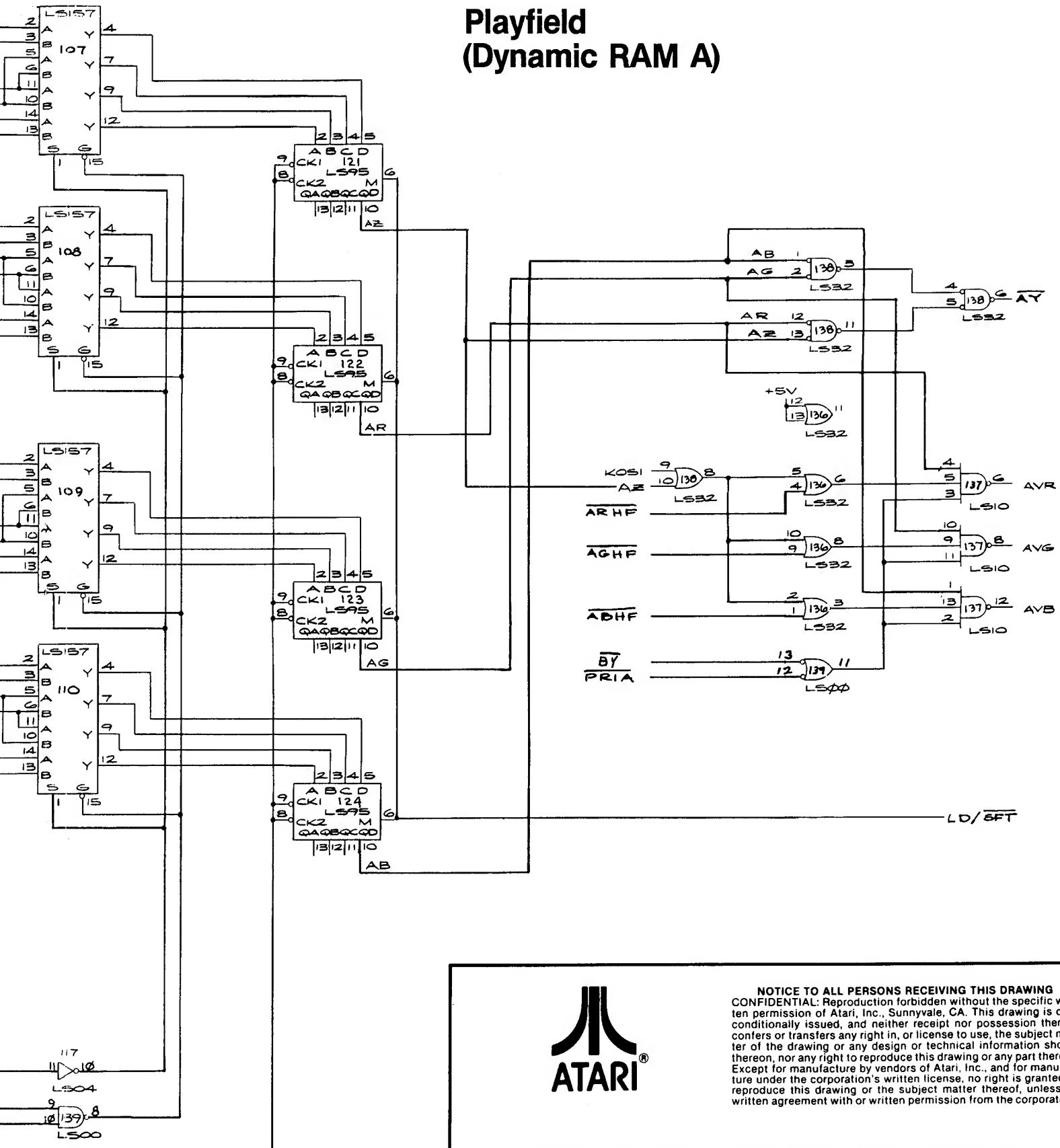
Kangaroo Video PCB Schematic Diagram

Dynamic RAM Data Selector

Dynamic RAM

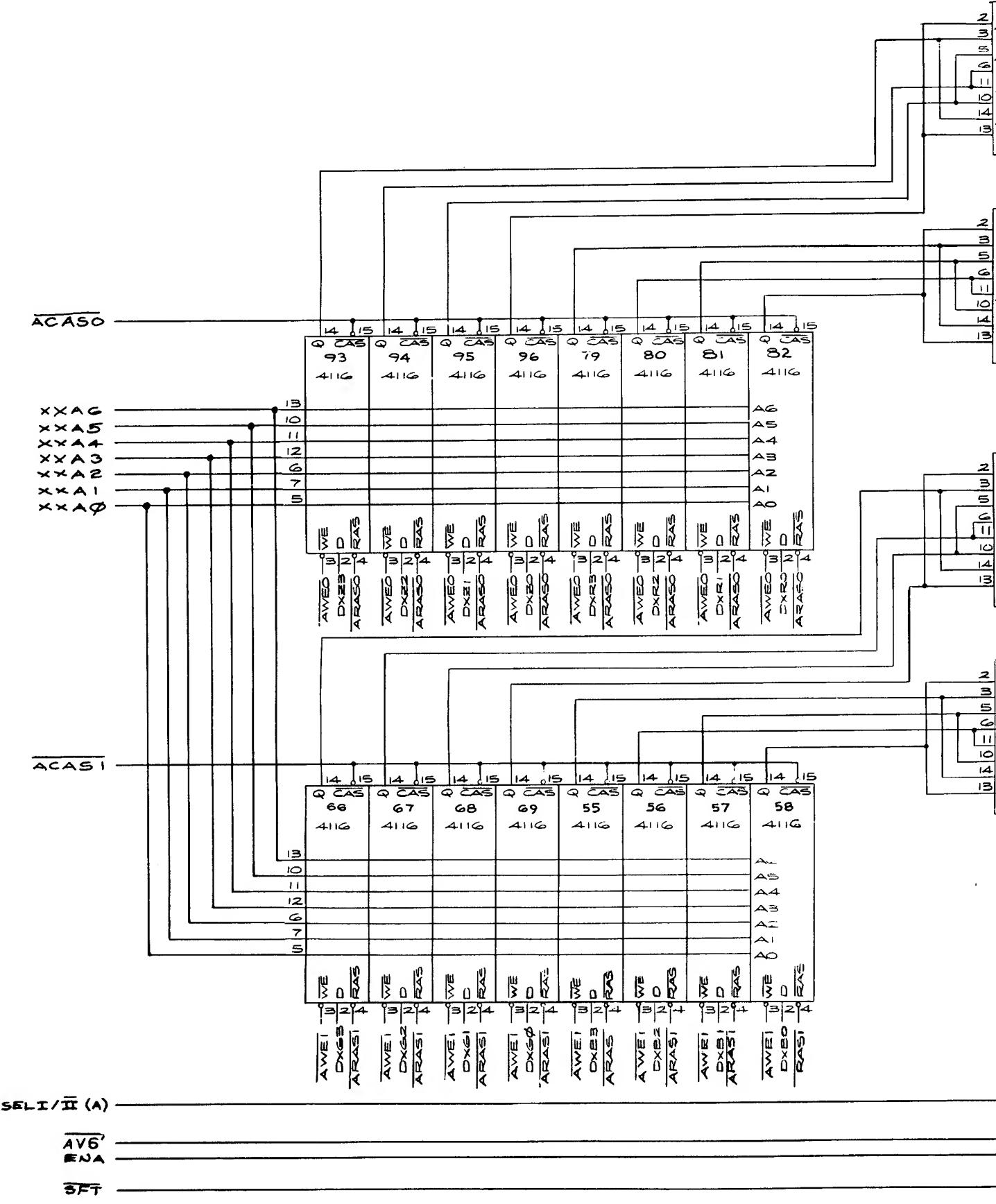


Playfield (Dynamic RAM A)

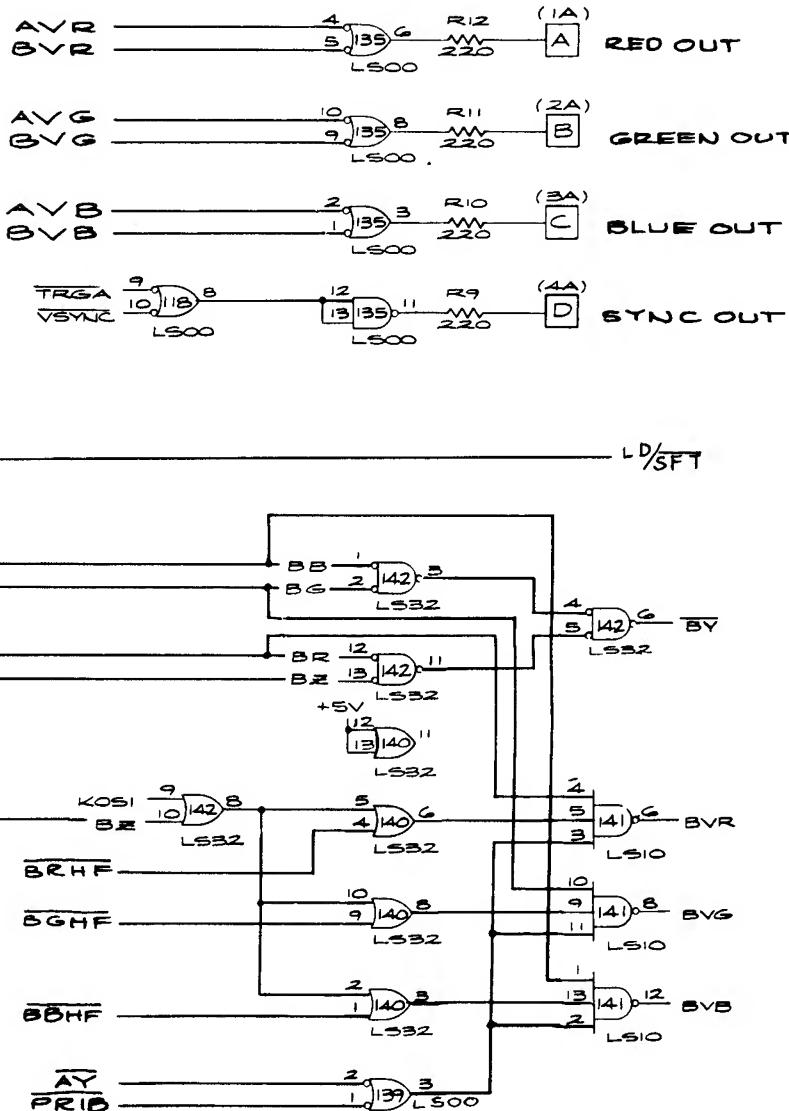
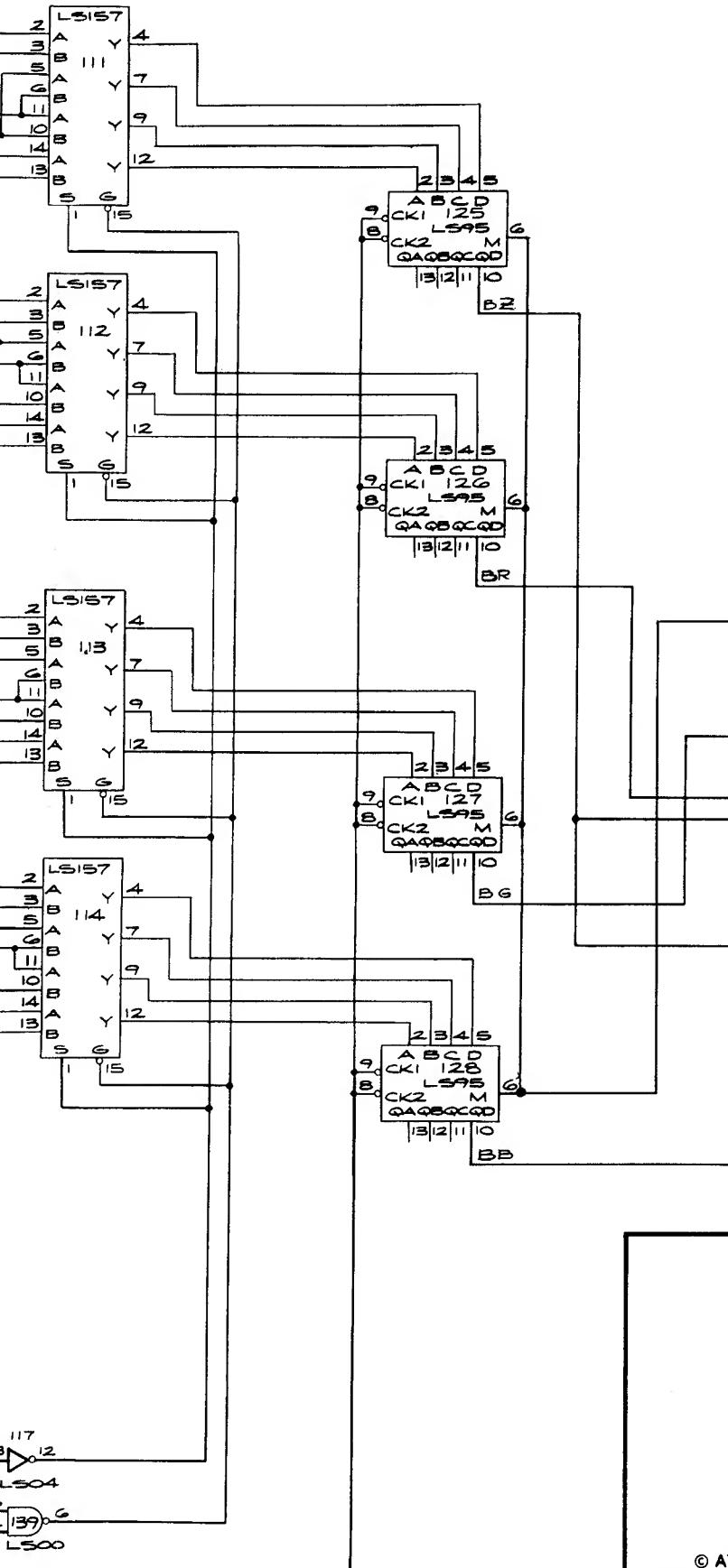


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Kangaroo Video PCB Schematic Diagram



Video Output



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Kangaroo Video PCB Schematic Diagram

Motion Object (Dynamic RAM B)

