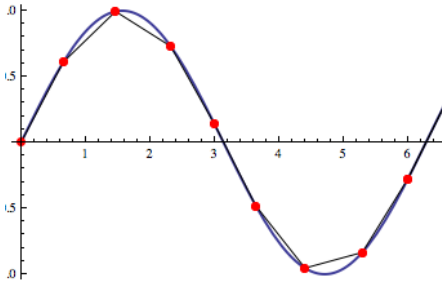
CASE STUDIES

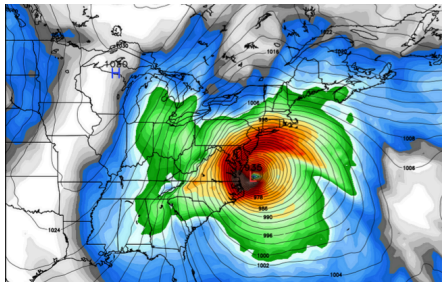
Reversible FFTs using posit arithmetic

16-bit posit has demonstrated higher accuracy and dynamic range, enabling forward reverse FFTs to perfectly restore the original signal. Posit-based FFTs are effectively lossless and eliminate the need for 32-bit floats.



Posit for weather and climate models

16-bit posit compared to 16-bit float presents the benefits on this study on weather and climate models of low and medium complexity (shallow water model). Posit arithmetic in Computational Fluid Dynamics (CFD) shows promising results for reduced-precision on geophysical fluid simulation.



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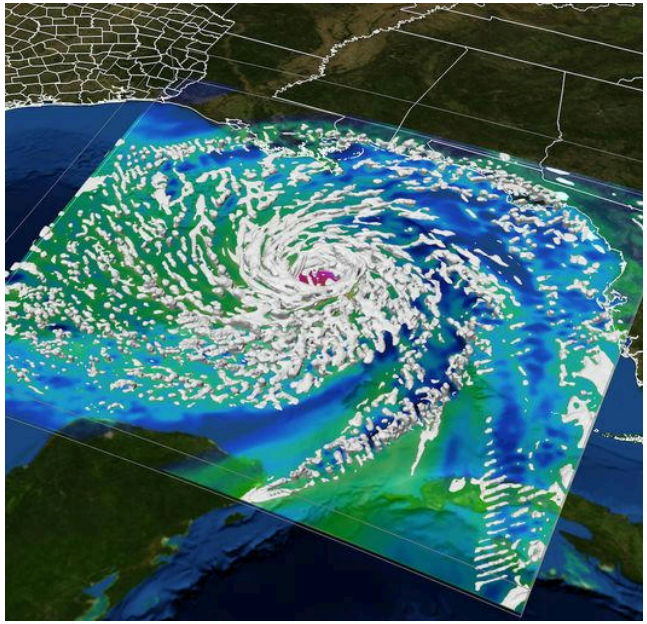


POSIT for HPC/HPDA

Going Beyond IEEE-754 FP64

Posit GPGPU implementation with
- Minimized error & memory size
- Cuda like API software

VIVIDSPARKS

E.M.G.2 TECHNOLOGIES INNOVANTES

WHO ARE WE ?

VividSparks Europe, a self-funded high-speed computing technology company, specializes in fabless semiconductors. We solve fundamental arithmetic circuit design problems with silicon-efficient, high-performance libraries and algorithms. Our goal is to deliver high performance with minimal power consumption, making novel, affordable technology accessible to everyone.

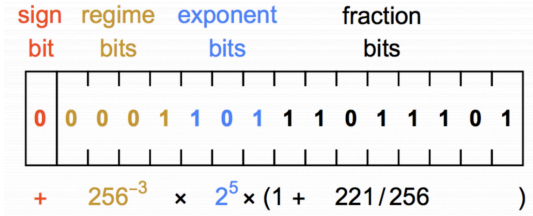
OUR PRODUCTS

VividSparks Europe proposes hardwares IP for all use cases: AI, Automotive, HPC or GPGPU. Our expertise enables us to build custom chips incorporating the Posit arithmetic format. From 16 to 512 cores, we can optimize the response to your needs.

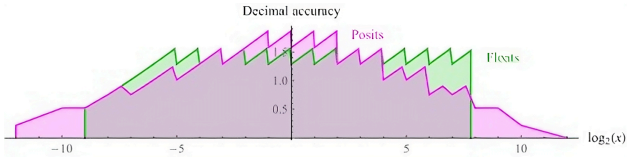
- **HPC: 64 posit-cores**
- **GPGPU: up to 512 posit-cores**
- **AI: 16 posit-cores**
- **Automotive: 32 posit-cores**

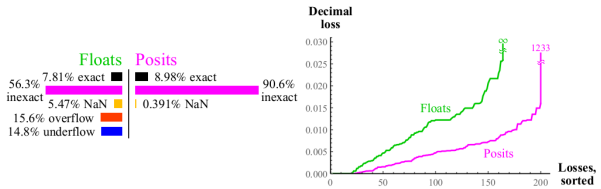
POSIT : WHAT AND WHY ?

- **More efficient** use of bits for representing real numbers
- Aims to **address the limitations** of IEEE-754 floating-point standard
- Dynamic range for regime and exponent bits



- **Higher precision** and **superior dynamic range** for the same bit length
- Tapered accuracy

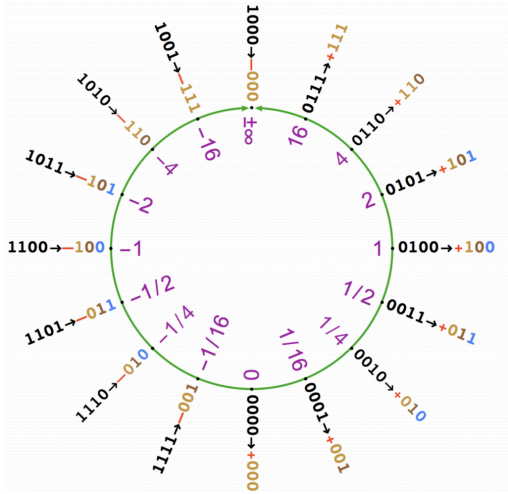




Quantitative comparison of floats and posits computing 2^x

Elimination of redundant representations

- **Reduced amount** of NaN
- **Just one** Infinite and Zero



Hardware and software implementations

- Hardware accelerators, implemented on FPGA
- CUDA-like sotware API
- C & C++ libraries

```
// Allocation on RacEr device
RacEr_mc_device_malloc (&device, size,
&a_device);
// Kernel enqueue and execute on RacEr
RacEr_mc_kernel_enqueue (&device, grid_dim,
tg_dim, "kernel_float_matrix_memcpy", 5,
kernel_args);
RacEr_mc_device_tile_groups_execute (&device);
```