TIMER

# 8-bit Timer/Counter0 with PWM

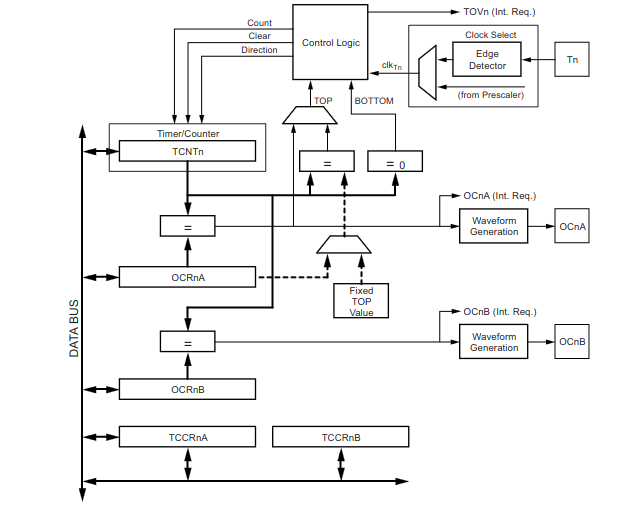
## Features

* Two independent output compare units;
* Double buffered output compare registers;
* Clear timer on compare match (auto reload);
* Glitch free, phase correct pulse width modulator (PWM);
* Variable PWM period;
* Frequency generator;
* Three independent interrupt sources (TOV0, OCF0A, and OCF0B).

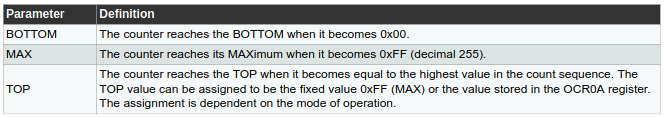
## Overview

Timer/Counter0 is a general purpose 8-bit Timer/Counter module, with two independent output compare units, and with PWM support. It allows accurate program execution timing (event management) and wave generation.

A simplified block diagram of the 8-bit Timer/Counter is shown in Figure 1.

**Figure 1. 8-bit Timer/Counter Block Diagram**

## Definitions

**Table 1. Definitions**

## Registers

* The Timer/Counter (TCNT0) and output compare registers (OCR0A and OCR0B) are 8-bit registers;
* Interrupt request (abbreviated to Int.Req.) signals are all visible in the timer interrupt flag register (TIFR0);
* All interrupts are individually masked with the timer interrupt mask register (TIMSK0).

About Timer/Counter:

* The Timer/Counter can be clocked internally, via the prescaler, or by an external clock source on the T0 pin;
* The clock select logic block controls which clock source and edge the Timer/Counter uses to increment (or decrement) its value;
* The Timer/Counter is inactive when no clock source is selected;
* The output from the clock select logic is referred to as the timer clock (clkT0).

About OCR0A and OCR0B:

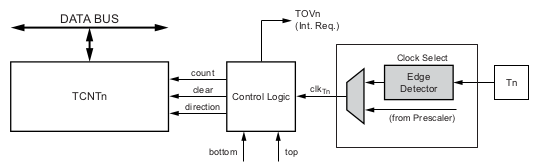
* The double buffered output compare registers (OCR0A and OCR0B) are compared with the Timer/Counter value at all times. The result of the compare can be used by the waveform generator to generate a PWM or variable frequency output on the output compare pins (OC0A and OC0B);
* The compare match event will also set the compare flag (OCF0A or OCF0B) which can be used to generate an output compare interrupt request.

## Timer/Counter Clock Source

* The Timer/Counter can be clocked by an internal or an external clock source;
* The clock source is selected by the clock select logic which is controlled by the clock select (CS02:0) bits located in the Timer/Counter control register (TCCR0B).

## Counter Unit

* Counter Unit Block Diagram

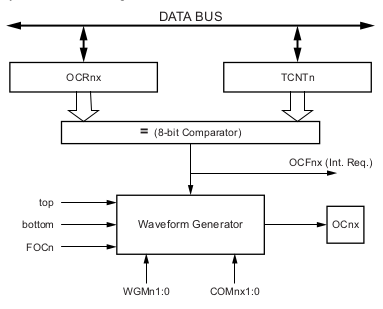


Some signal description:

* count: Increment or decrement TCNT0 by 1;
* direction: Select between increment and decrement;
* clear: Clear TCNT0 (set all bits to zero);
* The counting sequence is determined by the setting of the WGM01 and WGM00 bits located in the Timer/Counter control register (TCCR0A) and the WGM02 bit located in the Timer/Counter control register B (TCCR0B). There are close connections between how the counter behaves (counts) and how waveforms are generated on the output compare outputs OC0A and OC0B;
* The Timer/Counter overflow flag (TOV0) is set according to the mode of operation selected by the WGM02:0 bits.

## Output Compare Unit

* The 8-bit comparator continuously compares TCNT0 with the output compare registers (OCR0A and OCR0B). Whenever TCNT0 equals OCR0A or OCR0B, the comparator signals a match. A match will set the output compare flag (OCF0A or OCF0B) at the next timer clock cycle. If the corresponding interrupt is enabled, the output compare flag generates an output compare interrupt. The output compare flag is automatically cleared when the interrupt is executed.
* The waveform generator uses the match signal to generate an output according to operating mode set by the WGM02:0 bits and compare output mode (COM0x1:0) bits. The max and bottom signals are used by the waveform generator for handling the special cases of the extreme values in some modes of operation.
* Output Compare Unit, Block Diagram:



* The OCR0x registers are double buffered when using any of the pulse width modulation (PWM) modes. For the normal and clear timer on compare (CTC) modes of operation, the double buffering is disabled. The double buffering synchronizes the update of the OCR0x compare registers to either top or bottom of the counting sequence. The synchronization prevents the occurrence of odd-length, non-symmetrical PWM pulses, thereby making the output glitch-free.

### Force Output Compare:

* In non-PWM waveform generation modes, the match output of the comparator can be forced by writing a one to the force output compare (FOC0x) bit. Forcing compare match will not set the OCF0x flag or reload/clear the timer, but the OC0x pin will be updated as if a real compare match had occurred (the COM0x1:0 bits settings define whether the OC0x pin is set, cleared or toggled).

### Compare Match Blocking by TCNT0 Write

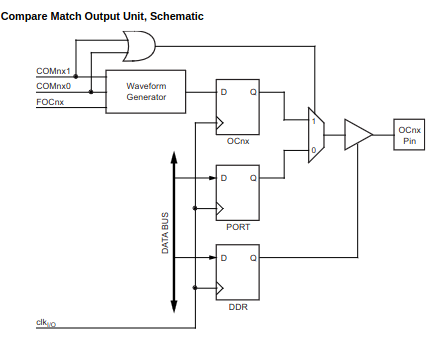
* All CPU write operations to the TCNT0 register will block any compare match that occur in the next timer clock cycle, even when the timer is stopped. This feature allows OCR0x to be initialized to the same value as TCNT0 without triggering an interrupt when the Timer/Counter clock is enabled.

### Using Output Compare Unit

* Since writing TCNT0 in any mode of operation will block all compare matches for one timer clock cycle, there are risks involved when changing TCNT0 when using the output compare unit, independently of whether the Timer/Counter is running or not. If the value written to TCNT0 equals the OCR0x value, the compare match will be missed, resulting in incorrect waveform generation. Similarly, do not write the TCNT0 value equal to BOTTOM when the counter is down counting.
* The setup of the OC0x should be performed before setting the data direction register for the port pin to output. The easiest way of setting the OC0x value is to use the force output compare (FOC0x) strobe bits in normal mode. The OC0x registers keep their values even when changing between waveform generation modes.
* Be aware that the COM0x1:0 bits are not double buffered together with the compare value. Changing the COM0x1:0 bits will take effect immediately.

## Compare Match Output Unit

* The compare output mode (COM0x1:0) bits have two functions. The waveform generator uses the COM0x1:0 bits for defining the output compare (OC0x) state at the next compare match. Also, the COM0x1:0 bits control the OC0x pin output source.
* The figure below shows a simplified schematic of the logic affected by the COM0x1:0 bit setting. The I/O registers, I/O bits, and I/O pins in the figure are shown in bold. Only the parts of the general I/O port control registers (DDR and PORT) that are affected by the COM0x1:0 bits are shown.



* The general I/O port function is overridden by the output compare (OC0x) from the waveform generator if either of the COM0x1:0 bits are set. However, the OC0x pin direction (input or output) is still controlled by the data direction register (DDR) for the port pin. The data direction register bit for the OC0x pin (DDR\_OC0x) must be set as output before the OC0x value is visible on the pin. The port override function is independent of the waveform generation mode.

### Compare Output Mode and Waveform Generation

* The waveform generator uses the COM0x1:0 bits differently in normal, CTC, and PWM modes.
* For all modes, setting the COM0x1:0 = 0 tells the waveform generator that no action on the OC0x register is to be performed on the next compare match.
* A change of the COM0x1:0 bits state will have effect at the first compare match after the bits are written.
* For non-PWM modes, the action can be forced to have immediate effect by using the FOC0x strobe bits.

## Modes of Operation

* The mode of operation, i.e., the behavior of the Timer/Counter and the output compare pins, is defined by the combination of the waveform generation mode (WGM02:0) and compare output mode (COM0x1:0) bits.
* The compare output mode bits do not affect the counting sequence, while the waveform generation mode bits do.
* The COM0x1:0 bits control whether the PWM output generated should be inverted or not (inverted or non-inverted PWM).
* . For non-PWM modes the COM0x1:0 bits control whether the output should be set, cleared, or toggled at a compare match.

### Normal mode

* The simplest mode of operation is the normal mode (WGM02:0 = 0). In this mode the counting direction is always up (incrementing), and no counter clear is performed.
* The counter simply overruns when it passes its maximum 8-bit value (TOP = 0xFF) and then restarts from the bottom (0x00).
* In normal operation the Timer/Counter overflow flag (TOV0) will be set in the same timer clock cycle as the TCNT0 becomes zero. The TOV0 Flag in this case behaves like a ninth bit, except that it is only set, not cleared. However, combined with the timer overflow interrupt that automatically clears the TOV0 flag, the timer resolution can be increased by software.