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CECS 361 Section 01
Lab 2
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1 Introduction

The purpose of this lab is to implement a synchronous satisfiability checker for a number of given Boolean functions. Satisfiability refers to the problem of finding out whether or not a result of 1 can be achieved using all inputs. While satisfiability can be a complex problem to solve, especially with functions with many inputs, our functions only took 3 inputs, which means that there are only $2^3 = 8$ possibilities that need to be checked for satisfiability, which can be solved in less than a microsecond.

As stated earlier, the four functions that needed to be checked for satisfiability were given inside a Verilog module. Any given function's inputs are driven by another module, which was half-written. A top-level module connects both modules, and is then implemented on the Nexys A7 board running an Artix 7 FPGA. On the board, several LEDs light up displaying the status of satisfiability of the current function selected.

2 Implementation

The four functions to test were given in a file named `CNF.v`. It has three inputs, and a two-bit select input, which it uses to mux through the four functions.

Its output is sent to the module which drives its inputs, named `Solver.v`. This module was partially completed. Its function is to iterate through the numbers 0 through 7 in binary, sending the value to `CNF.v`'s inputs. If it detects a 1 from `CNF.v`, it will stop iterating through numbers, set the RGB LED to green, and set the simple LEDs to display the solution of the function—otherwise, the module will keep iterating numbers (infinitely), the RGB LED will stay red, and the simple LEDs will stay off.

The top-level module, named `top_level_mod.v`, connects the previous two modules. It is also the module that interfaces to the board through the constraints file `NexysA7-100T-Lab2.xdc`, which was given. Two switches are used for the mux (`CNF.v`), and one for the reset (`Solver.v`). The rightmost three basic LEDs are used for displaying the value that satisfies the current function, and the on-board RGB LED displays green if the function is indeed satisfiable and red if the function is unsatisfiable.

3 Testing and Verification

Testing was performed for both the `Solver.v` and `top_level_mod.v` modules.

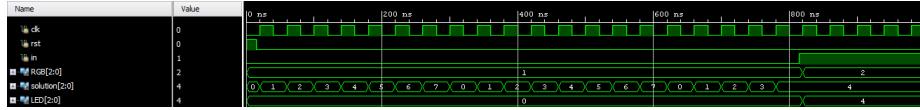


Figure 1: Waveform output of `Solver.v`.

Figure 1 shows the waveform for `Solver.v`. Its function is to loop through the numbers 0 to 7 and back again until it detects a 1 from its input `in`. When it does, it stops looping and sets the output `LED` to the value it found a 1 for. Additionally, the output `RGB` goes from 1 (representing red) to 2 (representing green).

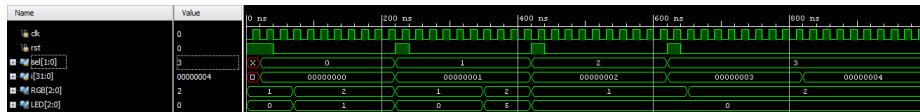


Figure 2: Waveform output of `top_level_mod.vv`

Figure 2 shows the waveform for `top_level_mod.v`. Just as before, an easy indicator to see whether a function has been satisfied is the `RGB` output: 1 means “no”, and 2 means “yes”. All functions are indeed satisfiable except Function 2 (where `sel` is 2).

Below are pictures of all four functions. Note that Function 2 is unsatisfiable and therefore its light is red.

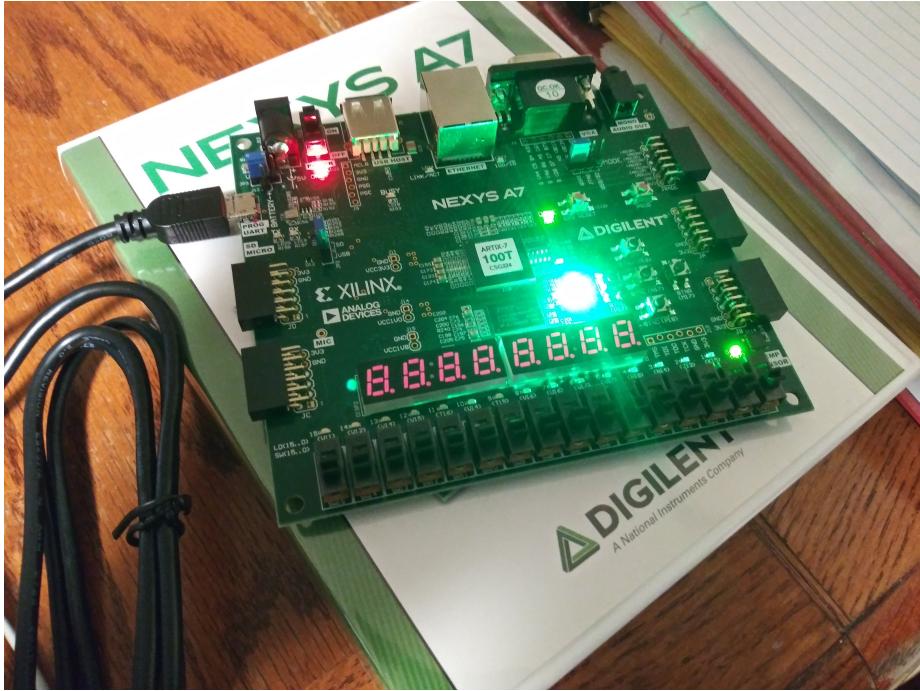


Figure 3: Function 0.

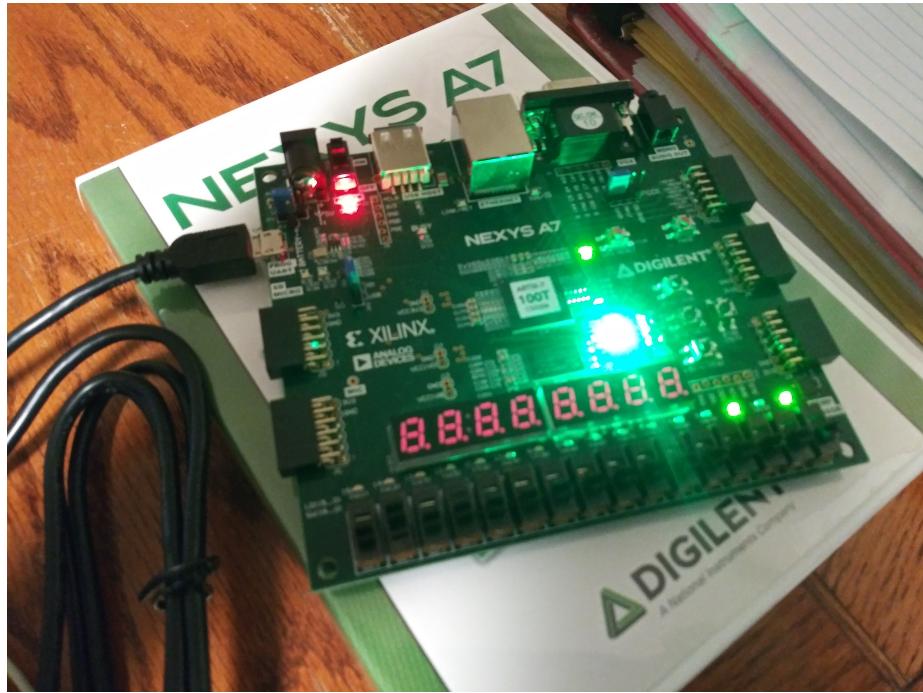


Figure 4: Function 1.

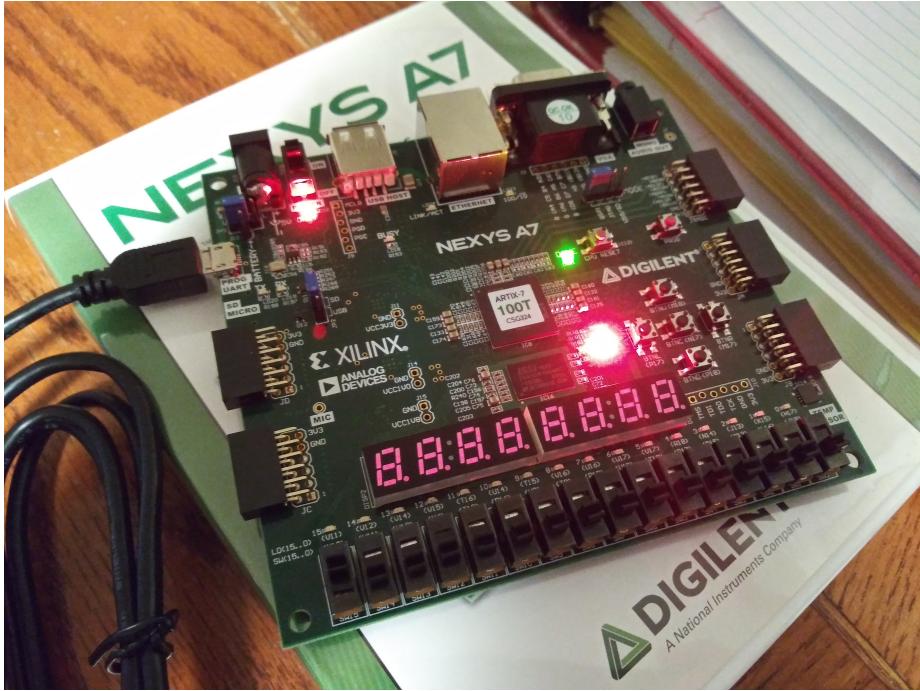


Figure 5: Function 2.

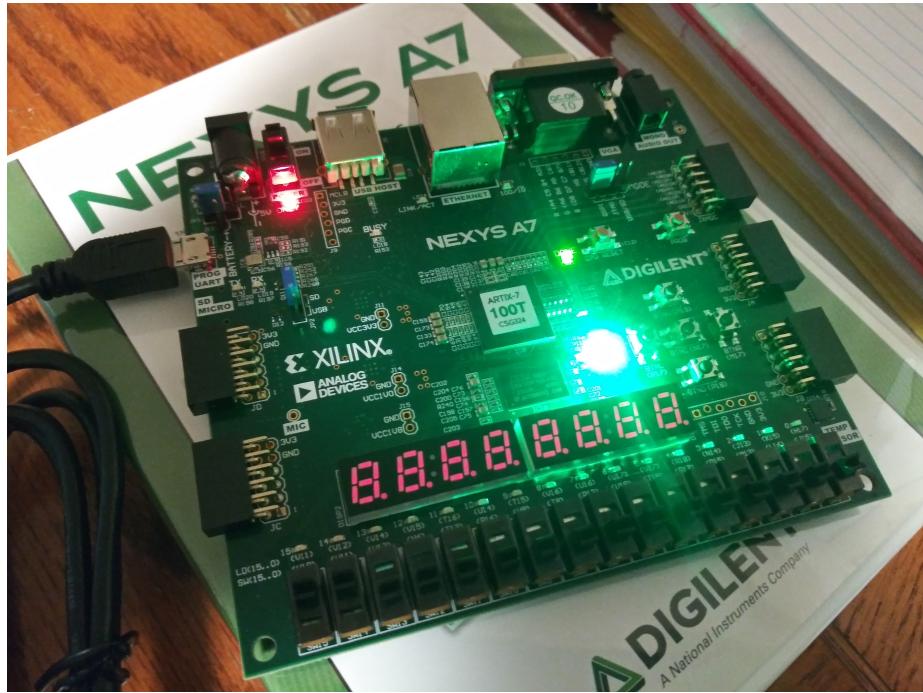


Figure 6: Function 3.