CECS 201 - Lab 6

"Combinational Datapath Components: Adders and Subtractors"

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I certify that this submission is my original work.

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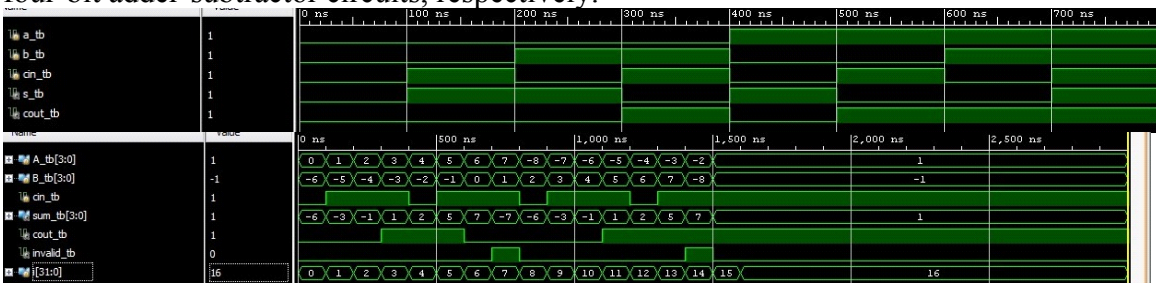
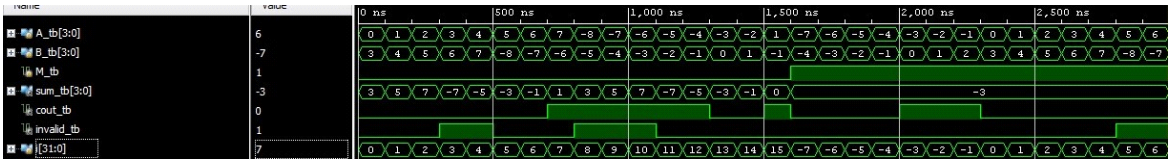
Lab Report: Lab Assignment 6 - "Combinational Datapath Components: Adders and Subtractors"

1. **Goal:** The goal of this lab assignment is to continue practicing the process of programming circuits in Vivado using Verilog. We are also practicing using the FPGA board. In this lab, we created a full adder circuit, a four-bit adder circuit, and a four-bit adder-subtracctor circuit. At the end, we implemented both the full adder circuit and the four-bit adder circuit onto the board.

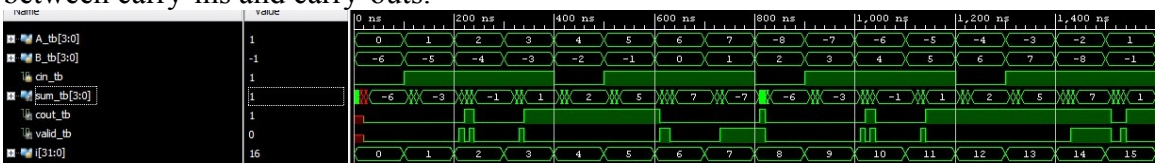
2. **Steps:** First, it was necessary to program the full adder circuit. This circuit was built using logic gates. Next, four full adders were used and connected to one another inside a four-bit adder circuit. It was necessary to define extra wires in order to do so. Then, the four-bit adder was used in conjunction with a 4-bit 2-to-1 multiplexor in order to make the final 4-bit adder-subtractor. The multiplexor is used to select either a normal or inverted input to the adder (one half of 2's complement representation). Finally, I implemented both the full adder and the four-bit adder on the Nexys A7 FPGA board (nonsimultaneously).

3. **Results:** The following are the timing diagrams for the full adder, four-bit adder, and four-bit adder-subtractor circuits, respectively.





The following timing diagram is the same four-bit adder timing diagram, but with delays between carry-ins and carry-outs.



The delay helps show how the carry-ins and carry-outs work.

Here are the truth tables for the full adder and the four-bit adder.

a	b	cin	sum	cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

a	b	cin	cout	sum	invalid?
0000	1010	0	0	1010	0
0001	1011	1	0	1101	0
0010	1100	1	0	1111	0
0011	1101	1	1	0001	0
0100	1110	0	1	0010	0
0101	1111	1	1	0101	0
0110	0000	1	0	0111	0
0111	0001	1	0	1001	1
1000	0010	0	0	1010	0
1001	0011	1	0	1101	0
1010	0100	1	0	1111	0
1011	0101	1	1	0001	0
1100	0110	0	1	0010	0
1101	0111	1	1	0101	0
1110	1000	1	1	0111	1
1111	1001	1	1	1001	0

4. **Conclusion:** I learned how to use top-down design and program a digital circuit in Vivado using Verilog. I also learned how to program the Nexys A7 FPGA board.