2021 CECS 440 Computer Architecture Midterm 2

Student Name: _____

Student ID:_____

Points _____/104

(#1-17 2pts each)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

18 (5pts)	19 (10pts)	20 (5pts)	21 (10pts)	22 (10pts)	23 (10pts)	24 (20pts)

Multiple Choice (2pts each)

1. _____is the most general and least helpful performance metrics for RISC machines.

a) MIPS
b) Instruction Count
c) Number of registers
d) Clock Speed

2. The intel 8086 microprocessor is a _____processor

a) 32 bits
b) 16 bits
c) 8 bits
d) 4 bits

3. The length of the product of an n-bit number and an m-bit number could be a product that is _____ bit long.

a) n+m
b) n*m
c) n/m
d) n-m

4. MIPS provides a separate combine of 32-bit register to contain the ----------bit product, referred to as Hi and Lo

a) 32
b) 18
c) 64
d) 8

5. What will be the add of adding these 2 binary numbers (0000 0111)2 and (0000 0110)2?

a) $(00001101)_2$
b) $(0000\ 1110)_2$
c) $(1100\ 1100)_2$
d) $(0000\ 1101)_2$

6. Multithreading permitting Multiple-threads for sharing the practical units of a

a) Multi processors
b) Single processors
c) Multi core
d) Corei5

7. The elimination stage of WAR and WAW hazards is usually known as

a) Execution
b) Data hazards
c) Dispatch

d) Anti-dependence

8. The Goal of software techniques and hardware techniques is to take advantage of
   a) Copiability
   b) Scalability
   c) Supervision
   d) Parallelism

9. When Instruction I and instruction j tend to write same register or the memory location, it is called?
   a) Input dependance
   b) Ideal pipeline
   c) Output dependance
   d) Digital call

10. The latency clock rate of the AMD operation is
   a) 1
   b) 2
   c) 4
   d) 3

11. Any condition that causes a processor to stall is known as _____
   a) System error
   b) Page fault
   c) Hazard
   d) None of the mentioned

12. The periods of time when the unit is idle is called as _____
   a) Stalls

b) Bubbles
c) Hazards
d) Both a and b

13. Every pair of racks, including one rack-switch and the other holds
a) 40 2u
b) 80 u
c) 80 2u
d) 40 u

14. In pipelining, the CPU executes each instruction in a series of following stages: Instruction Fetching (IF) ——> Instruction Decoding (ID) ——> Instruction Execution (EX) ——>__ and Register Write back (WB).
a) Linear pipelines
b) Non-linear pipelines
c) Structural hazards
d) **Memory access (MEM)**

15.___ occur when an instruction depends on the result of previous instruction in a way that is exposed by the overlapping of instructions in the pipeline.
a) Data hazards
b) Control hazards
c) Structural hazards
d) Hazard in the pipeline

16. Which fetch and issue instructions from a queue or latch?
a) IF
b) DLX
c) ID
d) EX

17. Which is the simplest scheme to handle branches?
a) Freeze or Flush the pipeline
b) Forwarding

c) Assume each branch as not-taken
d) Predict-not-taken or predict-untaken scheme

Answer each question thoroughly:

18. Explain What Are the Different Hazards? How Do We Avoid Them? (5pt)

19. Explain What Are Five Stages in A Dlx Pipeline? (10pt)

20. List 3 of the addressing modes utilized in MIPS.? (5pt)

21. Give An overview of pipelining? (10pt)

22. What is Stalling vs. Forwarding in Data hazards (10pt)

23. Consider the following instruction sequence executing on the 5-stage MIPS pipeline.

LOAD R1, #12(R3)
ADD R6, R1, R7
OR R3, R1, R6
STORE R4, #20(R5)
SUB R6, R4, R3

(a) Draw a pipeline execution diagram for the above instruction sequence, showing the flow of instructions through the pipeline during each clock cycle. Indicate any necessary stalls on the pipeline diagram without Pipeline diagram without forwarding: (10 pts)

Clock Cycle														
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14

(b) Now, assume that all possible forwarding paths have been added to the pipeline. Redraw the pipeline execution diagram, indicating operand forwarding by arrows. (10pts)

Clock Cycle										
Instruction	1	2	3	4	5	6	7	8	9	10