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CECS 440 Section 02

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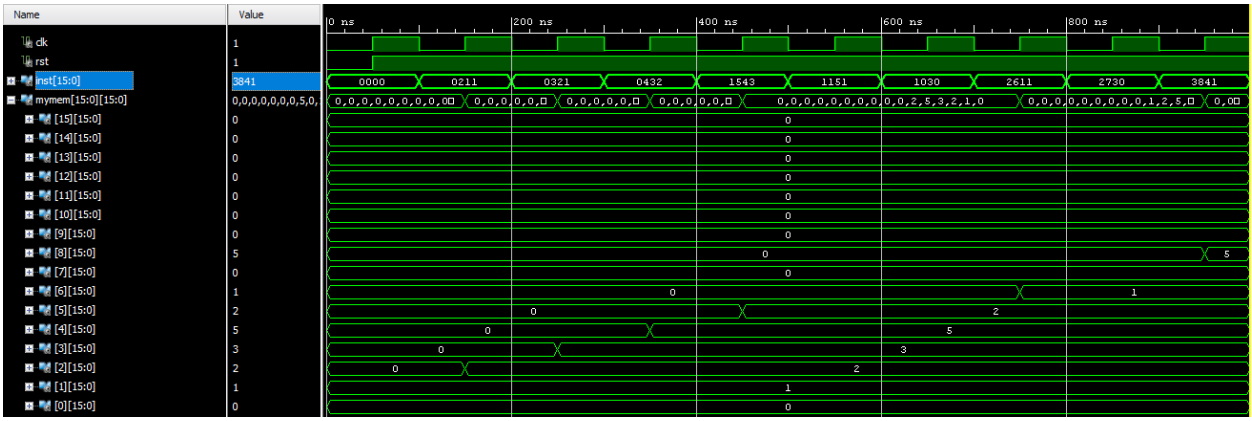
Lab 5

The purpose of Lab 5 is to simulate a very basic processor. This processor takes 16-bit instructions, performs calculations, and saves the result in the specified address. The register is a 16-bit 16-wide memory block that has a few differences from your average load register: it includes build-in asynchronous read outputs that read values from specified addresses in the register. Also, on reset, all values inside the memory are initialized to 0 except the value inside address 1, which is initialized to 1. Lastly, addresses 0 and 1 are untouchable: any attempted writes to these addresses fail, and their values are always 0 and 1, respectively. A video demonstration of this lab can be found here: https://youtu.be/EIHFrSmEKOs.

Here is the waveform of the simulation as seen in the video:



Below is a table as requested in the Lab description detailing the results of all the instructions requested:

Instruction	op	rd	rs	rt	Value in rd
ADD R2, R1, R0	0x0	0x2	0x1	0x0	2
ADD R3, R2, R1	0x0	0x3	0x2	0x1	3
ADD R4, R3, R2	0x0	0x4	0x3	0x2	5
SUB R5, R4, R3	0x1	0x5	0x4	0x3	2
SUB R1, R5, R1	0x1	0x1	0x5	0x1	1
SUB R0, R3, R0	0x1	0x0	0x3	0x0	0
AND R6, R1, R1	0x2	0x6	0x1	0x1	1
AND R7, R3, R0	0x2	0x7	0x3	0x0	0
OR R8, R4, R1	0x3	0x8	0x4	0x1	5