CECS 201 - Lab 7

"Synchronous Sequential Logic: Registers'"

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I certify that this submission is my original work.

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Lab Report: Lab Assignment 7 - "Synchronous Sequential Logic: Registers'"

1. **Goal:** The goal of this lab assignment is to learn to progam digital sequential circuits, as this is the first sequential circuit that we have programmed. Another goal is to implement said circuit onto the Nexys A7 FPGA board. A challenge was inplementing a 32-bit register onto a board which only has 16 LEDs; this requires a multiplexor to select the top or bottom 16 bits.

2. **Steps:** First, it was necessary to program a basic register to learn how they function and how they are programmed. This first register is an 8-bit register, and functioned by giving the data input to the output on the rising edge of a clock input. This register also had a reset input that would reset the register regardless of the clock input.

   After this first register, we added a load input, so that when the load input was off, the output would stay the same, but if the load input was on, the output would match the data input.

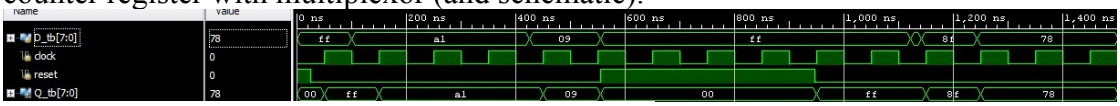
   Next, unrelated to the previous two registers, the next register built was a 32-bit register. Unlike the previous two registers, there was no data input: on the rising edge of the clock, the counter would add one to its previous output. A reset input like the other two registers was also implemented.

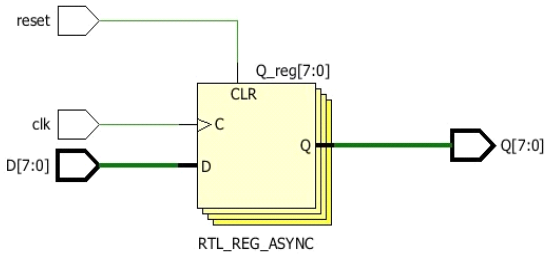
   Lastly, after extensive testing, this 32-bit counter was used in a different module in order for it to be implemented onto the Board. A 16-bit 2-to-1 multiplexor selects between the top or bottom half of the 32 bit counter, because the Board only has 16 LEDs to display bits on.

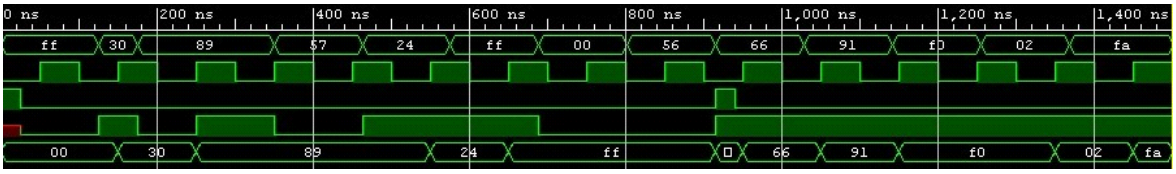
   This last module was implemented onto the Board, using the right three switches (from right to left) as the multiplexor selector, the enable for the count register, and the register reset, respectively.

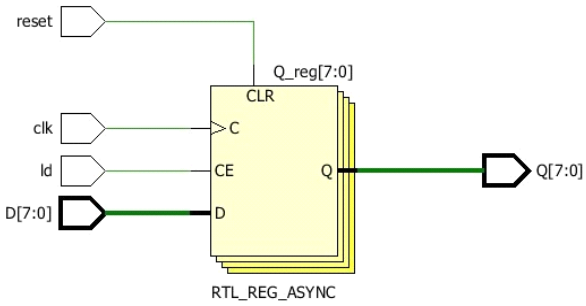
3. **Results:** The following are the timing diagrams for the 8-bit register (and schematic), 8-bit load register (and schematic), 32-bit counter register (and schematic), and 32-bit

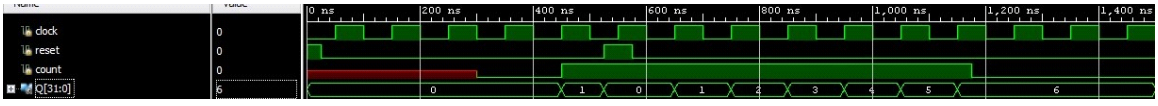
counter register with multiplexor (and schematic).

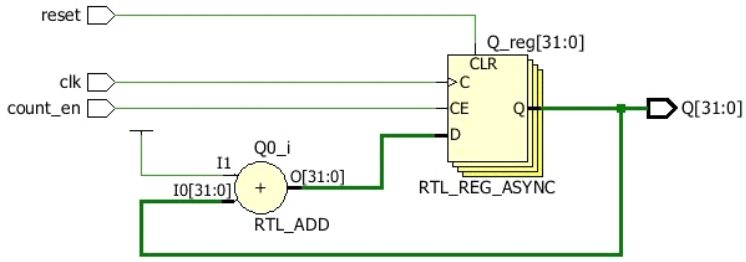


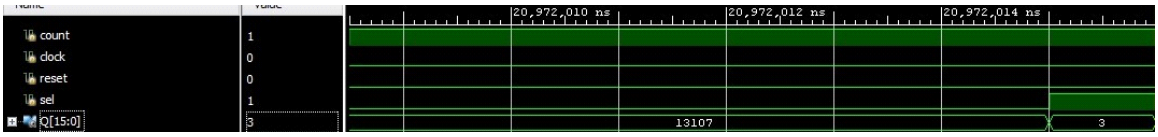


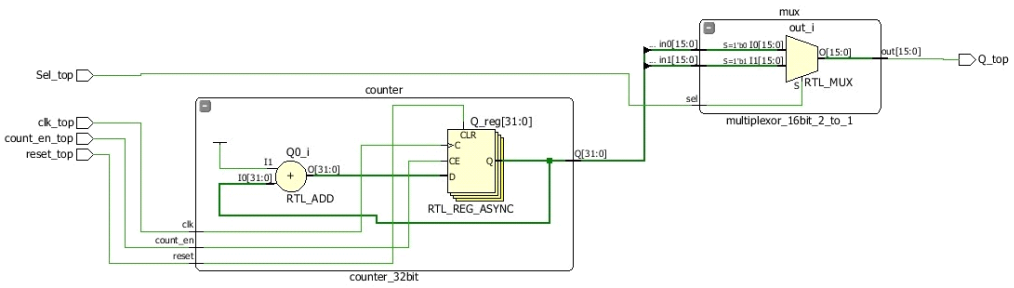












One interesting result I had is that the bottom 16 bits (bits 0 through 15) are always lit up when the counter is running. This is because the counter register is updating

at 50 GHz, which is too fast for the human eye to see. The top 16 bits are more visible; though bits 16 through 22 are still a bit too fast to see, the last few bits can be clearly seen counting up.

4. **Conclusion:** I learned how to use top-down design and program a digital sequential circuit in Vivado. I also learned some of the constraints of using an FPGA Board (mostly the finite amount of LEDs) and one way to get over these limitations, in this case by using a multiplexor. I did not have any problems with programming either the modules or the Board.