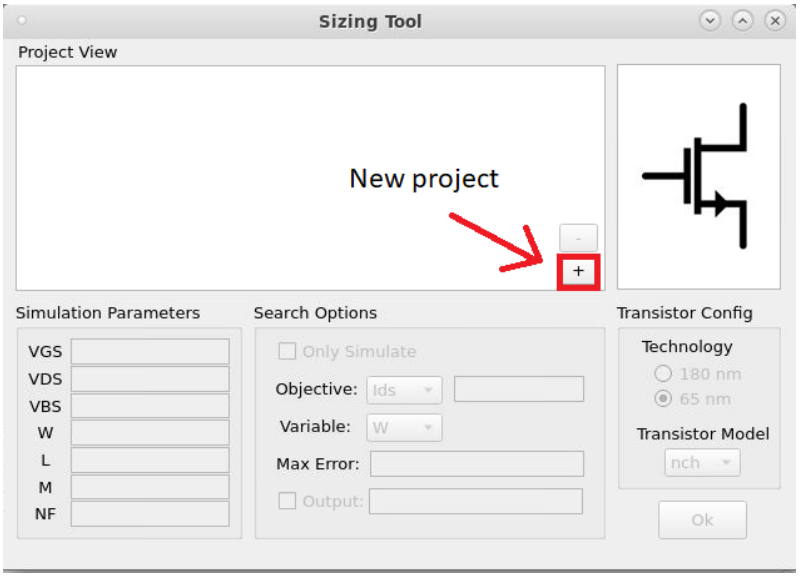
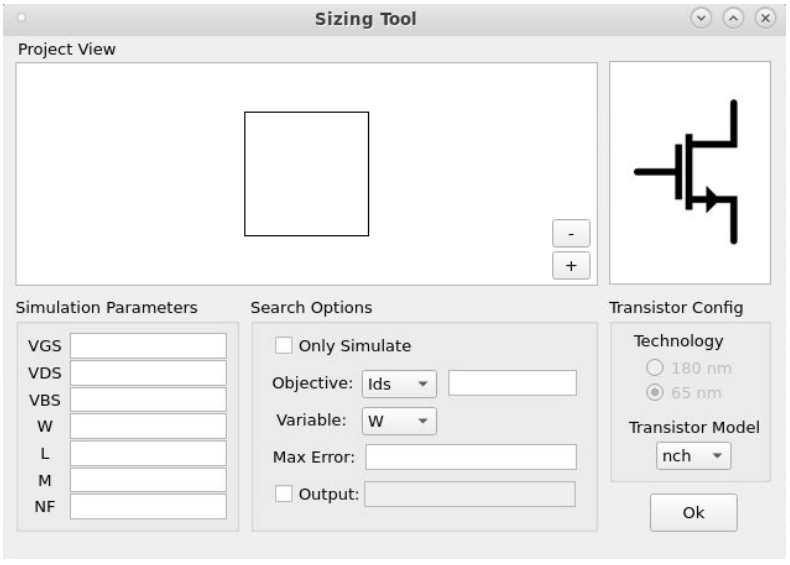
Sizing Tool Tutorial

To open the software, use the Cadence Virtuoso CIW menu.

The Sizing Tool window will be shown. To start a new project, click the “+” button:





After that, all the fields will be enabled. You can fill the text fields with the parameters of the transistor you want to simulate in the “Simulation Parameters” tab.
In the “Search Options” tab you will find the following parameters:

- **Only Simulate**: if the box is checked, the software will simulate the transistors with the parameters entered, but will not search for any specific parameter.
- **Objective**: You can select the parameter you want to search and then write the target value.
- **Variable**: This is the parameter that will be varying during the simulations.
- **Max Error**: The maximum error accepted for the project.
- **Output**: You can write the name of a parameter you want to use in the next simulation. See the examples for further explanation.

In the right side of the window, there is the transistor configurations tab. The technology cannot be switched after opening the software, since it depends directly on the virtuoso environment. If you want to change the technology, you must open the respective virtuoso environment for that technology. The transistor models depend on the technology used, for example, for 65 nm, the available models are “nch” (n-channel) and “pch” (p-channel).

If the parameters are not correctly entered, it may cause an error in the simulation process. If that is the case, you will see the following message:

If everything is typed correctly, the simulation process will occur with no major problems.

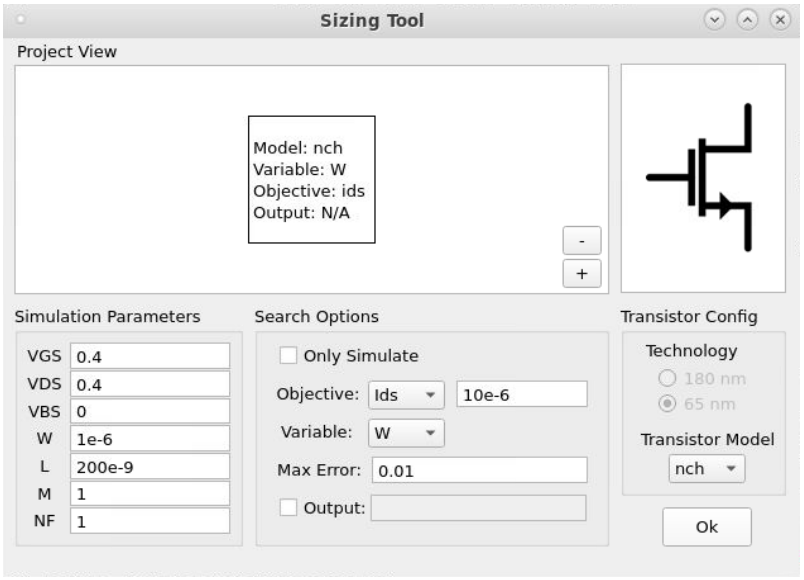
Examples:

1) In this example, a single transistor will be simulated, using the following parameters:

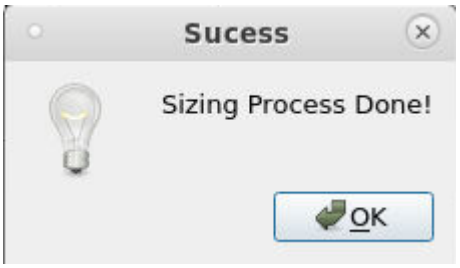
VGS	0.4 V
VDS	0.4 V
VBS	0 V
W	1e-6 m
L	200e-9 m
M	1
NF	1

The objective will be to find the value of **W** in a **NMOS** transistor on which we can get the current **Ids** = 10e-6 A.

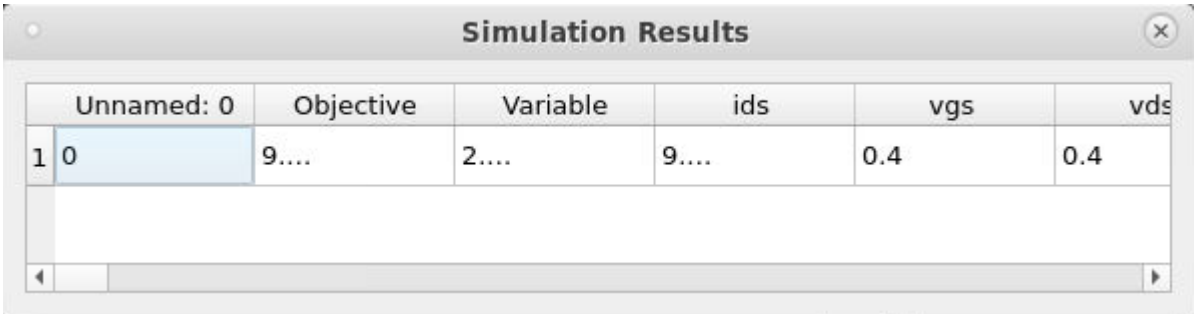
After typing the parameters into the respective fields, click the button “Ok”. The preview will show some parameters of the sizing process:



When the process is finished, a message will appear, confirming the successful search.



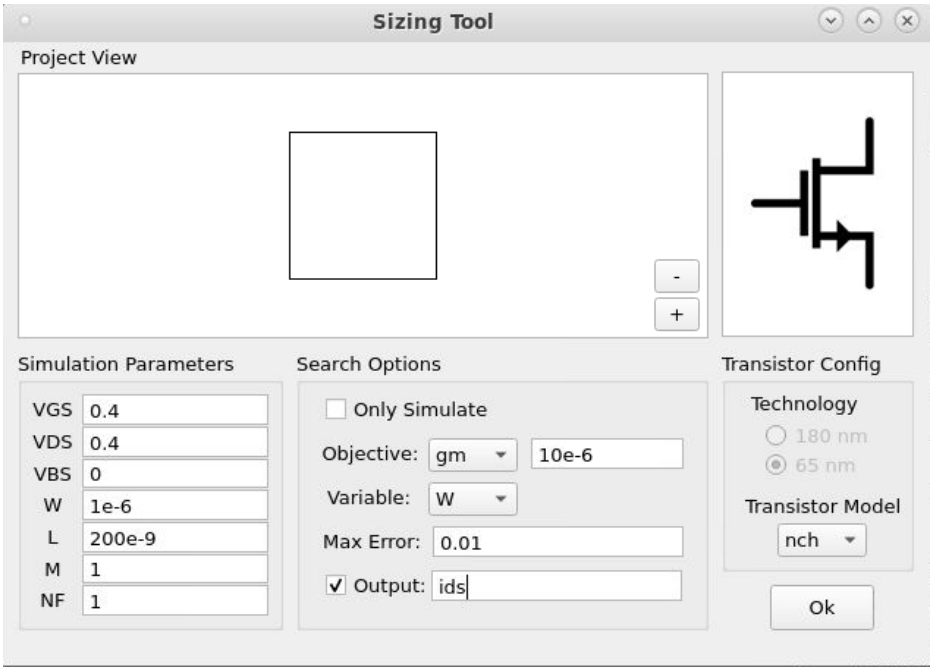
Then, the simulation results will be shown in a table:



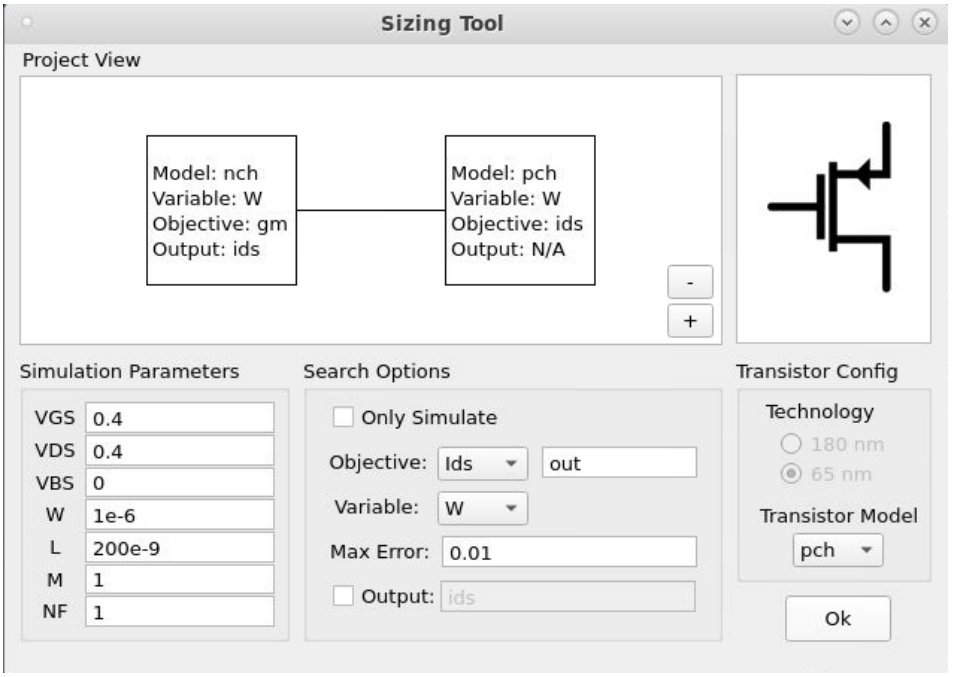
The file containing these values is located in the path “Circuit Sizing Tool/files/outputs”.

2) In this second example, we will simulate 2 transistors, a NMOS and a PMOS transistors, using the output parameter of the NMOS as the objective for the PMOS.

Using the same parameters as the first example, the project steps can be seen below:



The NMOS transistor is set to output the value of the parameter **Ids**. To attach more steps to the project, click on the “+” button.



The project will be shown as the figure above.

Notice that, to use the output value of the simulation done before, it is necessary to write “out” in the objective text field.

The results can be seen below: