CR - Project Proposal

Title of the project:

Cyclic Redundancy Check encoder with hardware Co-Processor.

Brief description of the functionality:

System with a DMA-assisted hardware accelerator for calculating a 16 bit CRC with a given generating polynomial of 17 bits.

Brief description of the proposed architecture:

The system will include a custom hardware module executing the CRC consecutive divisions, over an input message of 32 bits. Saving the results of the most used operations in the consecutive divisions in order to save time. The performance of software and hardware implementations will be analyzed and compared.

Why to use the suggested custom hardware module?

Reduce the CRC calculation time.

Test procedure and user interaction

Input data will be randomly generated. Software will check the hardware results. Testbench for the CRC encoder. User interaction through UARTLite and serial terminal.

P2 - G1
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