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Single Crossbar Array of Memristors With Bipolar Inputs for Neuromorphic Image Recognition

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 **ABSTRACT** In this paper, we propose a new crossbar architecture of memristors with bipolar inputs for animage recognition application. The performance of the proposed crossbar array with bipolar inputs is based on the simpli ed Exclusive-NOR function to measure the similarity between the input pattern and the stored patterns. In the proposed architecture, only one crossbar array is used instead of two crossbar arrays. The number of memristors in the proposed architecture is reduced by 50%, when compared to the complementary and the twin architectures. The proposed crossbar architecture with bipolar inputs consumes 16.7% and 7.2% less power than do the complementary and twin architectures. In addition, using only one crossbar array in the proposed architecture can improve the fault tolerance of the crossbar circuit. When 10% of memristors are defective, the proposed crossbar architecture shows a recognition rate improved by 5%, 7% and 4% over that of the memristor binarized neural network, the complementary architecture of the memristor crossbar and the twin architecture of the memristor crossbar when recognizing 10 images.



 **INDEX TERMS** Memristor, crossbar array, synaptic weight, image recognition.



**I. INTRODUCTION**

Neuromorphic computing was conceptually developed by C. Mead in the late 1980s [1]. It refers to a very-large-scale integration (VLSI) system for mimicking the functionality of biological neurons in nervous systems. VLSI implemen-tations of neuromorphic computing systems have gained more advantages in the past two decades [2], [3]. However, VLSI designs are predominantly based on CMOS technology, which is approaching the limit of physical scaling [4], [5]. The emerging memristive devices, termed memristors, have been considered a promising candidate for realizing neuro-morphic computing systems. The memristor was postulated by L. O. Chua in 1971 and experimentally demonstrated by HP Labs in 2008 as a fourth fundamental circuit ele-ment [6], [7]. Memristors have been potentially used to imple-ment neuromorphic computing systems because the change in a memristor’s conductance caused by the applied pulses is very similar to the plasticity behavior of synapses [8] [12]. More interestingly, the memristor’s conductance can be mod-i ed by the current owing through it. This characteris-tic of memristors is very similar to the brain’s plasticity and behavior [8]. Memristors can be formed as a crossbar array, in which any two crossing wires are connected by a

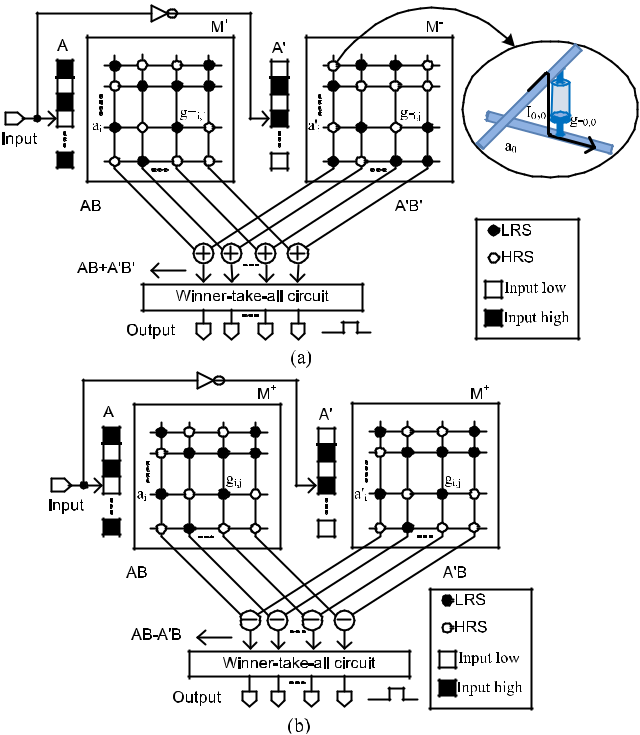
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memristor [13]. Memristor crossbar arrays with a possible 3-D architecture seem suitable to realize the high connectivity of a brain’s neuronal system [14], [15]. Recently, memristor crossbar arrays have been suggested as a way to achieve high cost- and energy-ef cient implementation of arti cial neural networks [16] [20]. To realize the signed synaptic weights, two memristor crossbar arrays are employed [19] [21]. The sign and magnitude of the synaptic weights are controlled by adjusting the values of the two memristors in two crossbar arrays. The memristor-crossbar-array-based implementations of arti cial neural networks are promising; however, they require an abundance of computational tasks and training processes. Other approaches for neuromorphic pattern recog-nitions have been proposed recently [22], [23]. The comple-mentary architecture, in which one memristor crossbar is the inversion of the other, is used for the application of speech recognition [22]. It is based on a logical Exclusive-NOR (XNOR) operation, which can measure the similarity of two binary arrays [22]. The twin crossbar architecture employing two identical crossbar arrays has been proven capable of measuring the similarity between an input pattern and the stored patterns as well [23]. The twin crossbar architecture consumes less power than the complementary crossbar archi-tecture does for the application of image recognition [23]. However, there are several drawbacks with memristor cross-bar architectures such as the sneak path leakage, the process

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**FIGURE 1.** Crossbar architecture of memristors for neuromorphic patternrecognition. (a) The complementary architecture [22], and (b) the twin architecture [23].



variation, and the fault of crosspoints [24]. In the previous works, two crossbar arrays are utilized to implement the signed synaptic weights of an arti cial neural network or to perform the XNOR function. In this work, we propose a single crossbar array with bipolar inputs for realizing the sim-pli ed XNOR function for measuring the similarity between the input pattern and the stored patterns. The proposed single crossbar array is implemented in the application of image recognition. The number of memristors is reduced by half. As a result, the power consumption is reduced. The impact of memristance variation and the fault of memristors are mitigated signi cantly.

1. **MEMRISTOR CROSSBAR ARCHITECTURE FOR NEUROMORPHIC IMAGE RECOGNITION**

**A. THE COMPLEMENTARY ARCHITECTURE AND THE TWIN ARCHITECTURE OF MEMRISTOR CROSSBARS**

Fig. 1(a) shows a conceptual diagram of a complemen-tary crossbar architecture of memristors for pattern recogni-tion [22]. It is based on the Exclusive-NOR (XNOR) function to measure the similarity between the input pattern and the stored patterns [22]. In Fig. 1(a), gC0;0 is the crosspoint’s conductance between the rst row and the rst column in the MC array. a0 is the input to the rst row of the MC array. I0;0 is the current owing through the crosspoint between the rst row and the rst column. The current I0;0 is high if and only if the input is high, and the crosspoint is a low-resistance memristor. Therefore, the current I0;0 is considered as a result of an AND function with its inputs as the input a0 and the

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crosspoint state. The crosspoints are either a low-resistance state (LRS) or high-resistance state (HRS) for storing the data of 1 or 0. In Fig. 1(a), A is a vector of inputs, B is stored patterns, and A’ and B’ are the inversions of A and B. The two memristor crossbar arrays in Fig. 1(a) perform the XNOR function to measure the similarity between the input pattern and the stored patterns in the crossbar array as presented in the following equation [25].

|  |  |  |  |
| --- | --- | --- | --- |
|  | D *AB* C *A*0*B*0 | (1) |  |
| *A B* |  |

The winner-take-all circuit compares all columns and pro-duces the winner corresponding to the column that is regarded as the best match to the input pattern [22], [23]. The XNOR function in Eq. (1) can be expressed as Eq. (2)

|  |  |
| --- | --- |
| *A B* D *AB*C *A*0(1 *B*) |  |
| D *AB A*0*B*C*A*0 | (2) |

In Eq. (2), A’ is neglected because it is a constant and has no operation with the stored pattern B. For this reason, AB A’B can measure the similarity between the input pattern and the stored pattern as well. Here, two identical crossbar arrays are used to store the patterns instead of using two complementary crossbar arrays [23]. Eq. (2) can be implemented using the twin crossbar architecture, as concep-tually shown in Fig. 1(b) [23]. The twin crossbar architecture has been demonstrated to be better than the complementary crossbar circuit in terms of power consumption and variation-tolerance [23], [26].

The complementary and twin crossbars of binary memris-tors exhibit very interesting results in the application of pat-tern recognition; however, the variation in memristance and the faults in crosspoints degrade the performance of crossbar circuits considerably [24], [27], [28]. Two crossbar arrays cannot be completely identical or complementary because of the variation in the conductance of crosspoints. Furthermore, memristor defects prevailingly occur in the crossbar array, with the result being that it is impossible to obtain two com-plementary or identical arrays. Therefore, trying to use only one crossbar array becomes a crucial solution for practically feasible neuromorphic pattern recognition circuits.

1. **THE PROPOSED SINGLE MEMRISTOR CROSSBAR ARRAY**

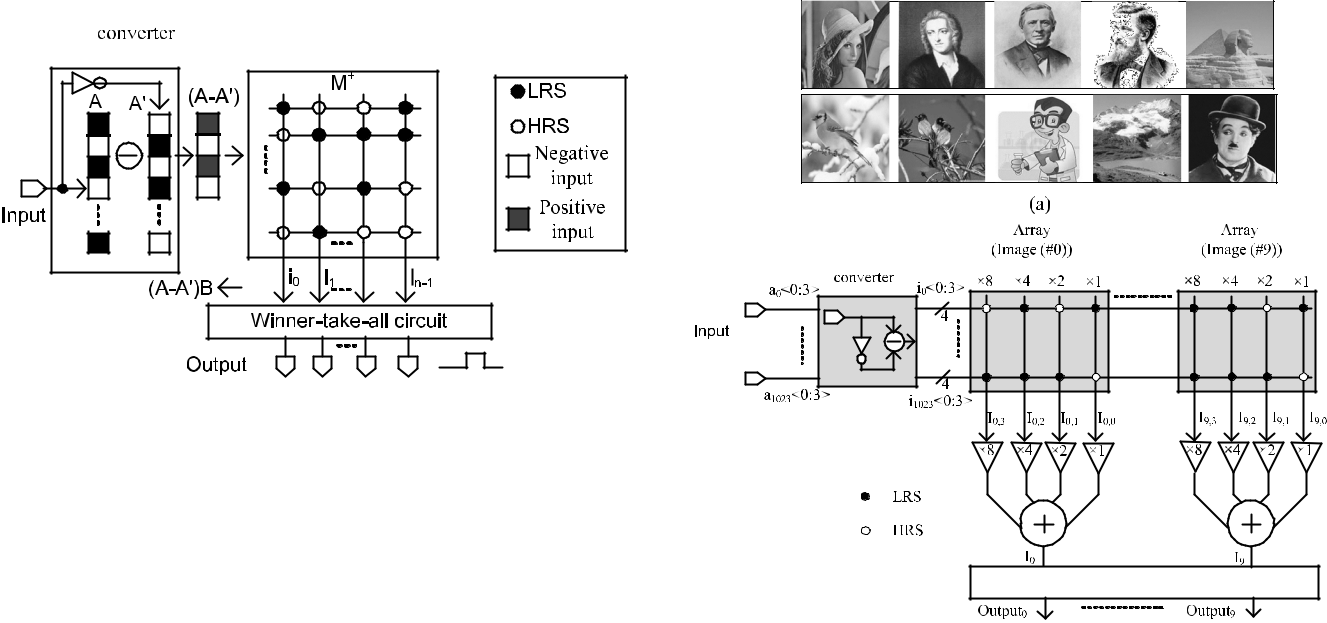
The XNOR function presented in Eq. (1) can be simpli ed as follows

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | D *AB* C *A*0(1 *B*) | |  |  |
| *A B* |  |  |
|  | D *AB* | *A*0*B* C *A*0 |  |  |
|  | D (*A* | *A*0)*B* C *A*0 | (3) |  |

The exclusive NOR function used to measure the similarity between the input pattern and the stored pattern is simpli ed, as presented in Eq. (3). It appears that only one memristor crossbar can be used to realize the XNOR function, instead of using two identical crossbar arrays. In Eq. (3), A’ can be neglected since it is a constant, as mentioned. A and A’ are the

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**FIGURE 2.** The proposed memristor crossbar architecture that employs

only one crossbar array for neuromorphic pattern recognition.

input vector and its inversion. Then, Eq. (3) can be rewritten

as Eq. (4)

|  |  |
| --- | --- |
| *A B* D *IB*C*A*0 |  |
| *where I* D(*A A*0) | (4) |



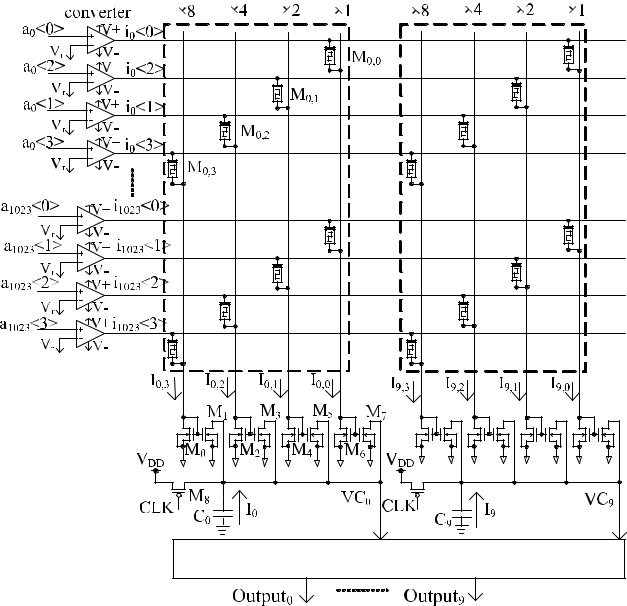
Here, I is a vector of bipolar inputs, that means, if the input vector A is {0, 1, 0, 1}, I is given by a vector of { 1; 1; 1; 1}.

Inspired from Eq. (4), the bipolarized inputs are applied to the crossbar to measure the similarity between the input pat-tern and the stored ones. The optimized crossbar architecture with only one crossbar array is shown in Fig. 2.

Fig. 2 shows a conceptual diagram of the proposed crossbar architecture, in which only one crossbar array of memristors is used to store the patterns. The column-line current i0 repre-sents the similarity between the input pattern and the pattern stored in the rst column. Similarly, the column-line current in 1 represents the similarity between the input pattern and the pattern stored in the last column. All the column-line currents from i0 to in 1 are fed into a Winner-take-all circuit, which nds the maximum column-line current corresponding to the column that is the best match with the input vector.

Fig. 3(a) shows 10 32 32 grayscale images used to test the proposed crossbar architecture. Each image is converted to a vector of 1024 pixels. Each pixel is digitalized by 4 bits. Fig. 3(b) shows a block diagram of the proposed single mem-ristor crossbar with bipolar inputs for image recognition. The inputs from a0 to a1023 are obtained from 32 32 grayscale images. i0 <0:3> are bipolar inputs obtained from a0 <0:3>. The bipolarized inputs of i0 <3>, i0 <2>, i0 <1>, and i0 <0> are connected to the columns with weights as large as 8, 4, 2, and 1, respectively. I0 is the result of the weighted summation for the rst image (#0). I0 represents the amount of similarity between the input vector and the rst image (#0). Similarly, I9 is the result of the weighted summation for the stored image (#9). I9 represents the similarity between the input vector and the stored image (#9). The winner-take-all circuit can choose one stored image that is the best match to the input image by comparing the currents from I0 to I9 [22], [23].

**FIGURE 3.** (a) The 32 32 grayscale images stored in the crossbar arrayand (b) the block diagram of the proposed single crossbar architecture with bipolar inputs for image recognition.



**FIGURE 4.** The schematic of the proposed crossbar architecture withbipolar inputs for neuromorphic image recognition.

Fig. 4 shows a detailed schematic of the proposed crossbar architecture. The input pixels from a0 to a1023 are converted to bipolar inputs of i0 to i1023 using the unipolar to bipolar con-verter circuits simply realized by the comparators, as shown in Fig. 4. The bipolarized input of i0 <3> connects to the column with a weight as large as 8. Similarly, the inputs of i0 <2>, i0 <1>, and i0 <0> are connected to the columns with the weights as large as 4, 2, and 1, respectively. M0;3, M0;2, M0;1, and M0;0 are memristors for the crossbar array of image (#0), where i0 <3>, i0 <2>, i0 <1>, and i0 <0> are applied. The transistors M0 and M 1 constitute a current

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**III. SIMULATIONS AND RESULTS**

**The proposed memristor circuit in Fig. 4 was simulated using a Cadence Spectre circuit simulation [27]. Memristors are modeled using Verilog-A [28]. The 32 32 grayscale images shown in Fig. 3(a) are digitalized by 4 bits. Each image is**

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**I0 represents the similarity of the input vector and the stored image (#0). I9 is for the stored image (#9). C0 is discharged by I0. If I0 is large, C0 can be discharged very fast. If I0 is small, it takes a longer time to discharge. The capacitor C0 is precharged by M8 when CLK is low. When CLK is high, the winner-take-all circuit compares the discharging times of the**

**10 VC nodes from VC0 to VC9 and produces the activated output corresponding to node that is the fastest discharged to GND [21], [22]. The VC node chosen by the winner-take-all circuit is regarded as the best match to the applied input vector [21], [22].**

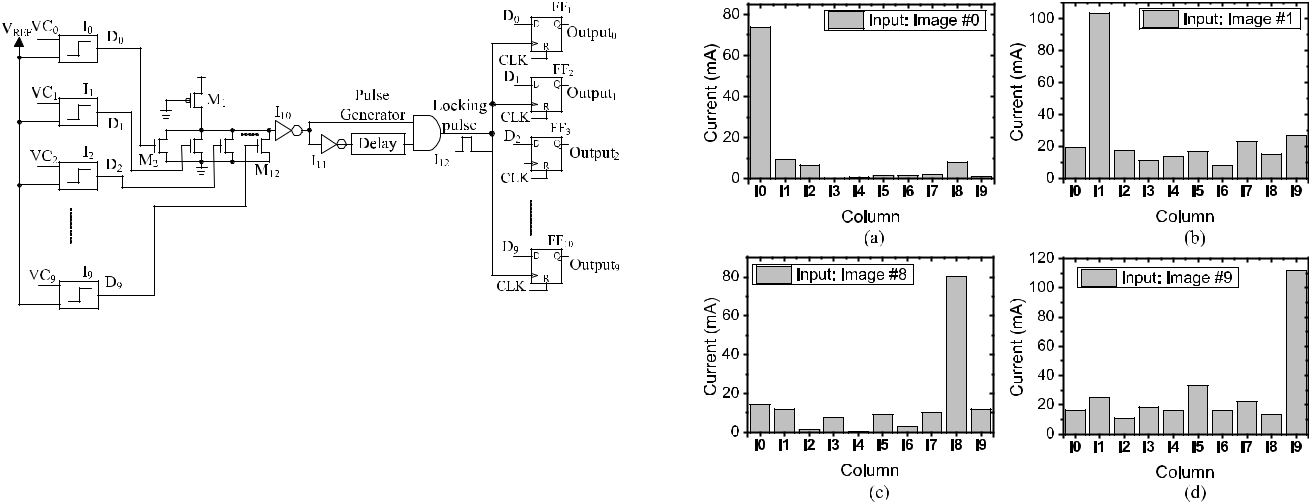
**The proposed architecture differs from the previous work. We use only one crossbar array, instead of two crossbar arrays, to conserve the power consumption and the area occupation. The weighted currents of I0 to I9 represent the amount of similarity between the applied input image and the 10 stored images. The values of the 10 weighted currents are used to discharge the capacitors C0 to C9, as shown in Fig. 4. The winner-take-all circuit detects the fastest discharge node among the 10 nodes**

**Fig. 5 shows the winner-take-all circuit that can detect which capacitor becomes discharged the fastest among the ten capacitors [22]. The comparators I0 to I9 compare VC0 to VC9 with a reference voltage, VREF. If VC0 becomes lower than VREF, D0 becomes high. The transistors M1 to M12 constitute a multiple input NOR gate. I11, I12, and a delay circuit constitute a pulse generator circuit. When one of the data from D0 to D9 becomes high, a locking pulse is generated to load D0 to D9 to the outputs Output0 to Output9.**

**mirror with a ratio as large as 8. To do this, M1 should be eight times that of M0. By the same way, M3 should be four times M2 to realize the weight of 4, and M5 should be twice as large as M4 to realize the weight of 2. M6 and M7 have the same size for the weight of 1. The weighted current I0 can be calculated as follows**

**FIGURE 5.** The schematic of a winner-take-all circuit to detect the fastestdischarge node among the 10 nodes [22].

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**FIGURE 6.** (a) The weighted currents I0to I9when the image (#0) isapplied to the inputs. I0 is the largest current indicating that the input image is best matched with the stored image (#0). (b) The weighted currents I0 to I9 when image (#1) is applied to the inputs. I1 is the largest

*I*0 D 8*I*0;3 C 4*I*0;2 C 2*I*0;1 C *I*0;0 (5) current among the 10 currents for recognizing image (#1). (c) and (d) The weighted currents I0 to I9 when image (#8) and image (#9) are applied to

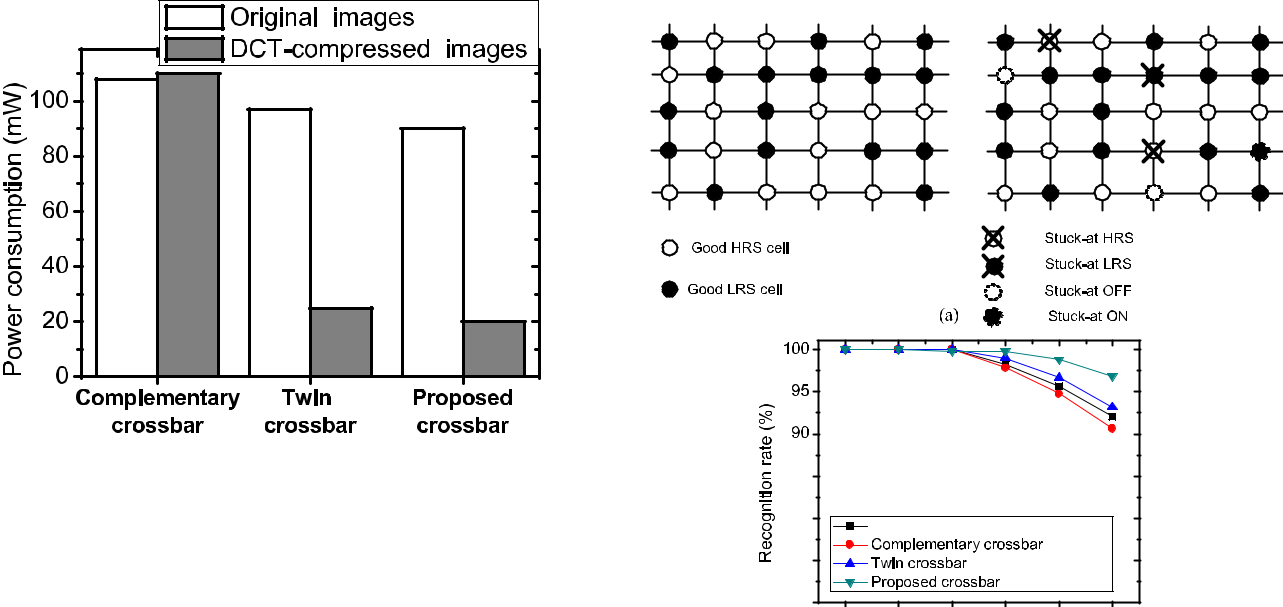
the inputs.

stored in 4 columns of the crossbar array with the weights being 8, 4, 2, and 1, respectively. Fig. 6(a) shows the weighted currents from I0 to I9 when image (#0) is applied to the crossbar. Among the 10 weighted currents, I0 is the largest one to indicate that the stored image (#0) is the most similar to the input image. That means the crossbar can recognize image (#0). Similarly, the weighted currents of I1, I8, and I9 are the largest currents when the input images are image (#1), image (#8), and image (#9), respectively. The winner-take-all circuit can choose the largest current among the 10 currents. The simulation results shown in Fig. 6 verify that the proposed single memristor crossbar with bipolar inputs can be used for the application of image recognition based on measuring the similarity between the input image and the stored images.

In the proposed architecture of a memristor crossbar for image recognition, only one memristor array is used instead of two crossbar arrays, as with the previous work. The advantage of the proposed architecture is that the number of memristors is reduced by half leading to the reduction in power consumption. Fig. 7 shows the comparison of power consumptions among the complementary architecture, the twin architecture, and the proposed architecture. The power consumptions shown in Fig. 7 are measured for the whole circuit including the crossbar array and the external circuits. In Fig. 7, we measure the power consumption of the circuit using the Cadence Spectre circuit simulation. The proposed single crossbar array with bipolar inputs consumes less power than do the complementary crossbar array and the twin crossbar array by 16.7% and 7.2%, respectively, for recognizing the original images. For DCT-compressed images, the proposed crossbar shows a power consumption reduced by 82% and 20%, when compared to the those of the complementary and the twin crossbar architectures. Though the unipolar to bipolar converter circuits are added to the

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**FIGURE 7.** The comparison of the power consumptions among thecomplementary architecture, the twin architecture, and the proposed architecture of a crossbar array.

proposed circuit, the single crossbar circuit consumes less power than the complementary and twin crossbar circuits because one memristor crossbar is utilized, and the memristor crossbar consumes more power than the external circuits such as unipolar to bipolar converter circuits.

One of the major challenges of memristor crossbar arrays is the crosspoint fault [24]. The faults of crosspoints can be de ned as stuck-defects and categorized as stuck-at-LRS, stuck-at-HRS, stuck-at-ON, and stuck-at-OFF [24]. LRS and HRS mean low-resistance state and high-resistance state. The state-of-the art memristor arrays have a fault rate as high as 10%, which causes the performance of a crossbar array to be severely degraded [29], [30]. Fig. 8(a) shows the ideal crossbar without defects and the real crossbar with defects. In Fig. 8(a), stuck-at-LRS faults mean the crosspoints are always in a low-resistance state. By contrast, stuck-at-HRS faults mean the crosspoints are always in a high-resistance state. These memristors cannot be programed to change their memristance values. Stuck-at-ON faults indicate that the crosspoints constantly conduct current, and these crosspoints ideally have zero resistance. Stuck-at-OFF faults mean the crosspoints have in nite resistance. In this work, we assume that the four levels of faults occur in the crossbar array, as shown in Fig. 8(a).

Fig. 8(b) shows the comparison of recognition rates among the memristor binarized neural network, the complemen-tary architecture of memristor crossbars, the twin archi-tecture of memristor crossbars, and the proposed single memristor crossbar with bipolar inputs. The memristor bina-rized neural network was proposed in a previous work with 1024 inputs, 2048 hidden units, and 10 outputs and is trained for recognizing the 10 images shown in Fig. 3(a) [20]. For the complementary and twin crossbar arrays, two arrays of 1024 rows and 40 columns are designed to store 10 4-bit images [22], [23]. The proposed single crossbar array is shown in Fig. 4. The percentage of faults varies from 0% to 10%. The faults are randomly selected among stuck-at-LRS, stuck-at-HRS, stuck-at-ON, and stuck-at-OFF. When the percentage of faults increases, the recognition

**FIGURE 8.** (a) The ideal crossbar without defects and the real crossbarwith defects. (b) The comparison of recognition rates among the memristor binarized neural network, the complementary architecture, the twin architecture, and the proposed architecture. Here the percentage of faults is varied from 0% to 10%. The faults are randomly selected among stuck-at- LRS, stuck-at-HRS, stuck-at-ON, and stuck-at-OFF.



rates of the binarized neural network, the complementary architecture, and the twin architecture decline dramatically. When the percentage of faults is 10%, the recognition rates of the memristor binarized neural network, the complementary architecture, and the twin architecture are as low as 92%, 90% and 93%, respectively. The proposed single crossbar with bipolar inputs shows a good recognition rate, when compared to that of the others. When the percentage of faults is 10%, the recognition rate of the proposed crossbar with bipolar inputs is as high as 97%. The difference in recognition rates can be inferred from the architecture of the crossbar. The stuck-at-ON is the most serious problem because it produces the largest current. In the complementary architecture, the currents in the two columns of two crossbars are added together, as indicated in Fig. 1(a). Therefore, if the stuck-at-ON occurs in both columns, the weighted cur-rent can increase remarkably. As a result, the recognition rate degrades dramatically. The memristor binarized neural network and the twin architecture use subtractions instead of additions. Therefore, the variation in weighted currents caused by memristor defects can be partially compensated. In the proposed architecture, the number of memristors is reduced by half. Additions and subtractions are not used in the proposed crossbar circuit. For these reasons, the proposed single crossbar shows a high recognition rate when 10% of the crosspoints are defective, when compared to that of the memristor binarized neural network, the complementary architecture and the twin architecture of memristors.

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For the same functionality of measuring the similarity between the input image and the stored images for image recognition; however, the proposed architecture of a memris-tor crossbar with bipolar inputs employs only one memristor crossbar. It is based on the simpli ed XNOR function. The number of memristors is reduced by half, thus lowering the power consumption and mitigating the impact of the varia-tions and the faults in the memristor crossbar array.

**IV. CONCLUSION**

In this paper, we proposed a single memristor crossbar cir-cuit with bipolar inputs for neuromorphic image recognition. The proposed single memristor crossbar with bipolar inputs was demonstrated to be capable of measuring the similarity between the input pattern and the stored patterns based on the simpli ed XNOR function. The number of memristors in the proposed architecture is reduced by 50% when compared to that of the complementary architecture and the twin architec-ture. The proposed architecture consumes 16.7% and 7.2% less power than do the complementary architecture and the twin architecture, respectively. In addition, using only one crossbar array in the proposed architecture can improve the fault tolerance of the crossbar circuit. When 10% of memris-tors are defective, the proposed crossbar architecture shows a recognition rate that is 5%, 7%, and 4% better than that of the memristor binarized neural network, the complemen-tary architecture, and the twin architecture of the memristor crossbar.

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