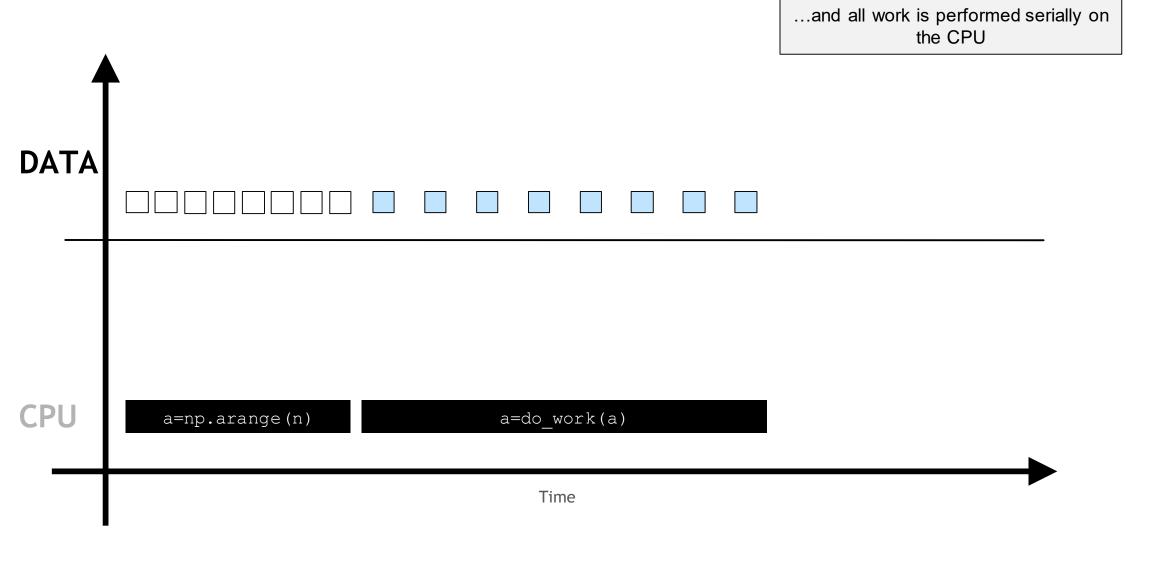
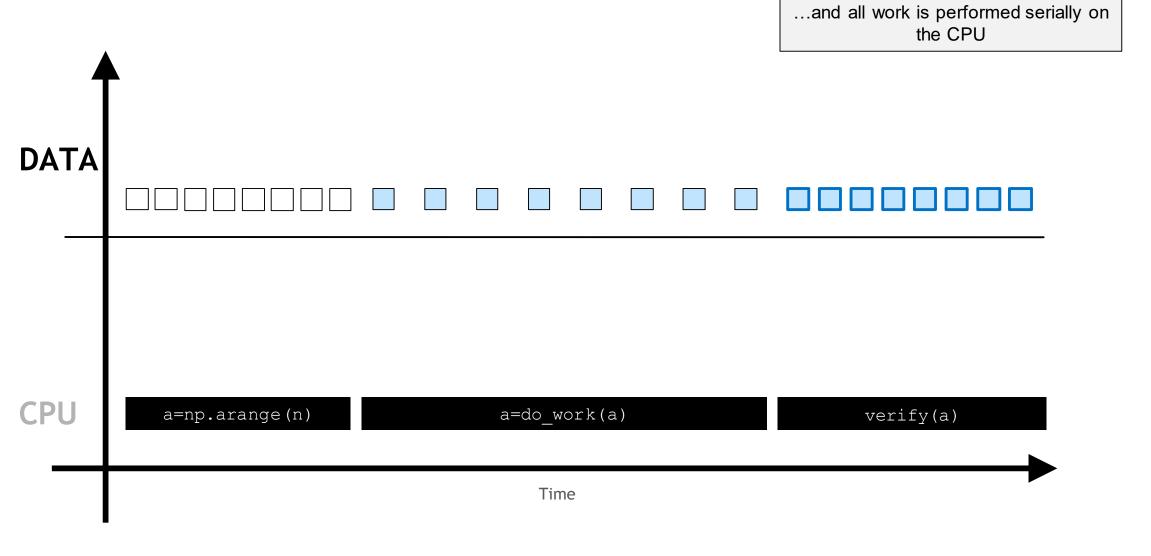
GPU-accelerated vs. CPU-only Applications

In CPU-only applications data is allocated on the CPU **DATA** a=np.arange(n) Time







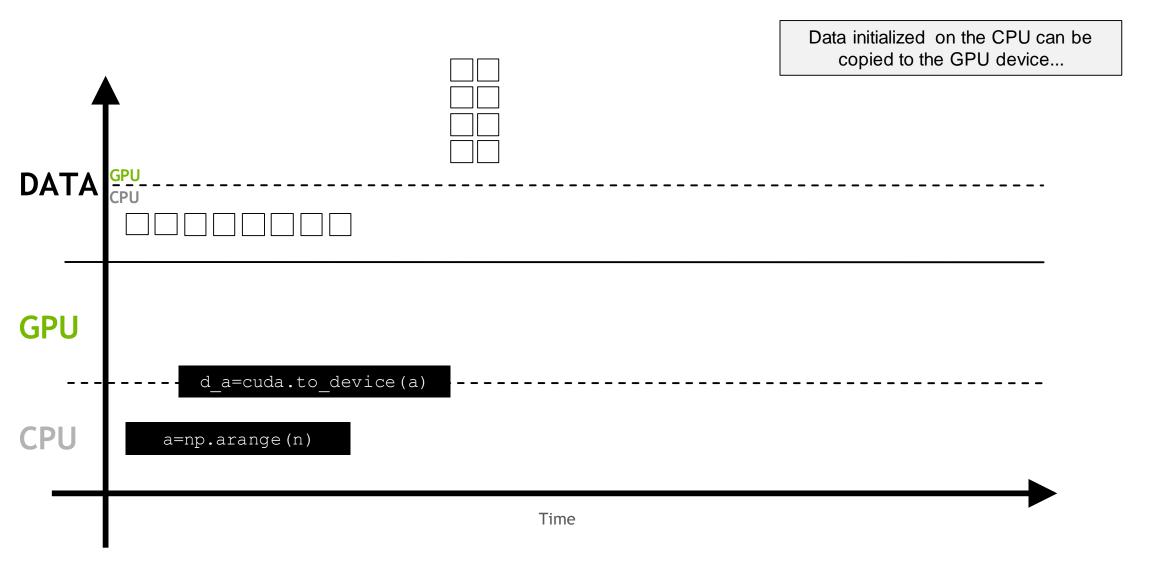


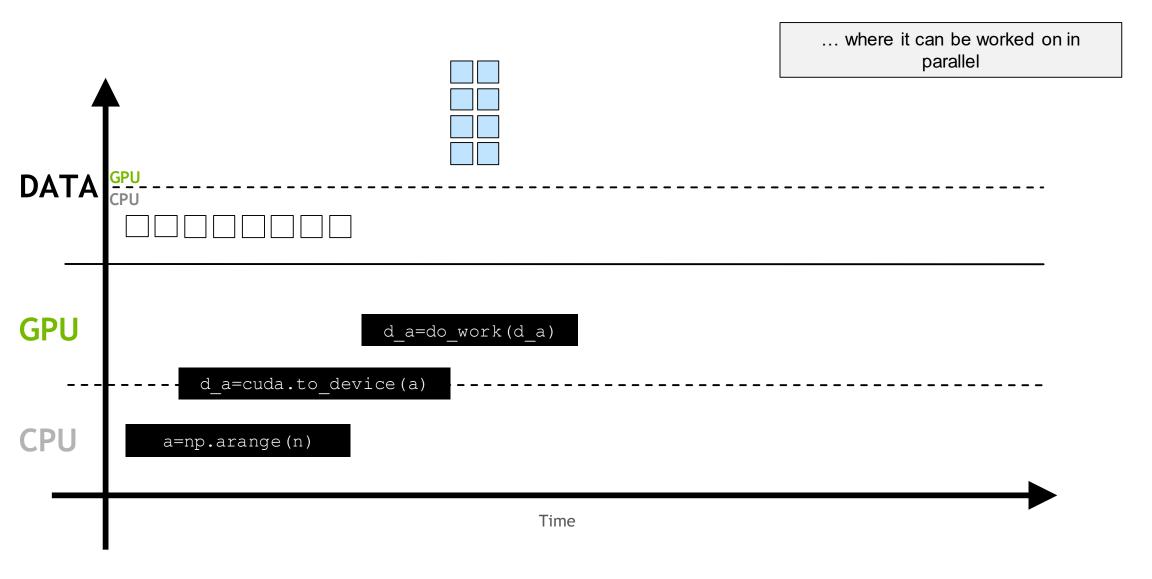


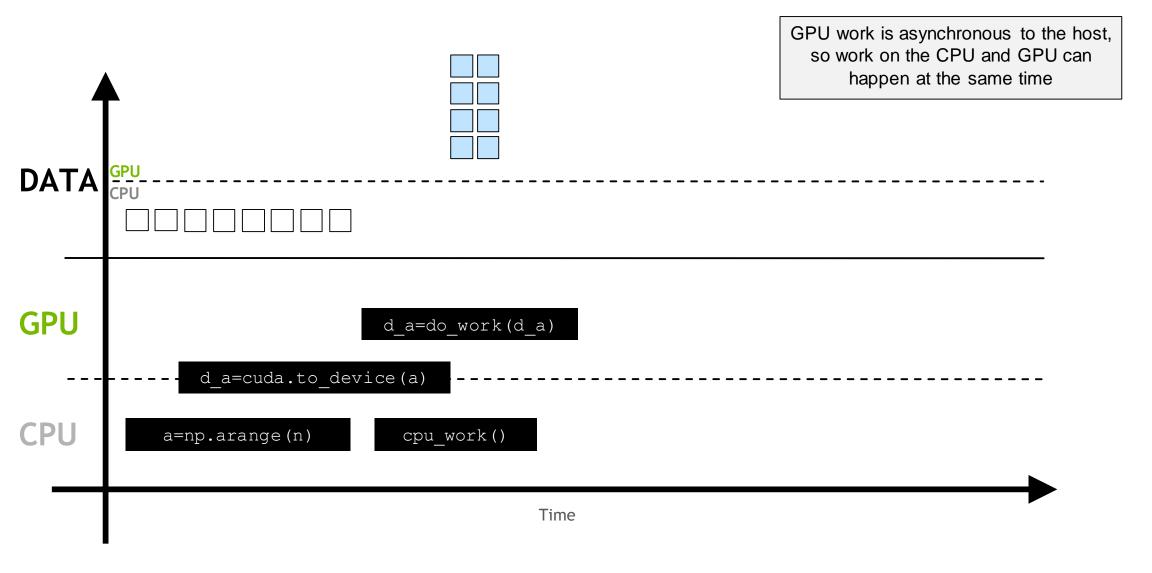
both host and device memory. **DATA GPU** a=np.arange(n) Time

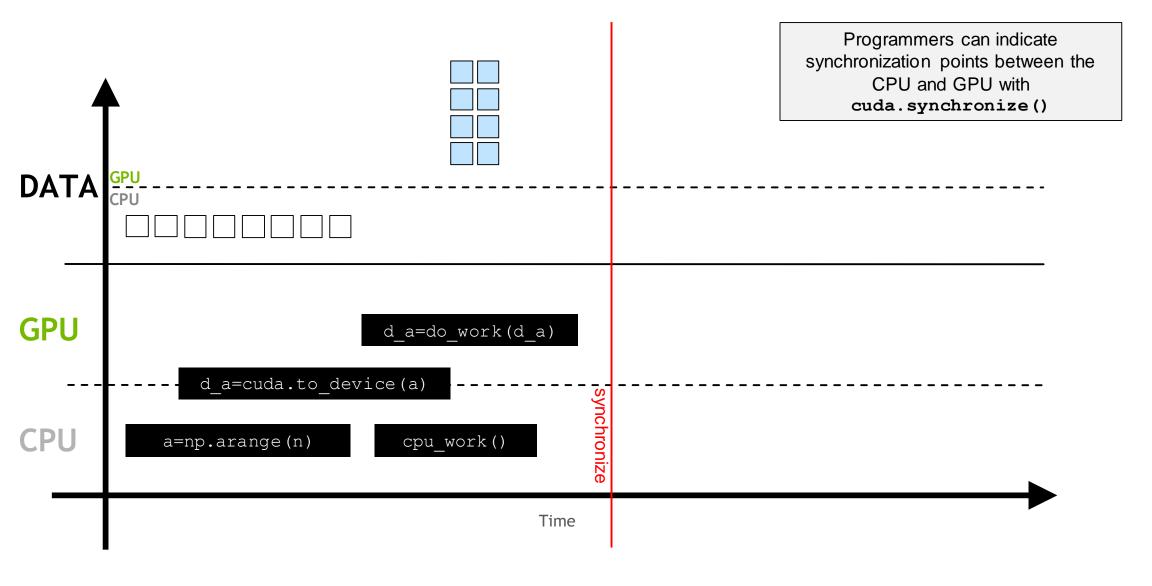


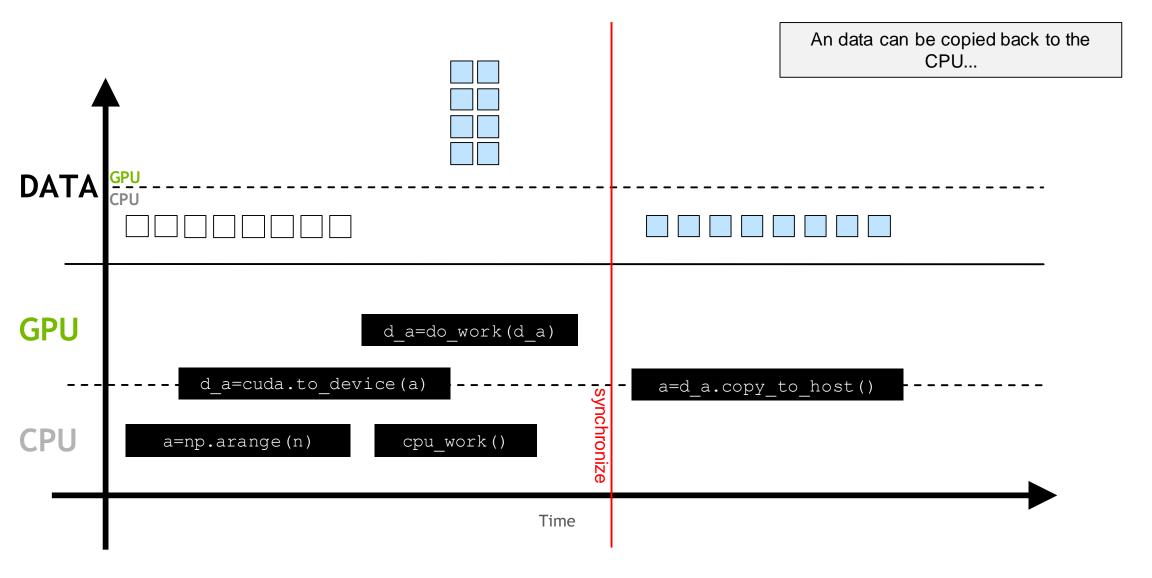
In accelerated applications there is

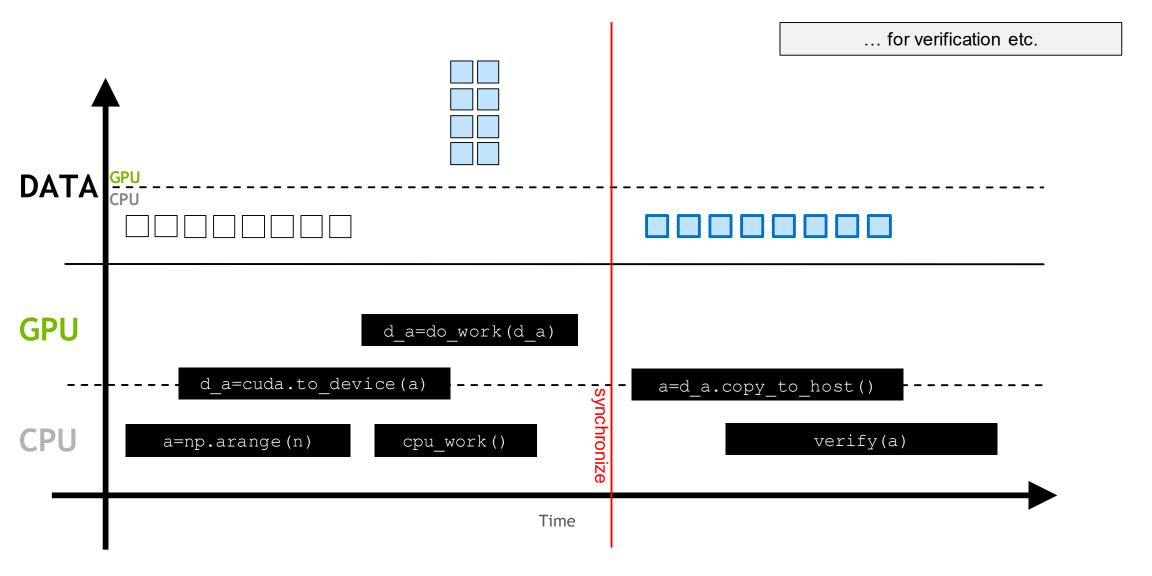




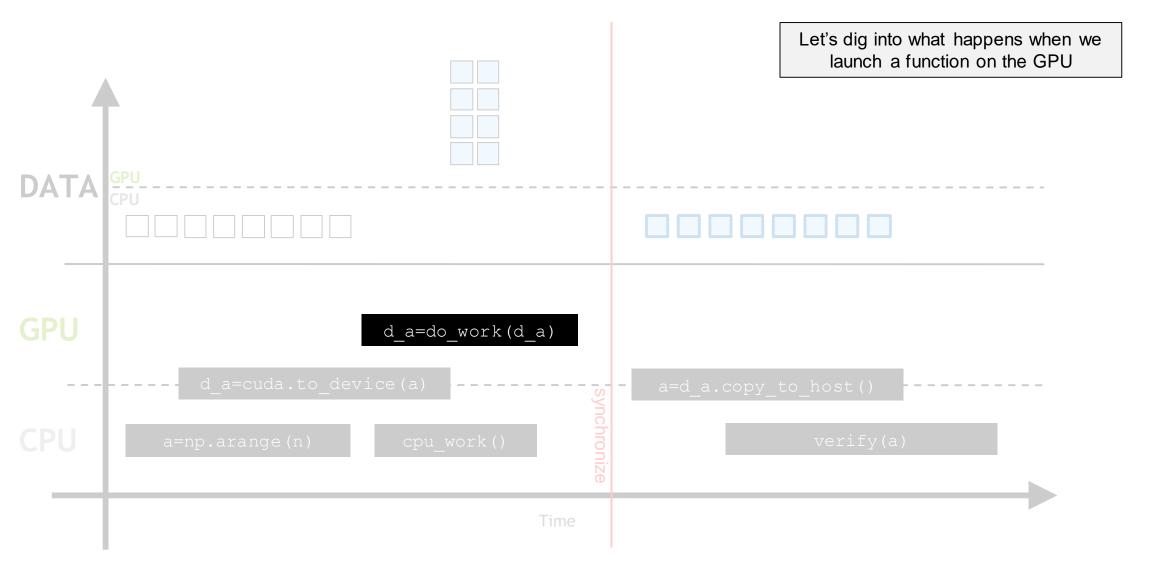




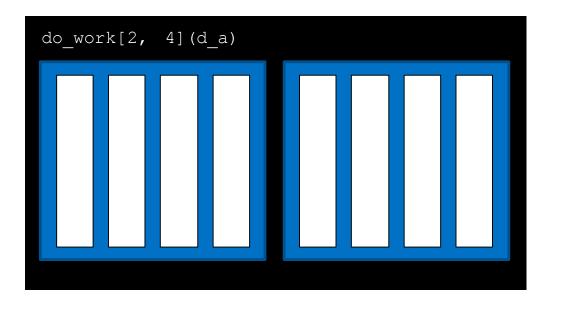


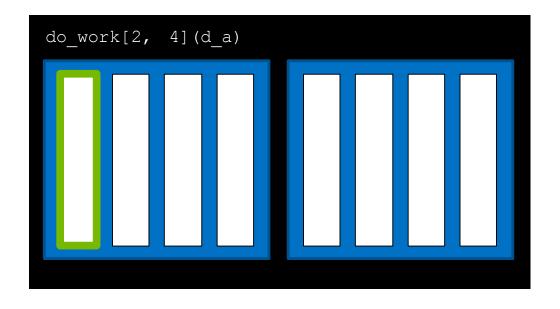


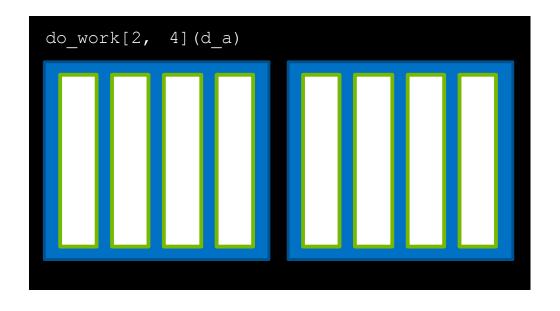
CUDA Thread Hierarchy



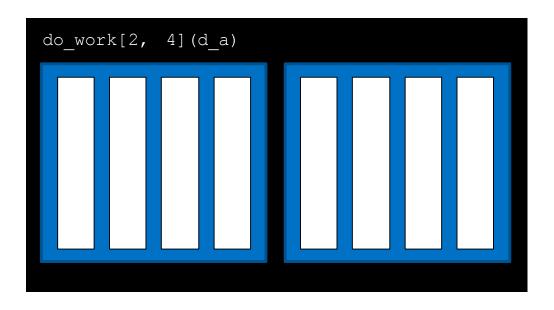


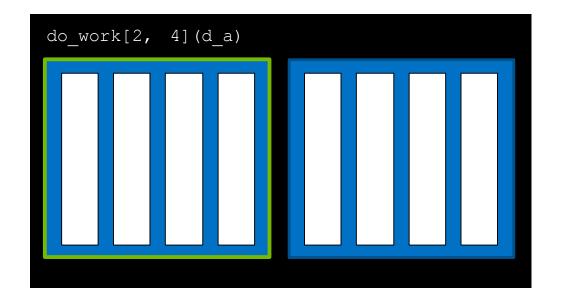


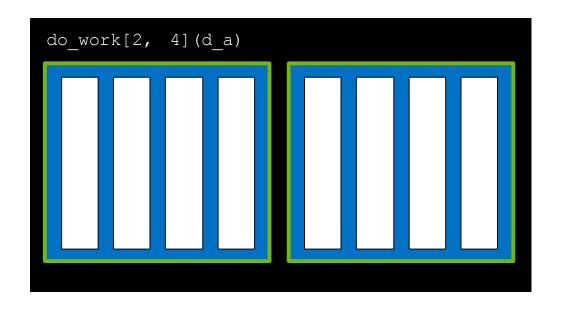


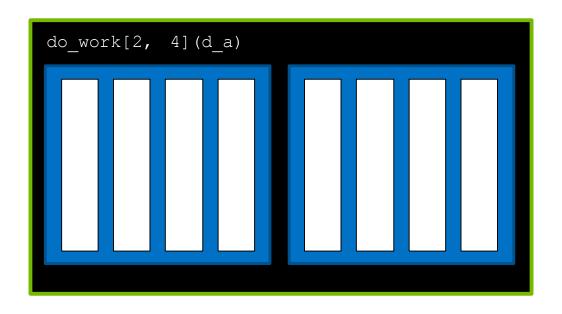


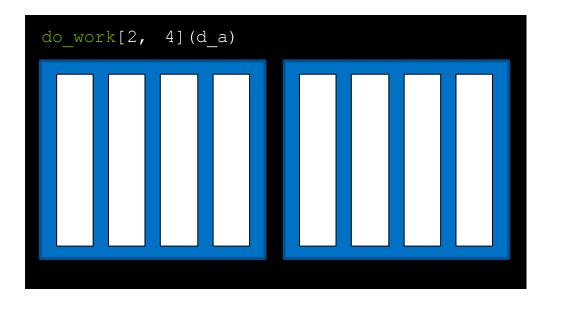
CUDA can process thousands of threads in parallel. The sizes are greatly reduced in these images for simplicity.



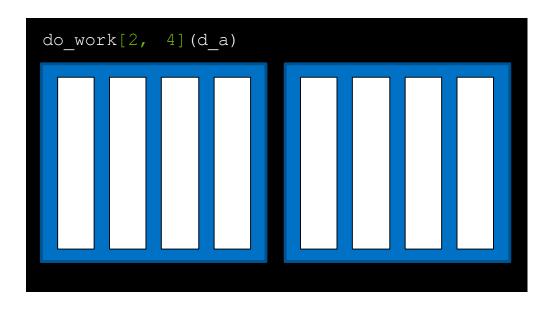




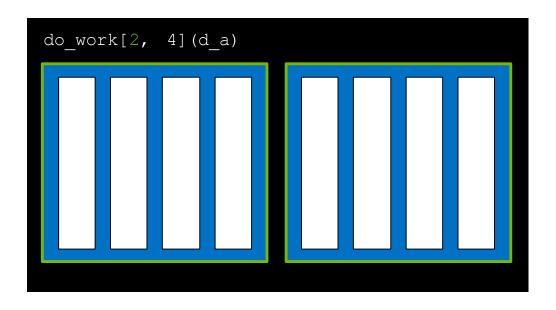


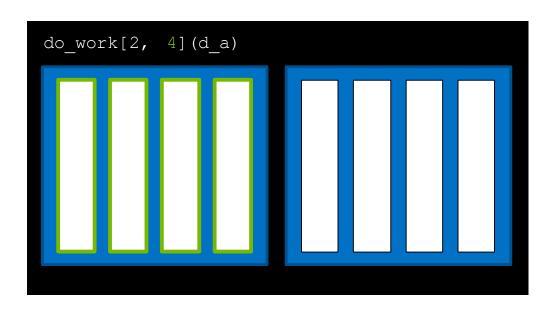


Kernels are **launched** with an **execution configuration**

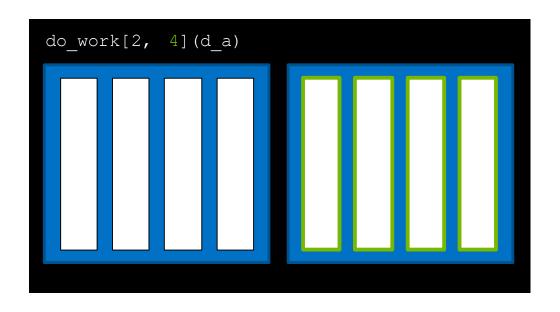






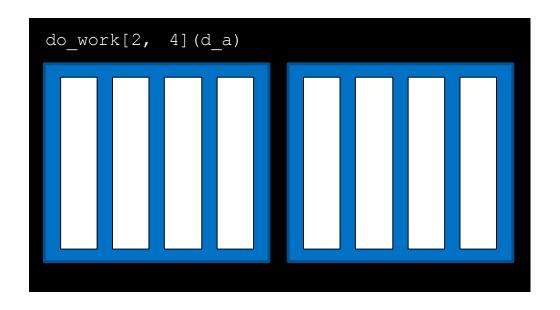




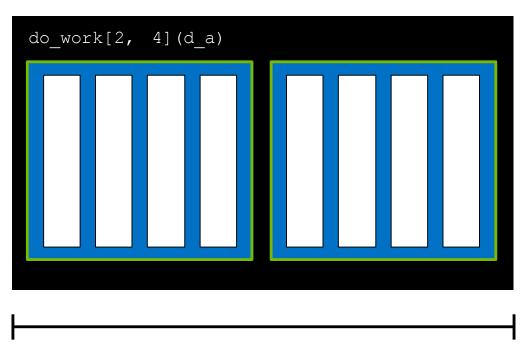


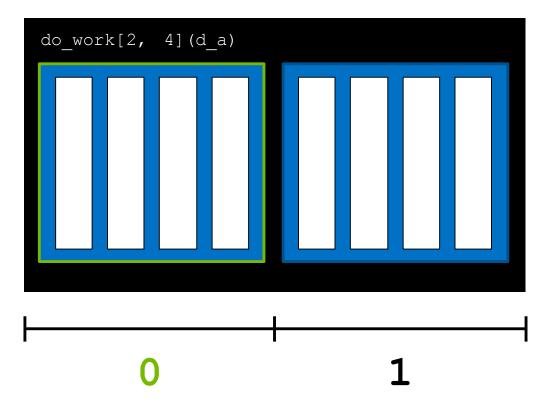
CUDA-Provided Thread Hierarchy Variables

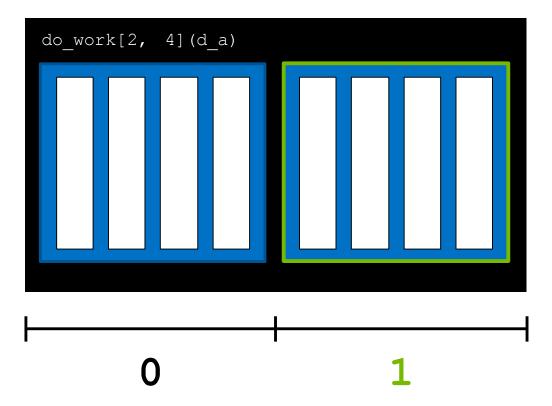
Inside kernel definitions, CUDAprovided variables describe its executing thread, block, and grid



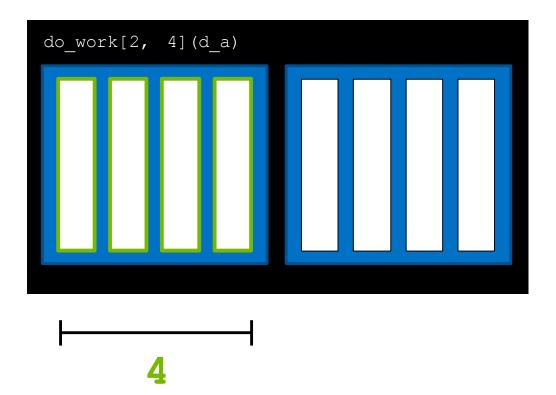
gridDim.x is the number of blocks in
the grid, in this case 2

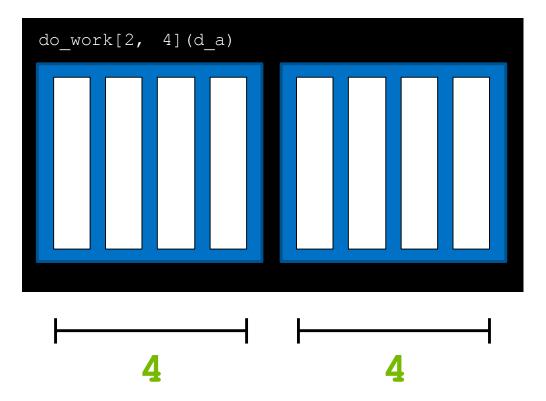


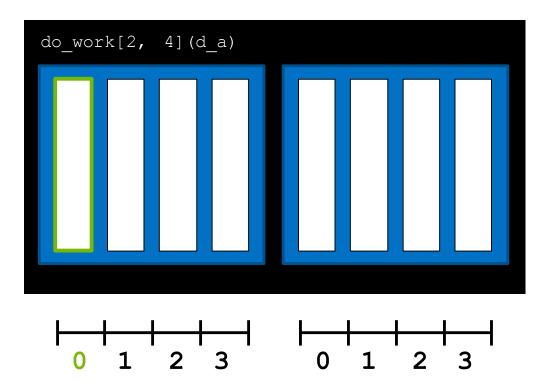


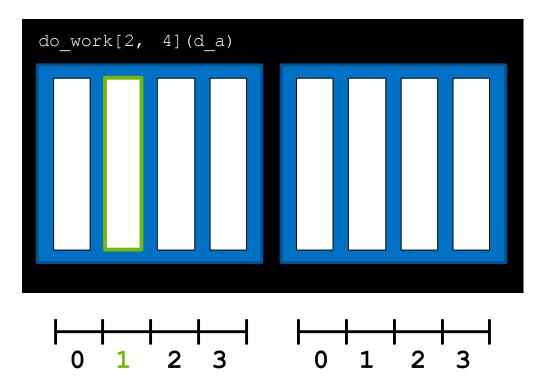


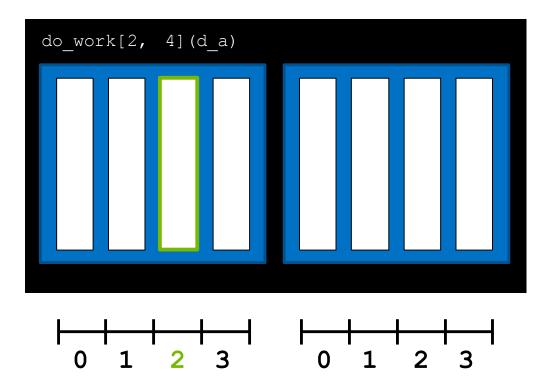
Inside a kernel **blockDim.x** describes the number of threads in a block. In this case **4**

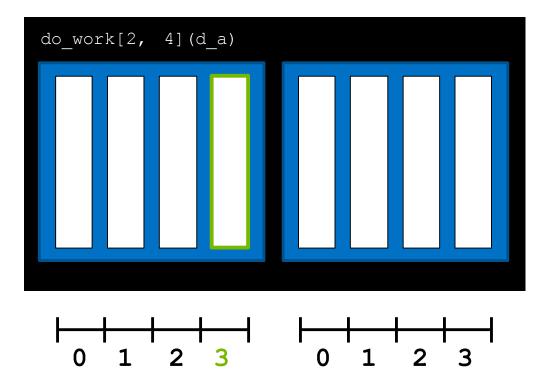


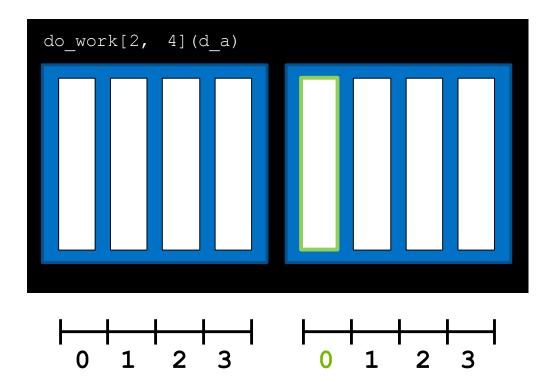


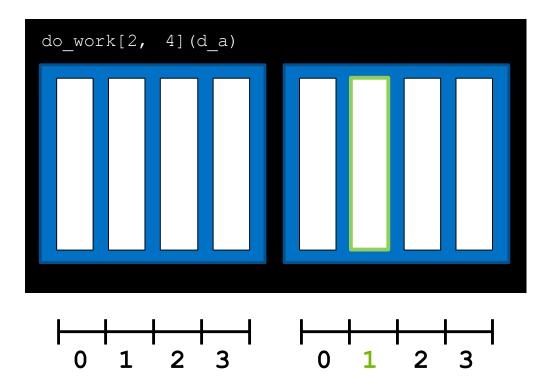


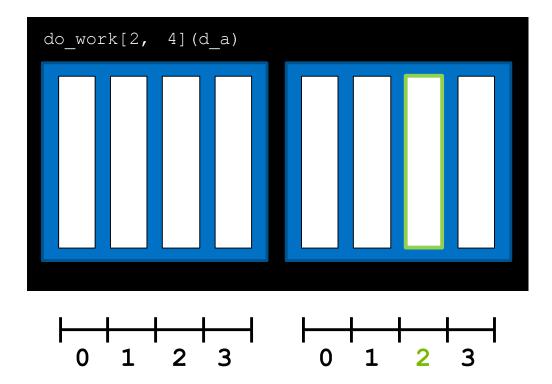


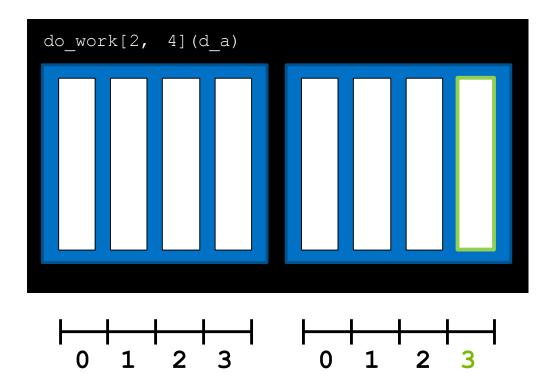




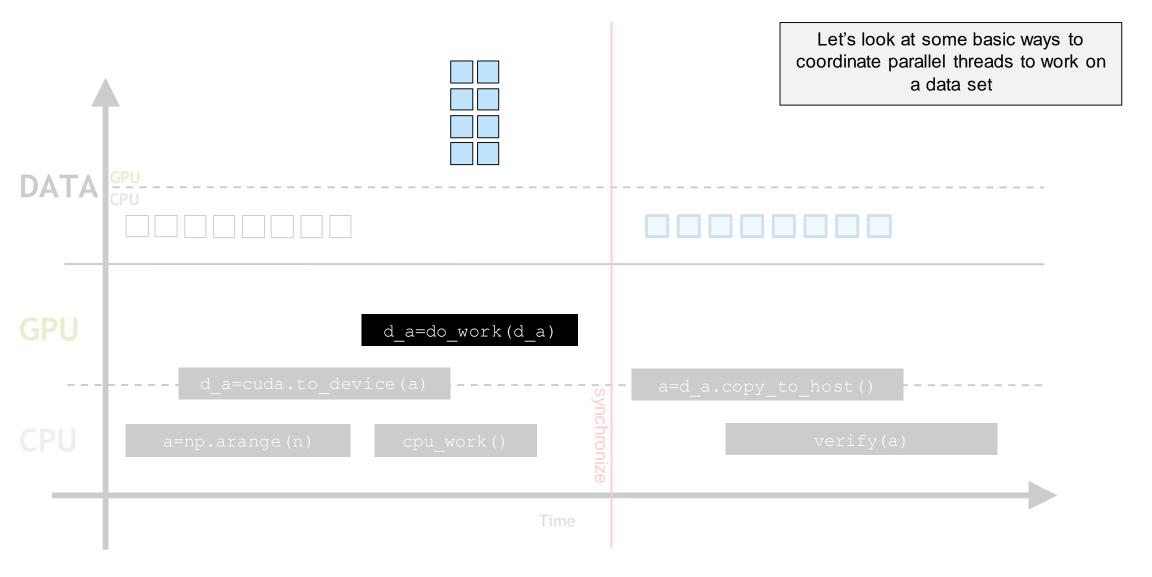




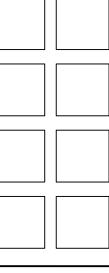


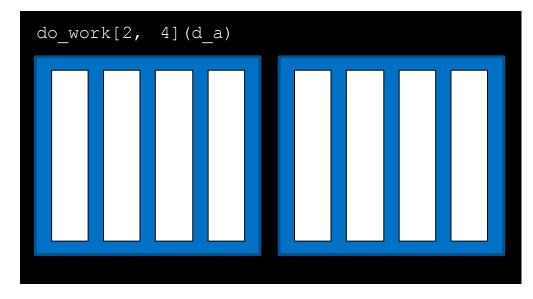


Coordinating Parallel Threads









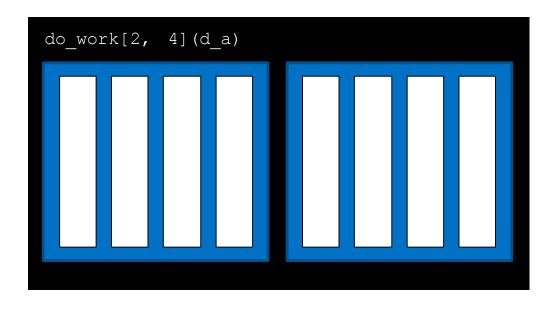


0 4

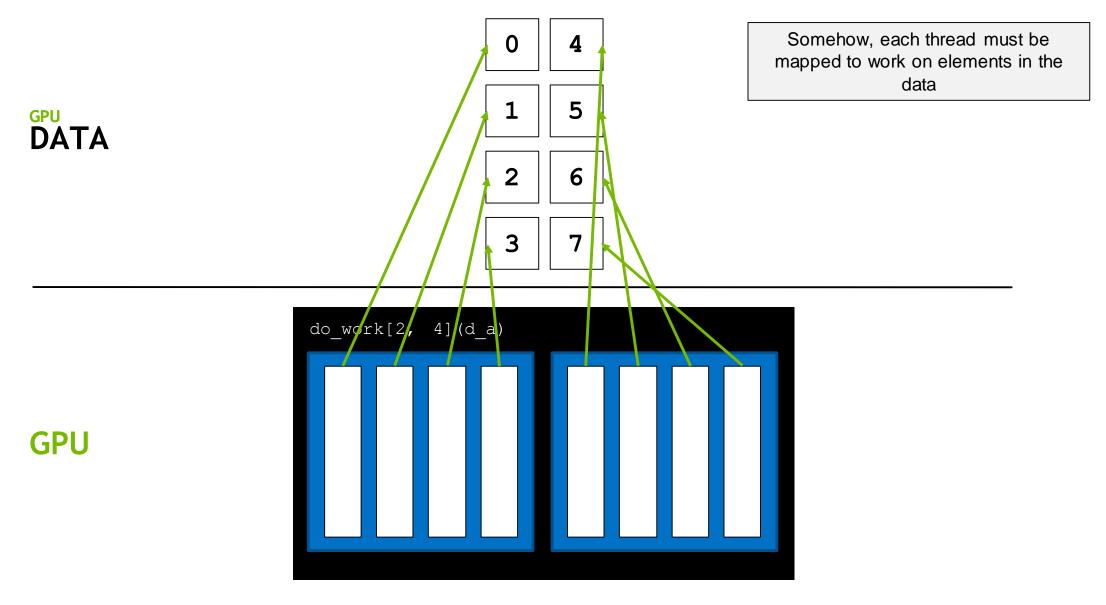
1 | 5

2 | 6

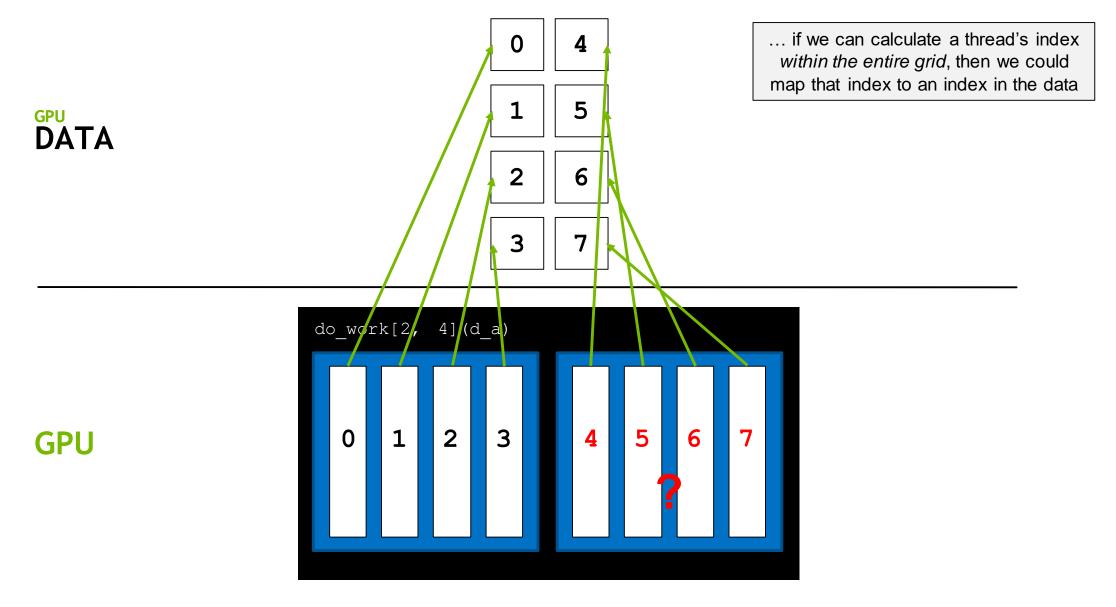
3 |



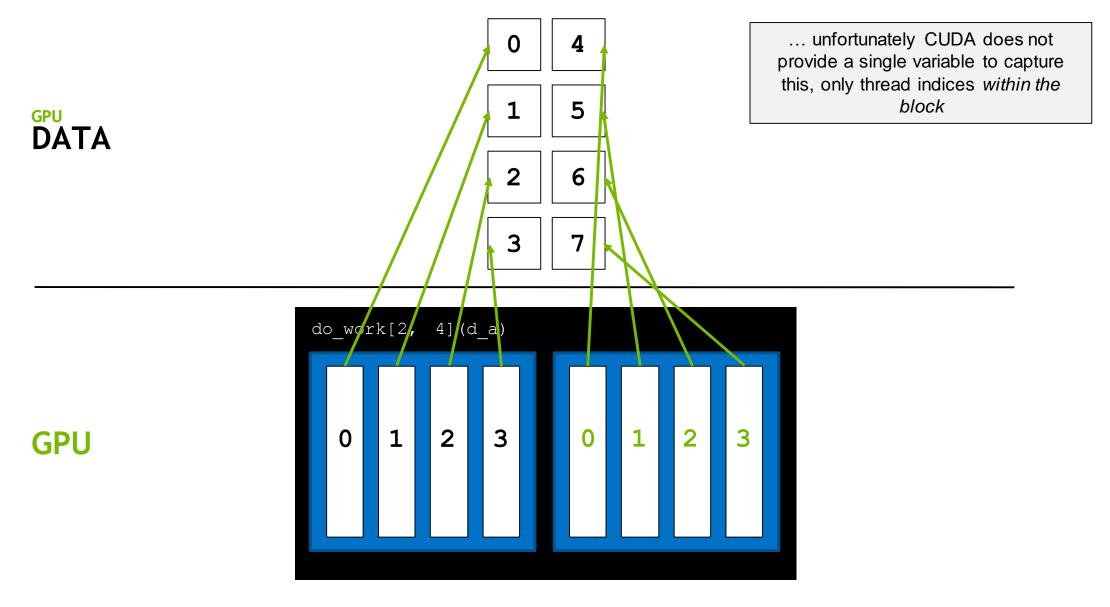












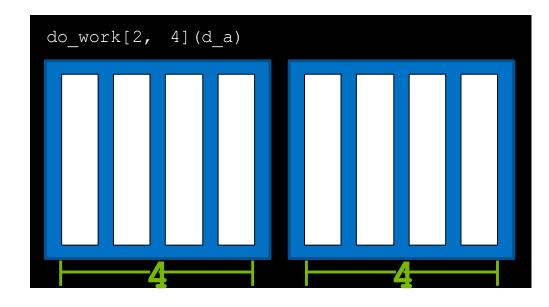
0 | 4

1 || 5

2 | 6

3 || 3

There is an idiomatic way to calculate this value, however. Recall that each thread has access to the size of its block via blockDim.x





GPU DATA 0 | 4

...and the index of its block within the grid via blockIdx.x

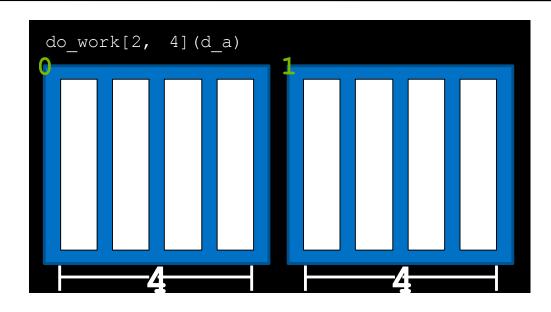
1 | 5

2

6

3

7





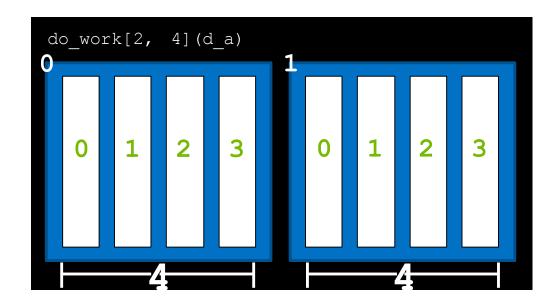
GPU DATA 0 | 4

1 5

2 | 6

3 || .

...and its own index within its block via threadIdx.x





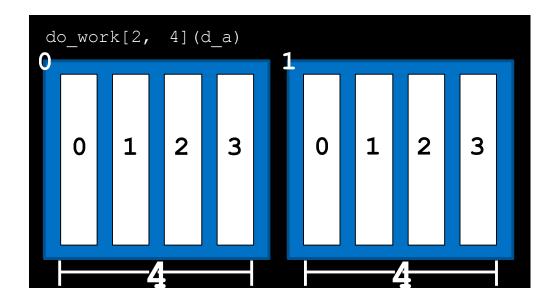
0 | 4

1 || 5

2 | 6

3 || .

Using these variables, the formula threadIdx.x + blockIdx.x * blockDim.x will return the thread's unique index in the whole grid, which we can then map to data elements.

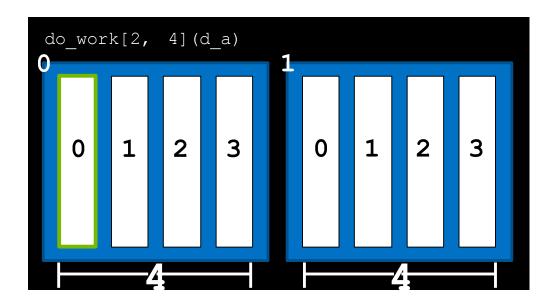


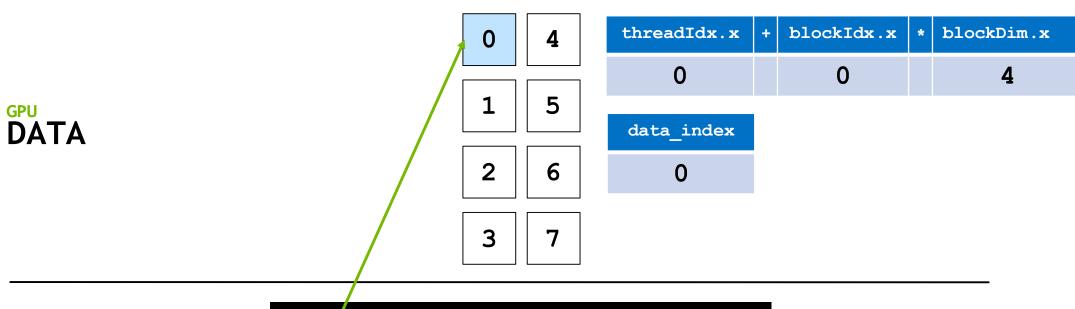


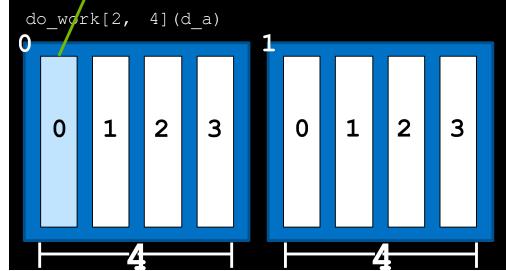
0 | 4

threadIdx.x + blockIdx.x * blockDim.x

data_index









0 4

blockIdx.x threadIdx.x + blockDim.x

0

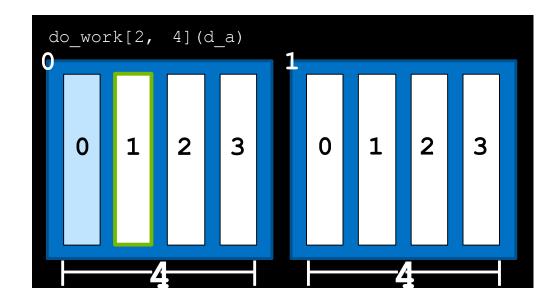
5

data_index

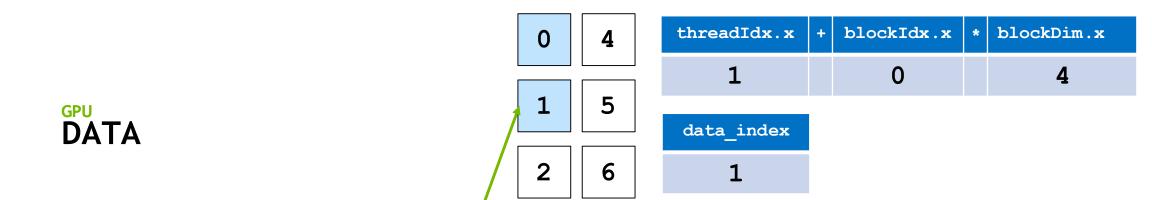
6

3

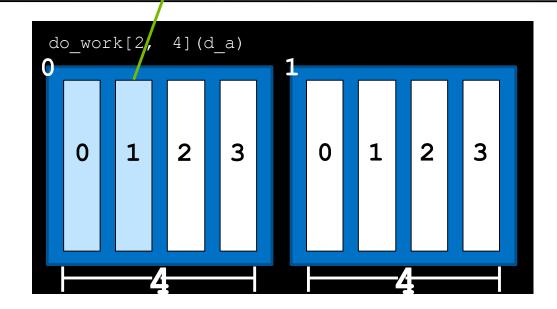
7







3





GPU

0 4

2

blockIdx.x threadIdx.x + blockDim.x

0

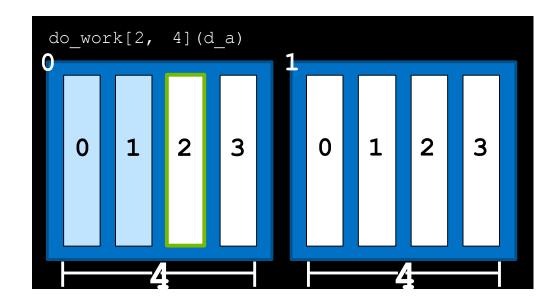
5

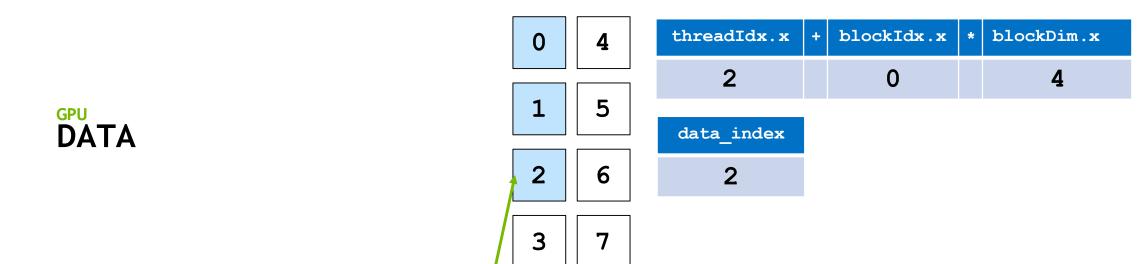
data_index

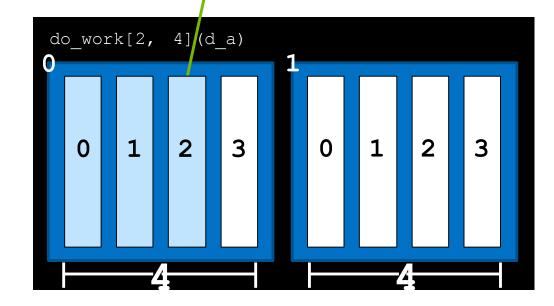
6

3

7









0 4

3

blockIdx.x threadIdx.x + blockDim.x

0

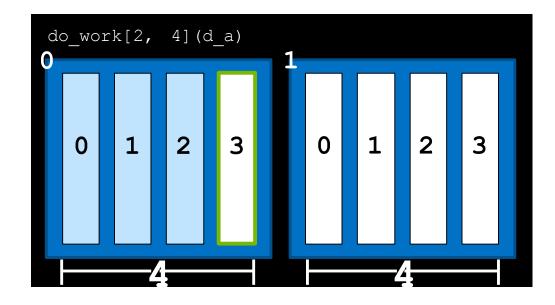
5

data_index

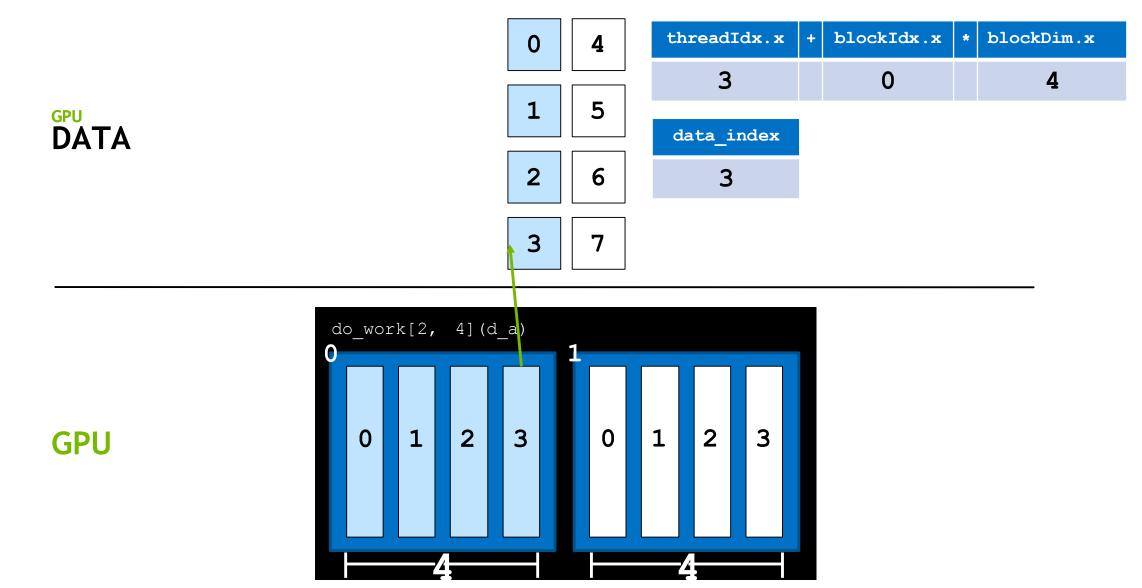
6

3

7









0 4

0

threadIdx.x + blockIdx.x * blockDim.x

1

5

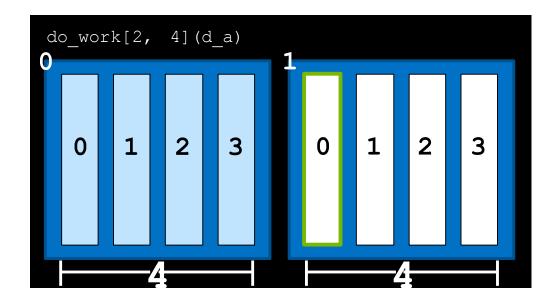
data_index

2

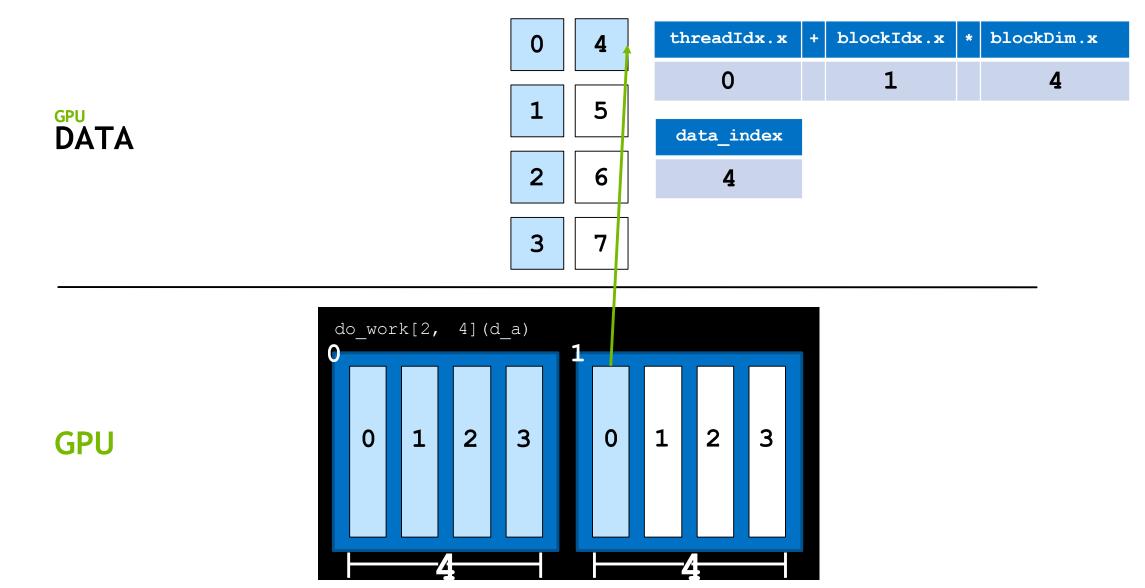
6

3

7









045

data_index

threadIdx.x +

blockIdx.x

blockDim.x

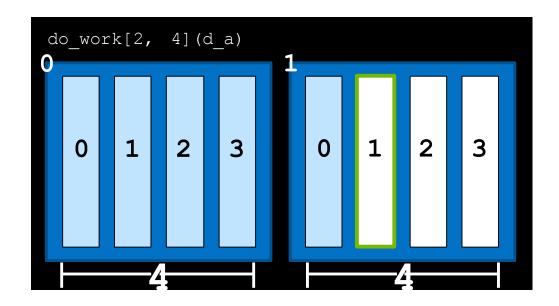
2

6

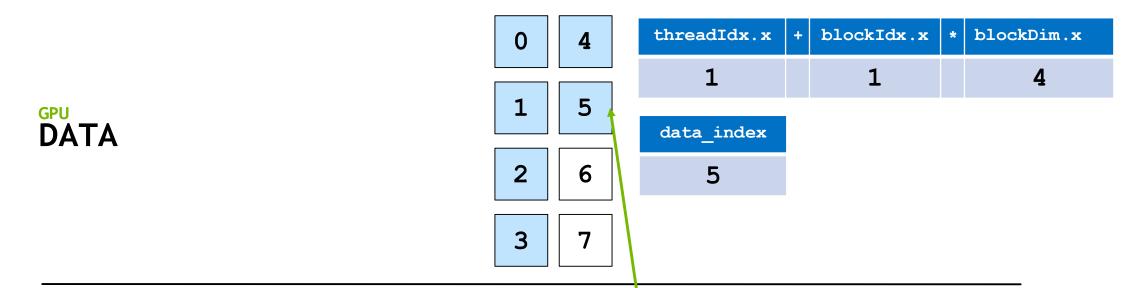
?

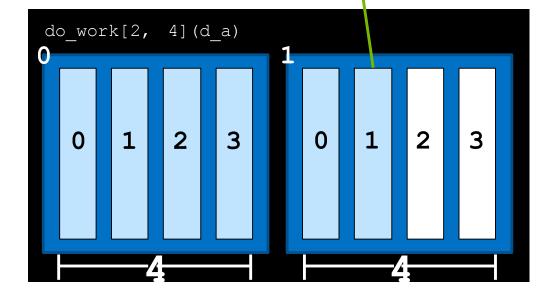
3

7











0 4

2

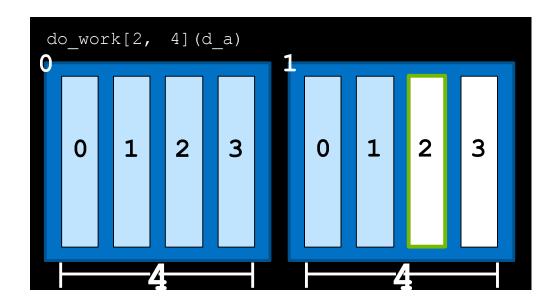
blockIdx.x threadIdx.x + blockDim.x

5

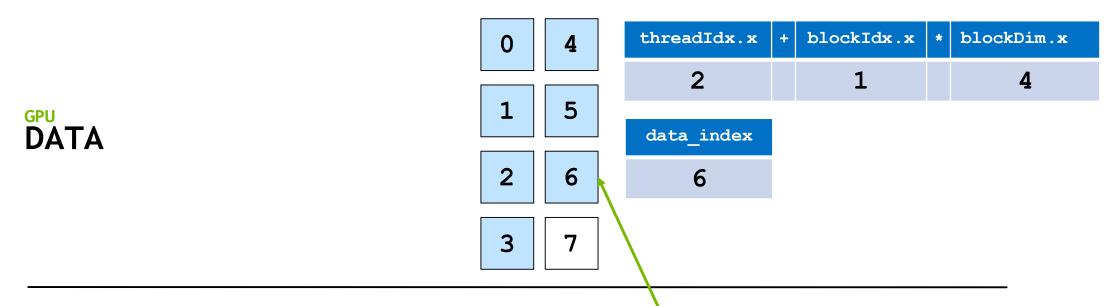
data_index

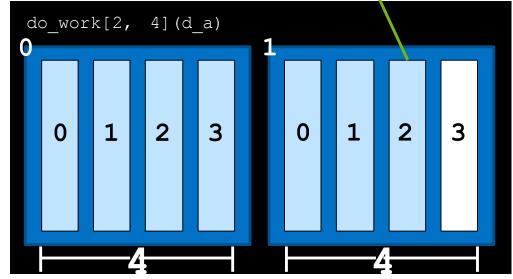
6

3











0 4

3

threadIdx.x + blockIdx.x * blockDim.x

1

5

data_index

2

6

3

7

