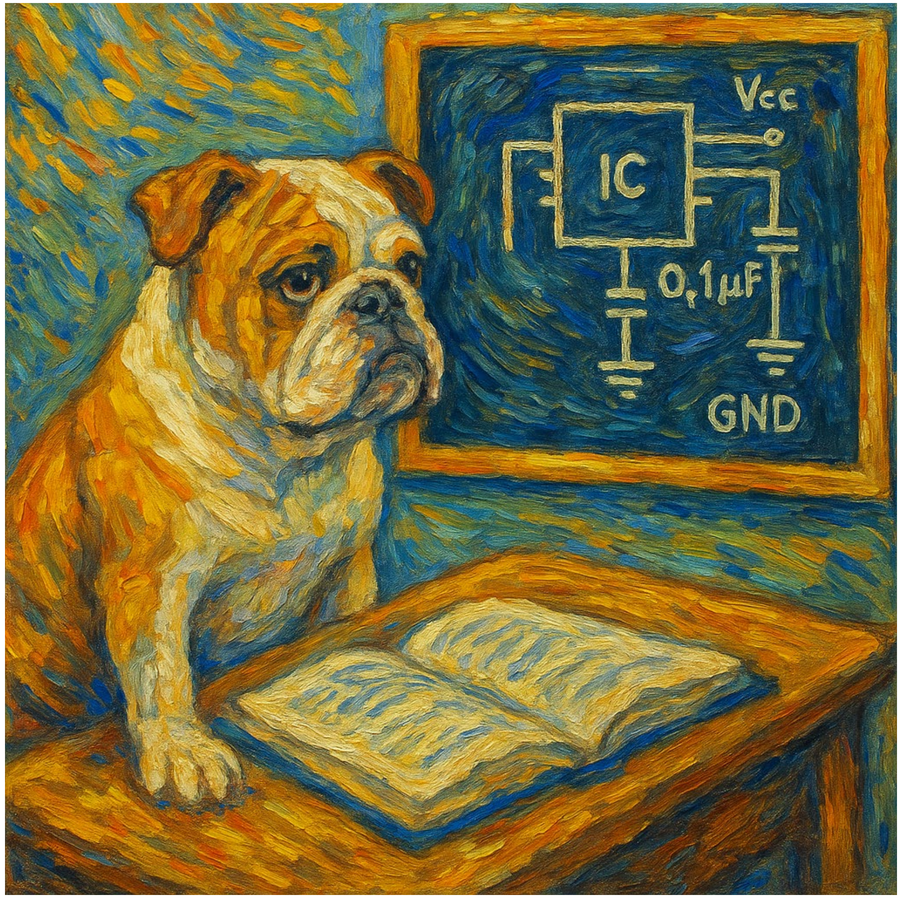
Hands-on PCB Design and Electronic Prototyping with Autodesk Fusion

SUMMER ENRICHMENT- LYLES COLLEGE OF ENGINEERING

REVISION 1.0

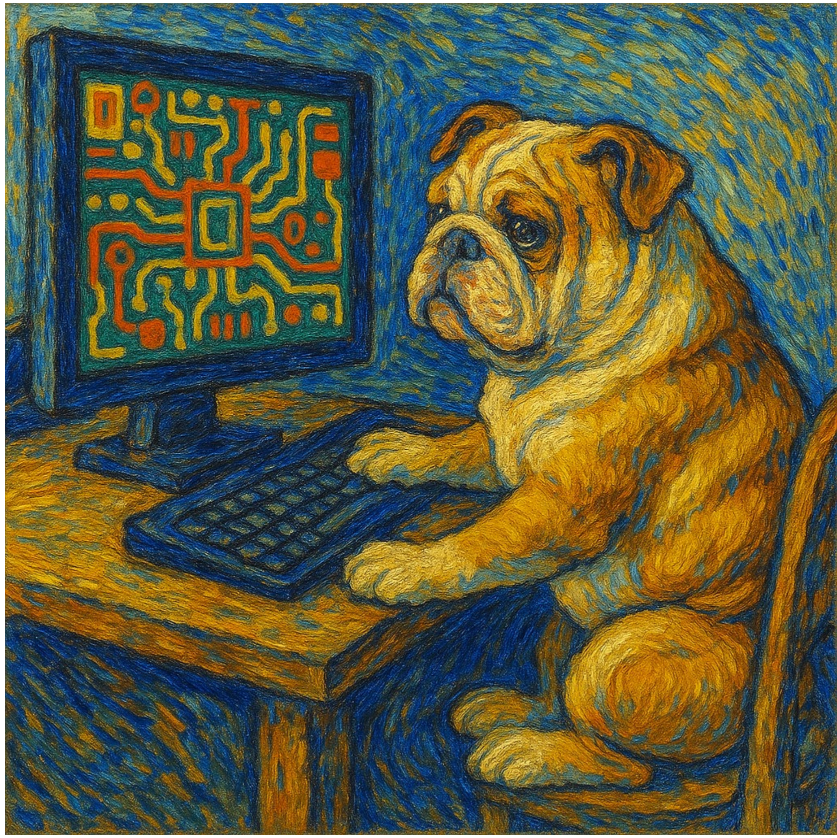
Day 3 Review

- Advanced Schematic Techniques
  - Complex Schematics
    - Creating custom symbols and parts
    - Hierarchical and modular schematic designs
  - Schematic Validation
    - Error checking and electrical rule checking (ERC)
  - Hands-on Activity
    - Creating a schematic for a Raspberry Pi Expansion Card



Day 4: PCB Layout Essentials (Part 1)

- Transitioning from Schematic to PCB
  - Generating PCB from schematic
  - Understanding PCB workspace and tools
- Component Placement
  - Placement strategies (signal integrity, EMI/EMC, thermal considerations)
  - Floor-planning
- Hands-on Activity
  - Component placement for a simple project PCB

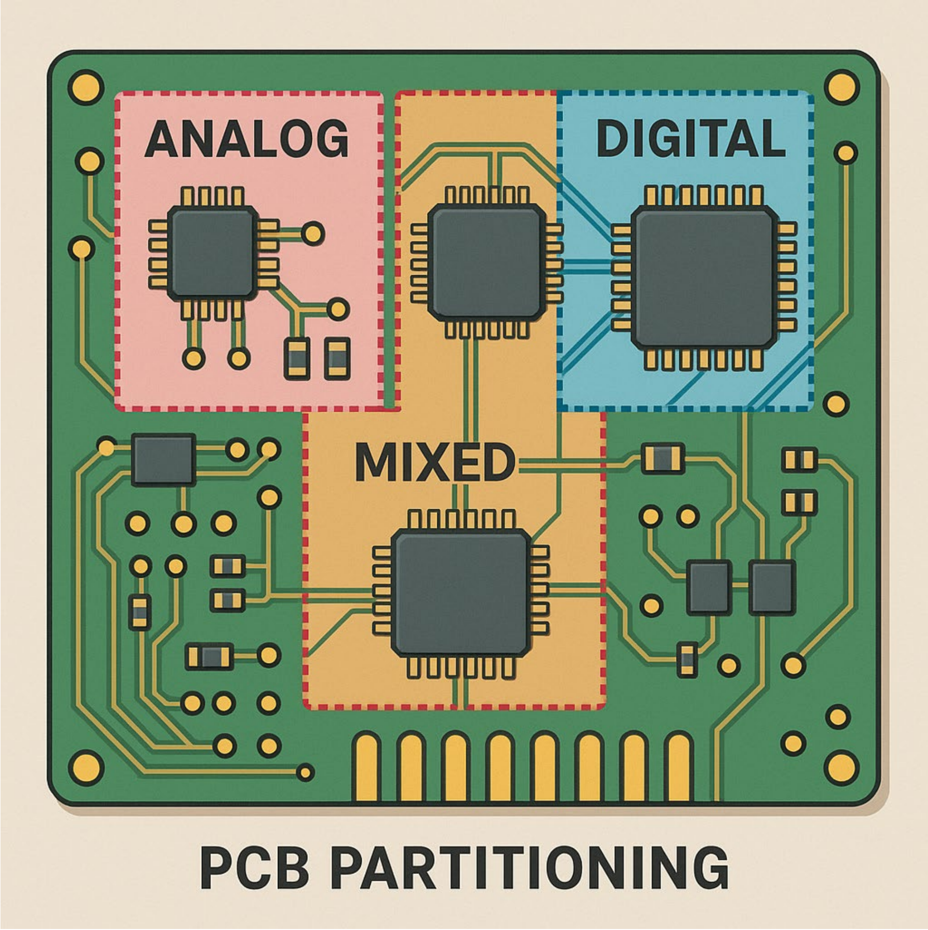


Some PCB Layout Resources

- Application Notes
  - https://www.nxp.com/docs/en/application-note/AN3962.pdf
- Linear Design Handbook
  - https://www.analog.com/en/resources/technical-books/linear-circuit-design-handbook.html
- Engineering Standards
  - IPC-2221 (Generic Standard on Printed Board Design)- Published by: IPC (Association Connecting Electronics Industries)
    - **Use:** The most widely accepted standard for calculating PCB trace widths.
  - IPC-2152 (Standard for Determining Current-Carrying Capacity in Printed Board Design)
    - **Use:** Supersedes some parts of IPC-2221 with more accurate data based on empirical testing.
- GitHub
  - https://github.com/RogerMoore2/

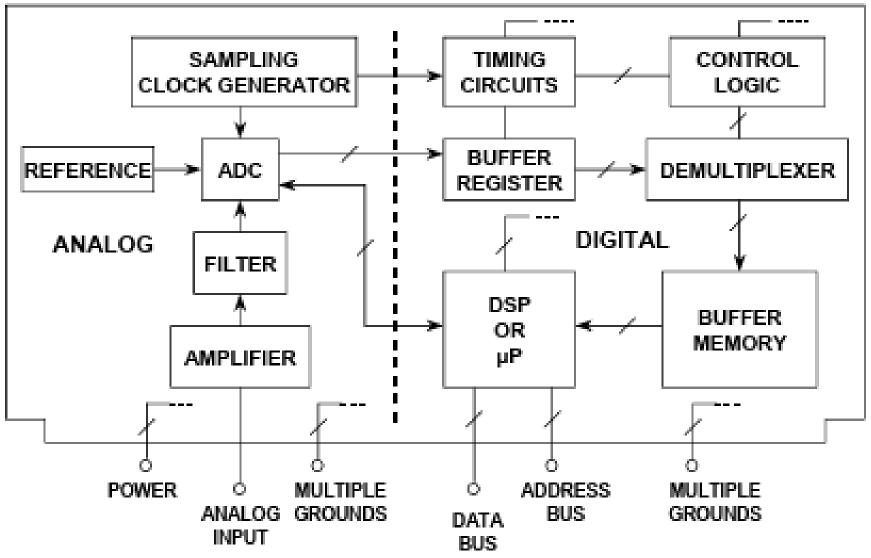
PCB Partitioning

- Definition:
  - The logical grouping and electrical separation of different circuit sections based on functionality
- Examples of partitioning blocks:
  - power supply
  - Analog
  - Digital
  - RF
- Purpose:
  - Improve signal integrity
  - Reduce electromagnetic interference (EMI)
  - Prevent crosstalk between sensitive and noisy signals
  - Simplify design troubleshooting.



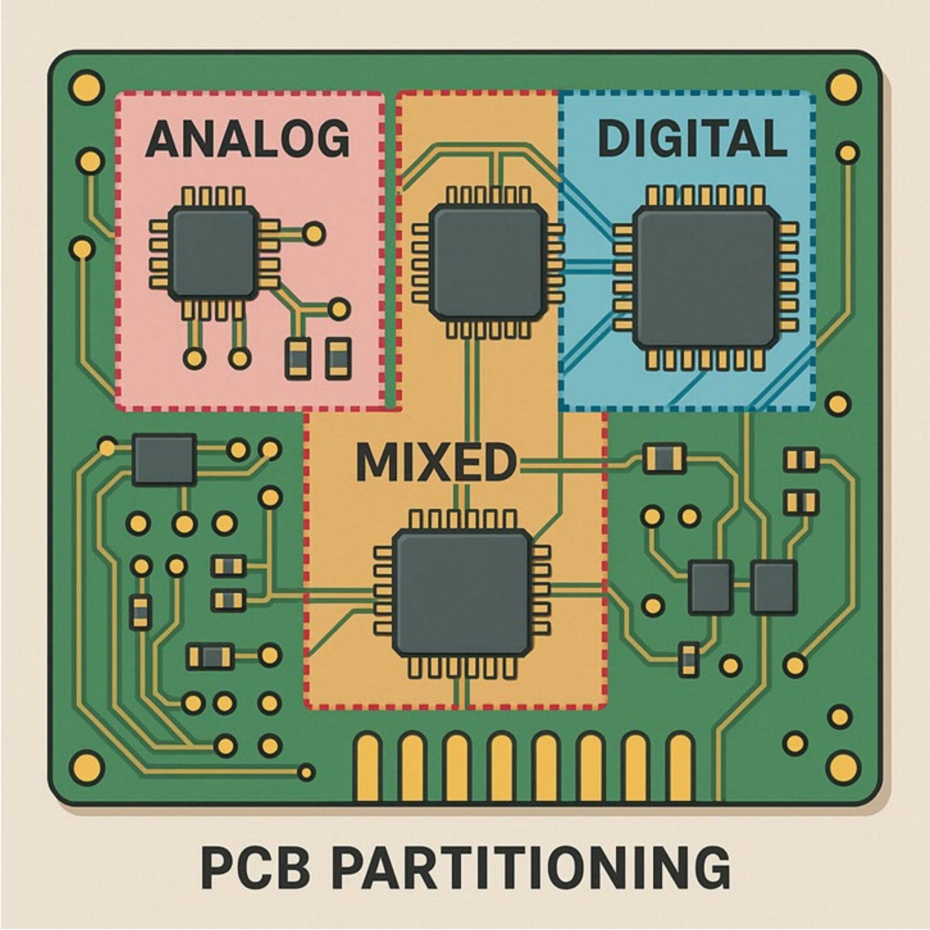
PCB Partitioning (continued)

- Key Characteristics:
  - Focuses on functional separation
  - Often uses ground islands or planes to isolate blocks
  - Dictates placement constraints for floor planning
  - Heavily influences routing strategies
- Analogy:
  - Like zoning in city planning — separating industrial, residential, and commercial areas to avoid conflict and ensure safety.



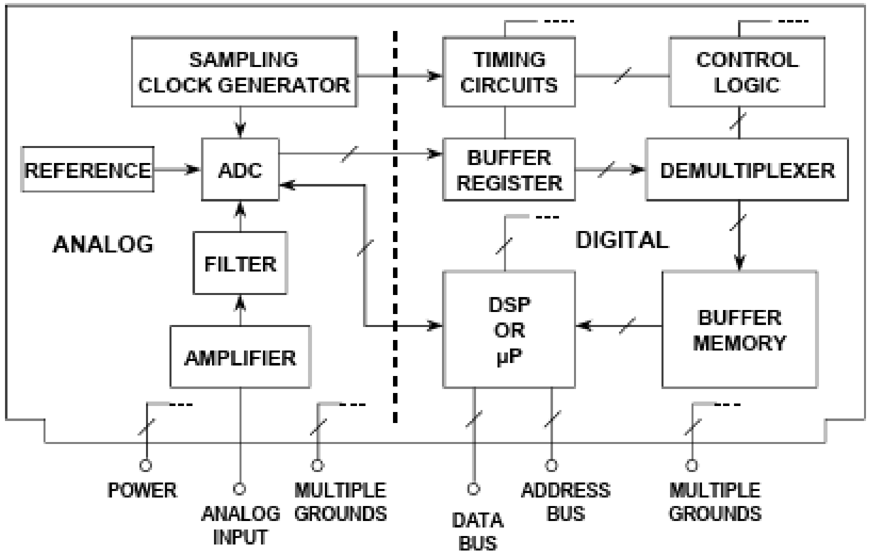
PCB Partitioning- Best Practices

- The following practices will help you design cleaner, more reliable boards.
  - Divide by Function
    - Group circuits by functionality: digital, analog, power, RF, high-speed, etc.
    - Keep noisy sections (e.g., switching regulators, microcontrollers) away from sensitive analog or RF areas.
    - Use silkscreen labels or bounding boxes to visually separate functional zones.
  - Isolate High-Speed & High-Current Paths
    - Keep high-frequency and high-current paths isolated to reduce EMI.
    - Avoid routing them through analog or control regions.
  - Separate Ground & Power Planes
    - Use separate ground planes or islands for analog and digital circuits (AGND vs. DGND).
    - Connect grounds at a single point (star grounding) to prevent ground loops and noise coupling.
    - Isolate power domains for analog, digital, and high-power components.



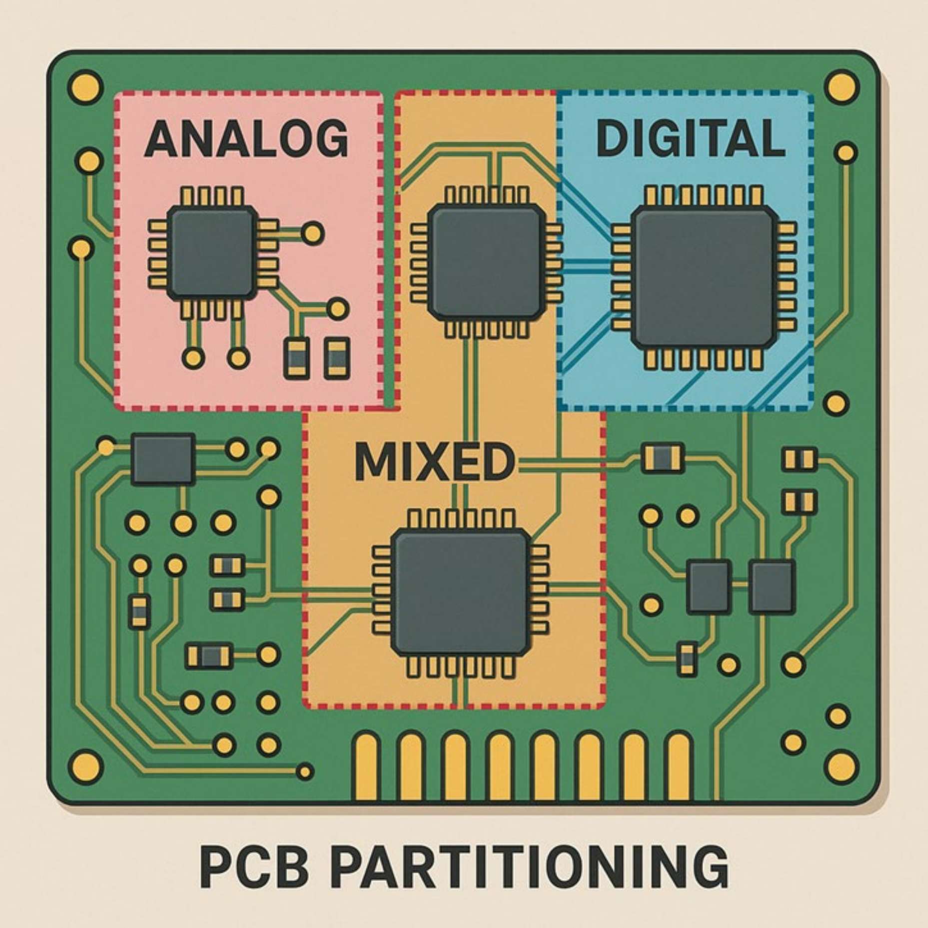
PCB Partitioning- Best Practices (continued)

- Define Clear Signal Flow
  - Arrange partitions to follow logical signal flow (e.g., sensor → ADC → MCU → output).
  - Avoid crisscrossing traces between zones.
  - Keep data direction intuitive to simplify debugging and EMI mitigation.
- Add Physical Separation
  - Use spacing between partitions to:
    - Prevent crosstalk
    - Allow for copper keepouts
    - Enable thermal management
    - Use keepout zones to enforce electrical and mechanical barriers.
- Use Shielding and Guard Traces
  - For analog/RF sections, add guard traces, shielding, or ground fences to isolate from digital noise.
  - Avoid shared return paths with noisy circuits.



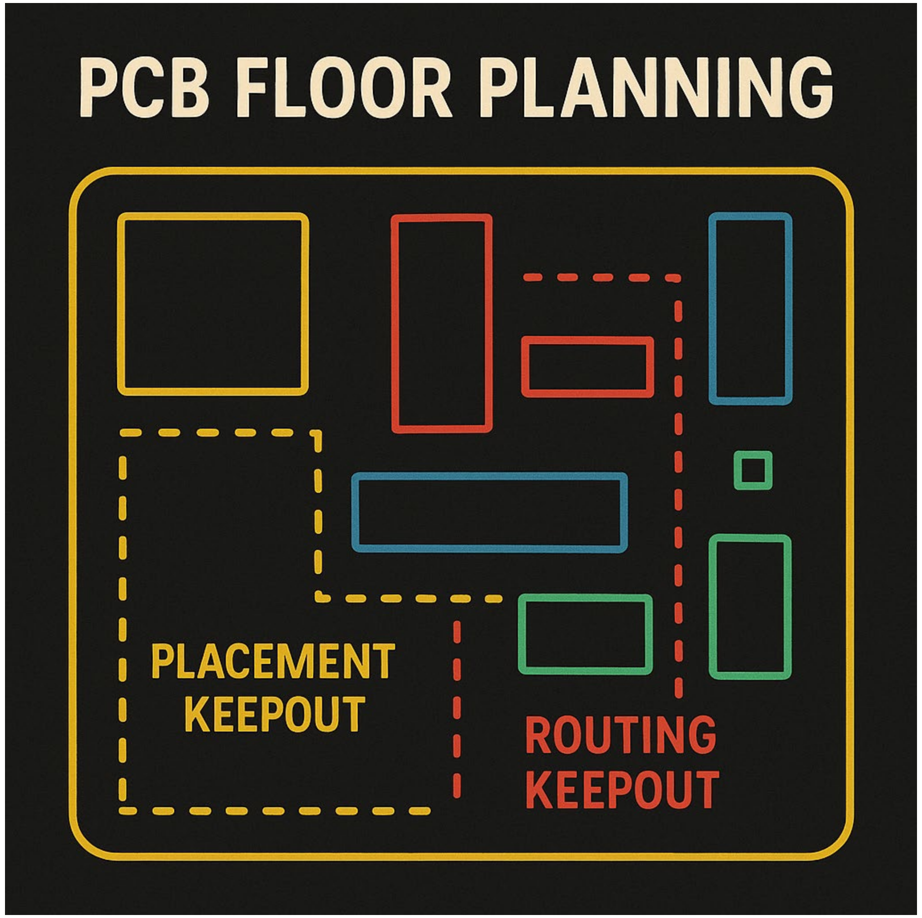
PCB Partitioning- Best Practices (continued)

- Minimize Trace Crossings Between Partitions
  - Reduce the number of traces that cross partitions.
  - If needed, route over controlled impedance layers with proper reference planes.
- Plan for Debugging & Testability
  - Leave test points within each partition.
  - Use headers or jumpers between partitions to allow isolation during testing.
- Thermal Isolation
  - Separate heat-generating components (e.g., power regulators, MOSFETs) from temperature-sensitive analog ICs.
  - Use copper pours and thermal reliefs as thermal boundaries.
- Optional:
  - Use Hierarchical Schematic Design
    - Create one schematic sheet per partition.This improves readability, maintenance, and layout partitioning in CAD tools like Autodesk Fusion.



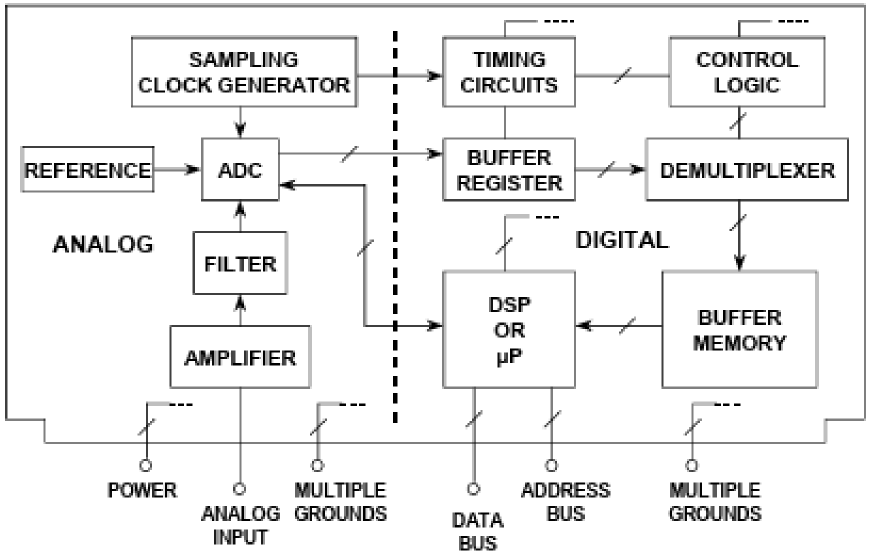
PCB Floor Planning

- Definition:
  - The physical arrangement of all components on a PCB considering electrical, mechanical, thermal, and manufacturability constraints.
- Purpose:
  - Optimize signal flow
  - Minimize trace lengths
  - Ensure thermal efficiency
  - Plan for mechanical fit and mounting
  - Allocate space for routing and vias



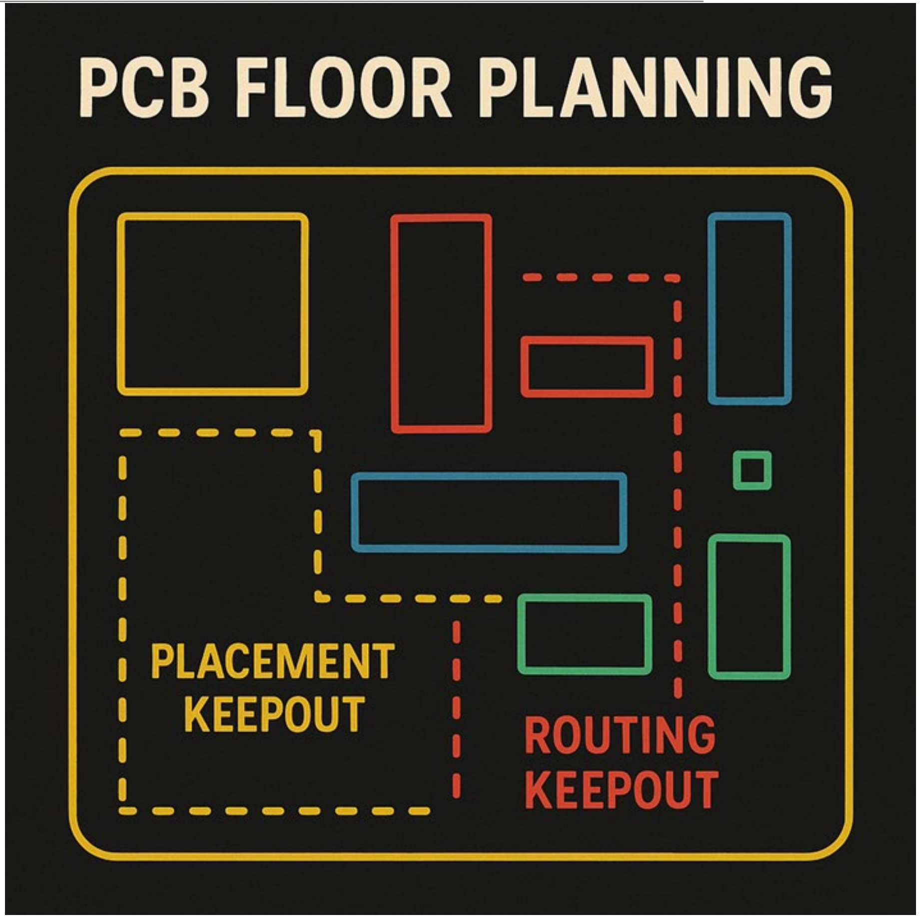
PCB Floor Planning (continued)

- Key Characteristics:
  - Happens early in the layout phase
  - Considers component orientation and placement
  - Involves power, ground, signal paths, connectors, and test points
  - Influenced by enclosure/mechanical design
- Analogy:
  - Like interior design — arranging furniture (components) in rooms (PCB) for best use of space and function.



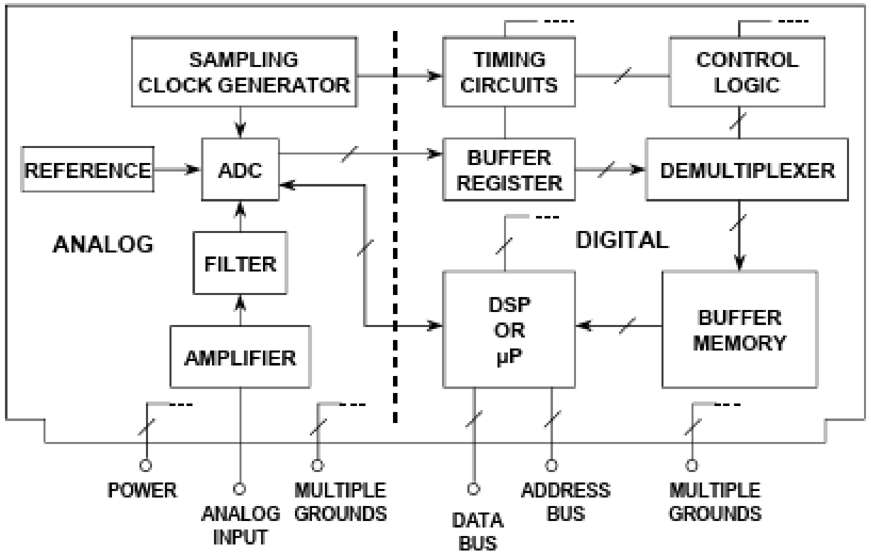
PCB Floor Planning- Best Practices

- Group Components by Functional Blocks
  - Best Practice: Arrange components according to their function (e.g., power regulation, microcontroller, sensors).
    - Why: Easier to debug, reduces signal routing complexity, and enhances clarity in layout.
- Place Connectors and I/O Strategically
  - Best Practice: Locate connectors on edges or where access is logical based on mechanical constraints.
    - Why: Prevents awkward wiring or mechanical interference; helps with enclosure integration.
- Prioritize Power and Ground Routing
  - Best Practice: Route power and ground early. Use wide traces or planes. Keep return paths short.
    - Why: Minimizes noise, voltage drop, and ensures signal integrity and safety.



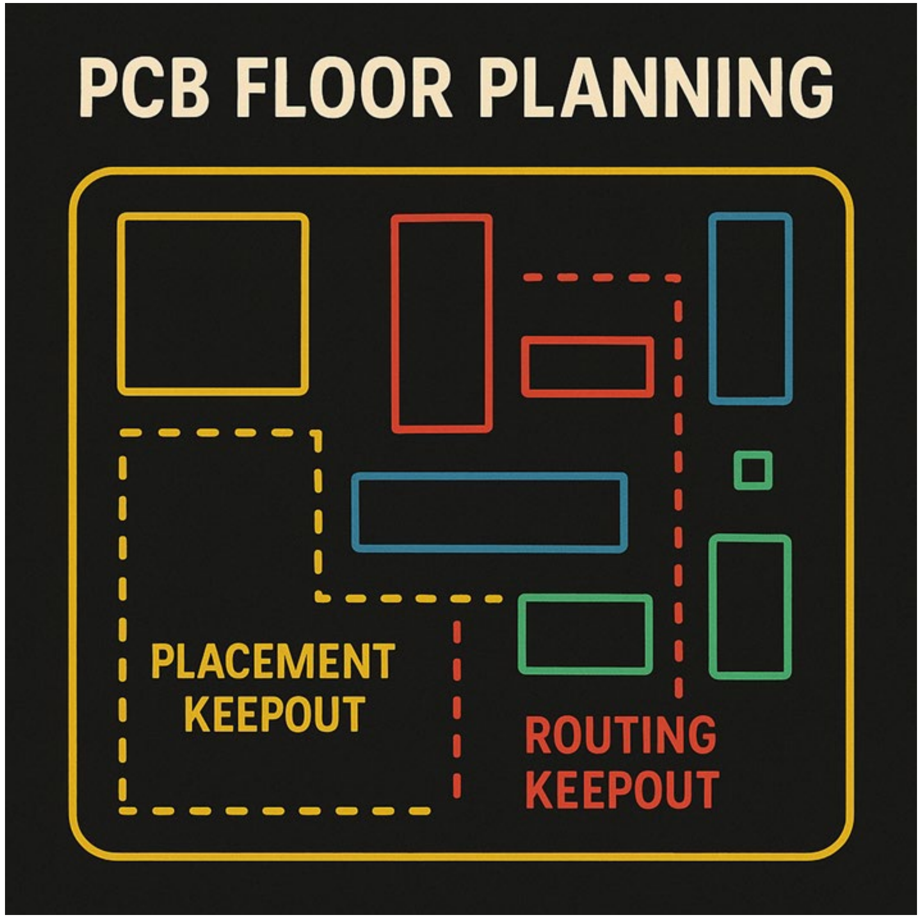
PCB Floor Planning- Best Practices

- Keep Traces Short and Direct
  - Best Practice: Short, direct traces reduce EMI and signal delay.
    - Why: Critical for high-speed or sensitive analog signals.
- Use Ground Planes Liberally
  - Best Practice: Fill unused areas with copper connected to ground.
    - Why: Reduces EMI, improves return path quality, and enhances thermal dissipation.
- Consider Routing Layers Early
  - Best Practice: Plan which layers carry which types of signals (e.g., top = signal, bottom = ground).
    - Why: Avoids conflicts and simplifies layer management in Fusion.



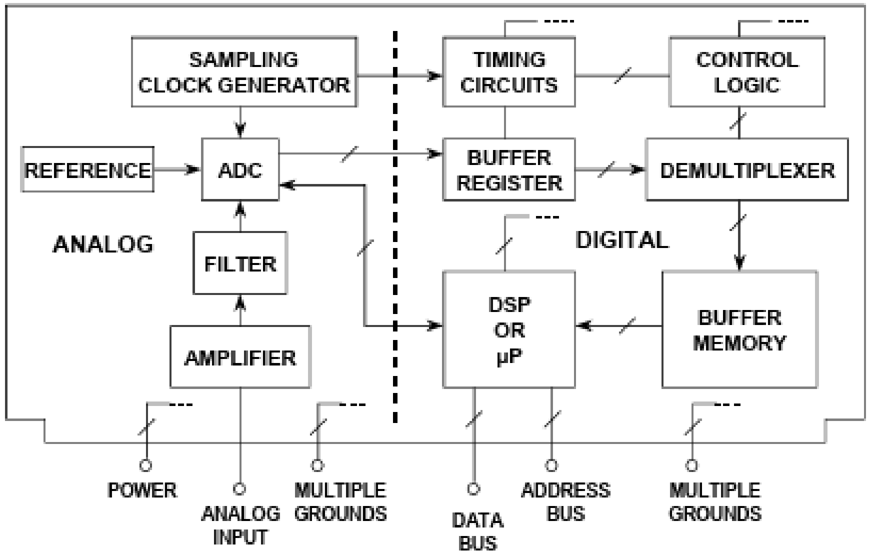
PCB Floor Planning- Best Practices

- Separate Analog and Digital Sections
  - Best Practice: Keep analog and digital components and grounds separated where possible.
    - Why: Prevents digital noise from corrupting sensitive analog signals.
- Plan for Decoupling Capacitors
  - Best Practice: Place bypass capacitors close to power pins of ICs.
    - Why: Filters power supply noise, improves IC stability.
- Reserve Mechanical and Keepout Areas
  - Best Practice: Add mechanical outlines and keepout zones early in the design.
    - Why: Prevents layout conflicts and ensures mechanical compatibility.
- Leave Space for Debugging
  - Best Practice: Leave test points and pads for key signals.
    - Why: Essential for testing and troubleshooting prototypes.



Partitioning vs. Floor Planning

- Relationship Between Partitioning and Floor Planning:
  - Partitioning comes first (logical grouping), then floor planning implements the partitioned blocks physically.
  - Partitioning defines what should be separated, and floor planning defines where and how to separate it on the board.



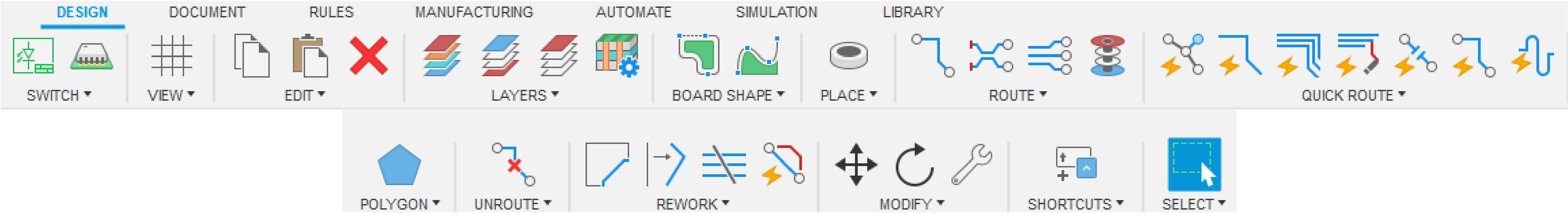
AI Minute

- Please type the following prompts into the AI Tool of your choice, Chat GPT, Gemini, Grok, Copilot, etc…

  - **On a PCB, what are keepout zones and why are they used?**
  - **For PCB Floor Panning, create a methodical procedure to determine where to place various components on a PCB.**

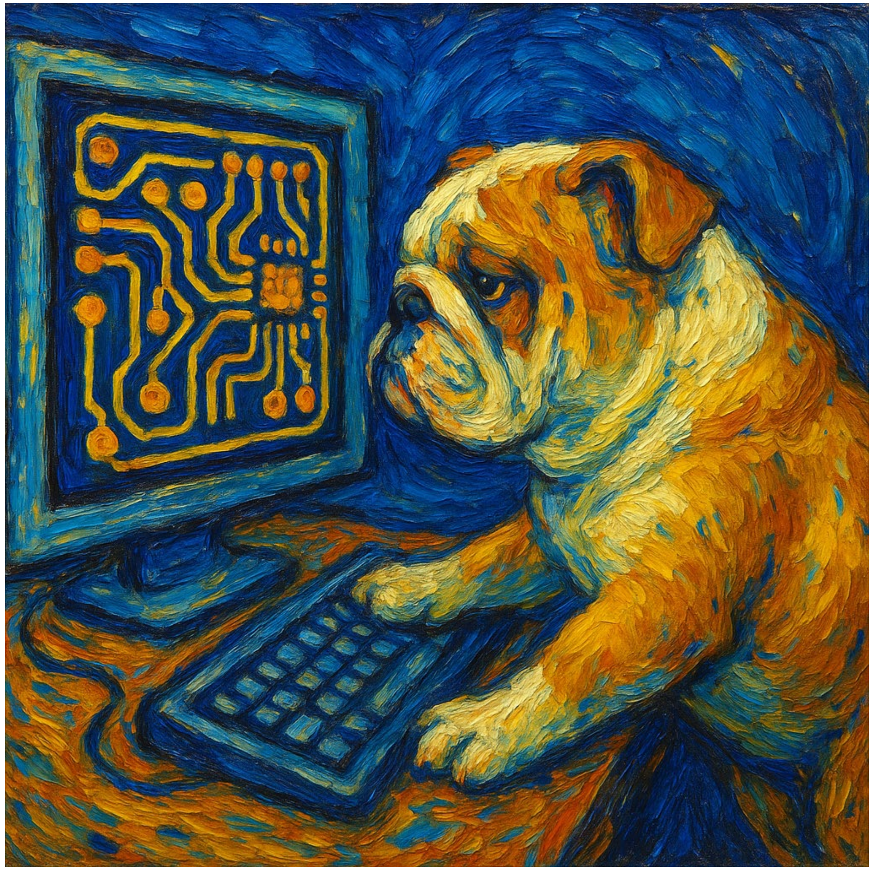
The Fusion PCB Layout Environment

- PCB Layout Tool Navigation



PCB Autorouting

- Create a new Fusion Electrical Project
- Link the Amplifier schematic
  - Remember to click the “Copy” box so you don’t change the original schematic
- Save and name project, e.g. “Amplifier_AutoRoute”
- Switch to PCB View and place components on the PCB
- Select the AutoRoute Command
- Disable viewing of Values layer to make the silkscreen less cluttered



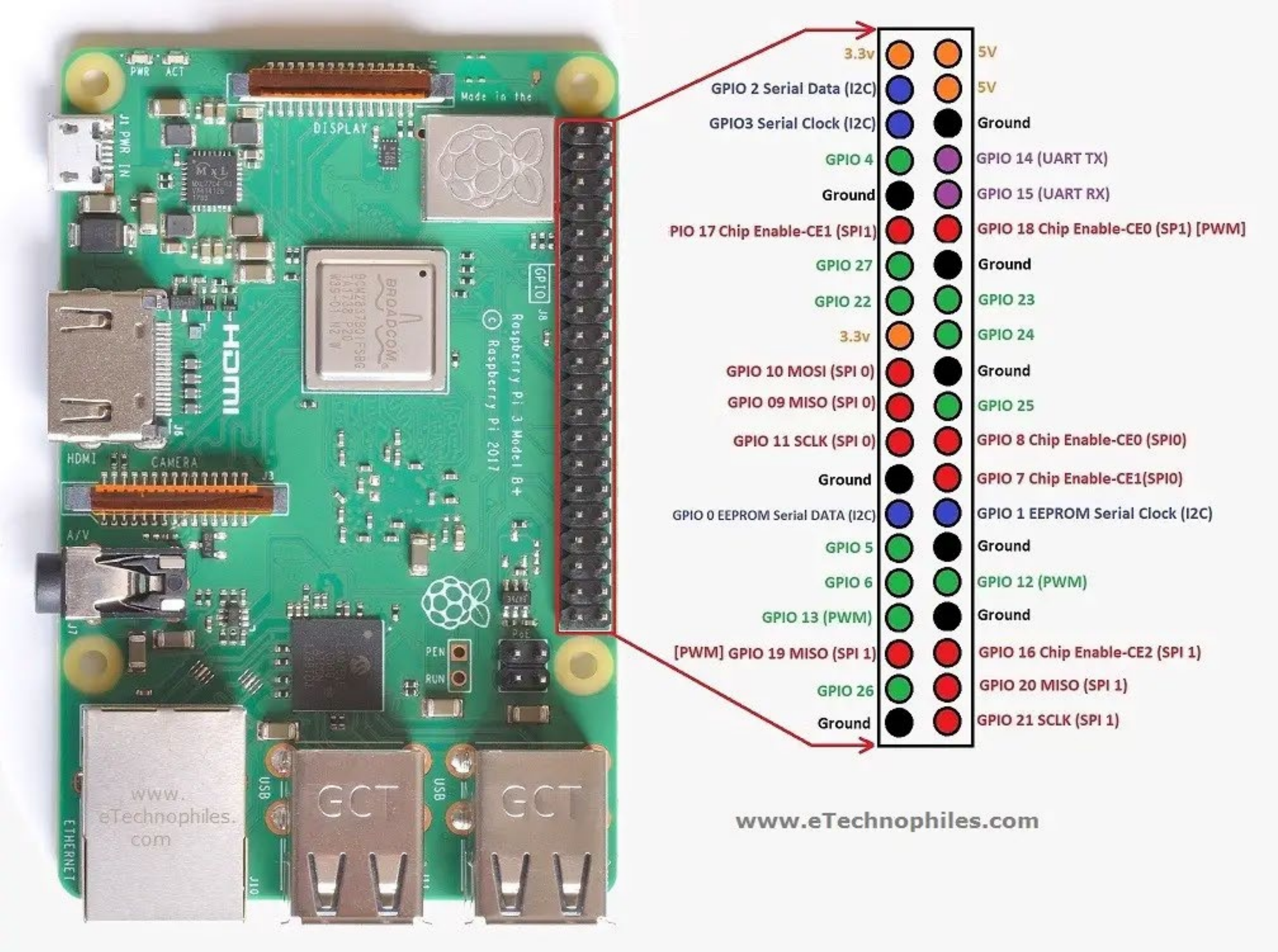
AI Minute

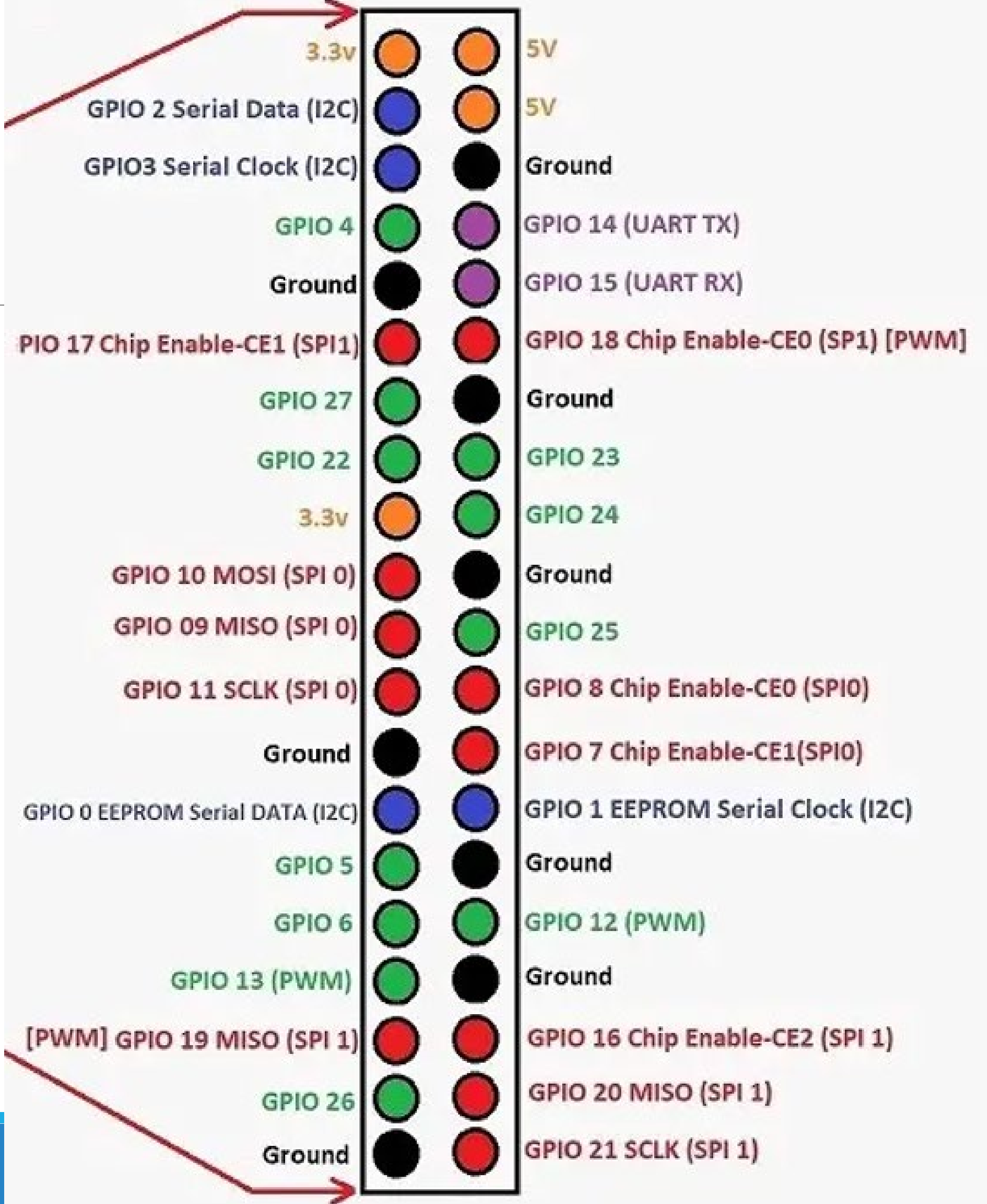
- Please type the following prompts into the AI Tool of your choice, Chat GPT, Gemini, Grok, Copilot, etc…

  - **In AutoDesk Fusion Electrical, can you describe all of the options for the "direction" of the pin under pin properties? What direction would you use for a 5v power supply? What direction would you use for ground? Some of the directions include nc, io, sup, pwr.**

Raspberry Pi Pinout- Create Library Component- PCB Footprint

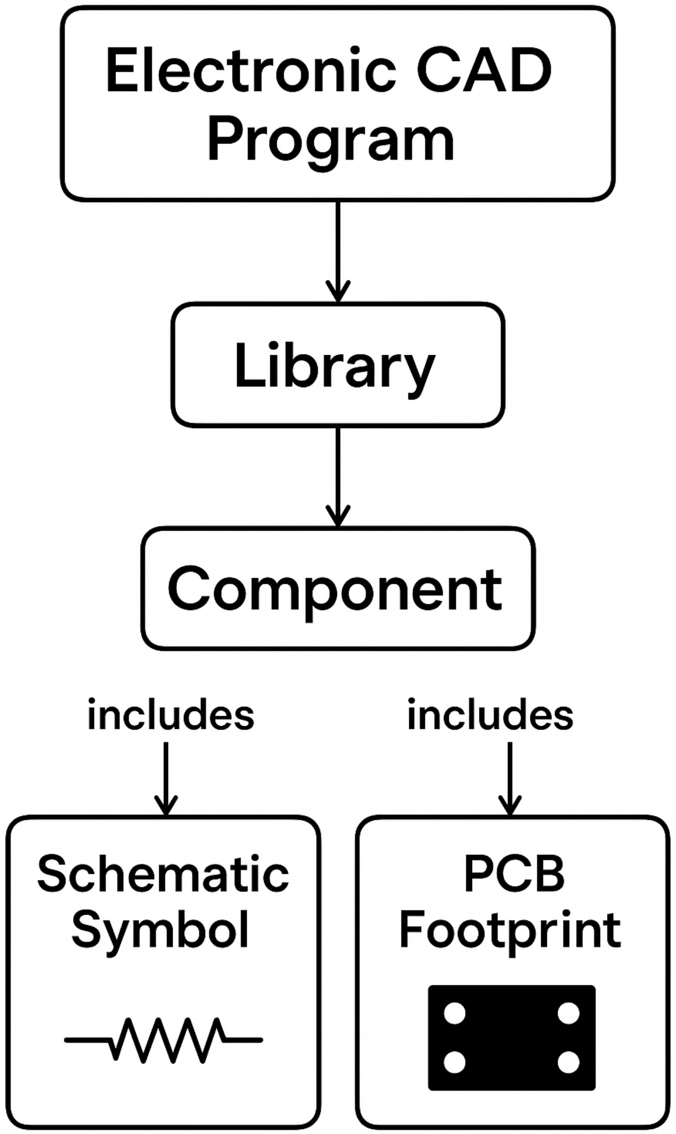
- Component Creation
  - Create Schematic Symbol
  - Create PCB Footprint
  - Combine Footprint and Symbol into a Component
- Create a new project
- Place the newly created Raspberry Pi I/O connector component on the schematic and run ERC
- Switch to PCB and place the component on the PCB
- Adjust the PCB outline to be a more appropriate size for the connector




3.3v
5V
GPIO 2 Serial Data (I2C)
5V
GPIO3 Serial Clock (I2C)
Ground
GPIO 4
GPIO 14 (UART TX)
Ground
GPIO 15 (UART RX)
PIO 17 Chip Enable-CE1 (SPI1)
GPIO 18 Chip Enable-CE0 (SP1) [PWM]
GPIO 27
Ground
GPIO 22
GPIO 23
3.3v
GPIO 24
GPIO 10 MOSI (SPI 0)
Ground
GPIO 09 MISO (SPI 0)
GPIO 25
GPIO 11 SCLK (SPI 0)
GPIO 8 Chip Enable-CE0 (SPI0)
Ground
GPIO 7 Chip Enable-CE1(SPI0)
GPIO 0 EEPROM Serial DATA (I2C)
GPIO 1 EEPROM Serial Clock (I2C)
GPIO 5
Ground
GPIO 6
GPIO 12 (PWM)
GPIO 13 (PWM)
Ground
[PWM] GPIO 19 MISO (SPI 1)
GPIO 16 Chip Enable-CE2 (SPI 1)
GPIO 26
GPIO 20 MISO (SPI 1)
Ground
GPIO 21 SCLK (SPI 1)

CAD Library Elements

- Libraries
  - Libraries contain components
- Components
  - Components include:
    - A Schematic Symbol
    - A PCB Footprint
    - A 3D Model



Questions?