MP3 Processor Design

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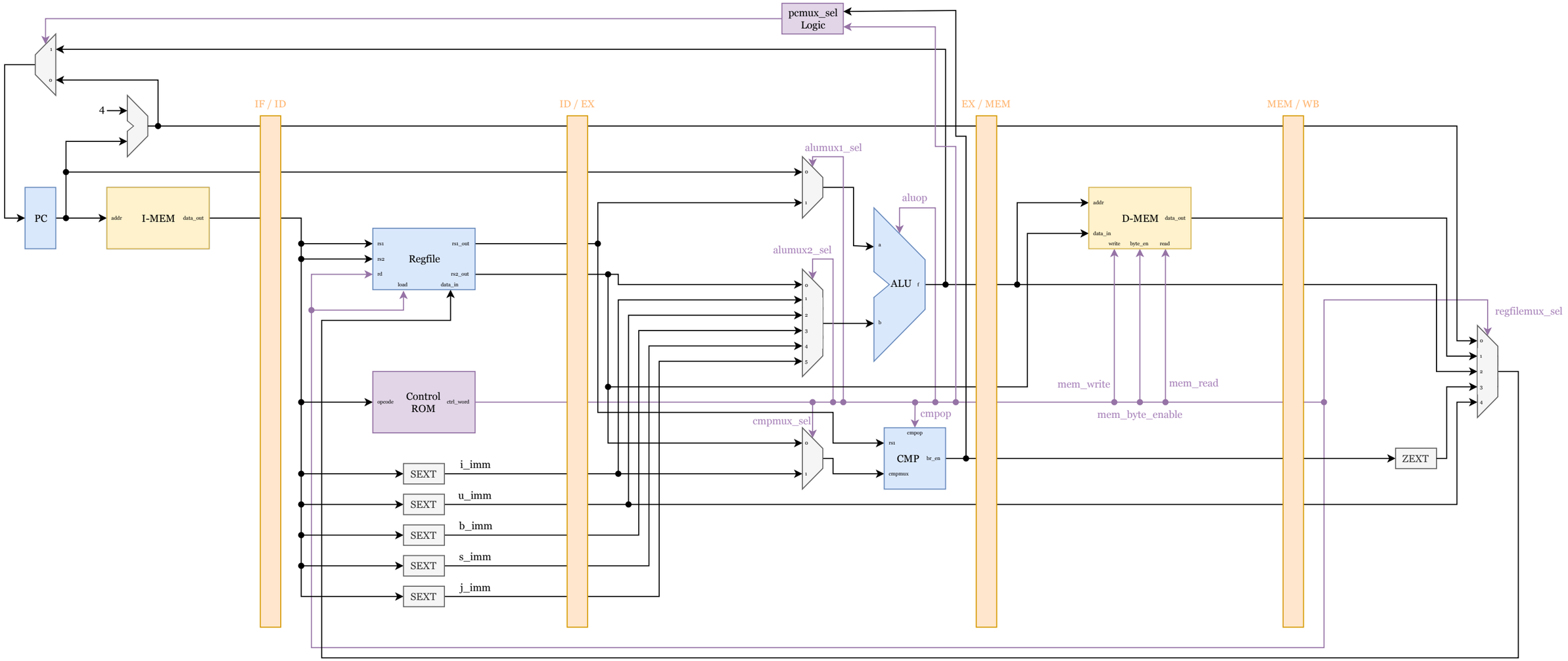
Internal Control Signals

pcmux_sel	(JAL/R || (BR && br_en)) ? {alu_out[31:2], 2'b0} : pc_plus_4
load_regfile	default: 0 reg | load: 1
aluop	default: funct3 auipc, jal, jalr, br, add, load, store: alu_add sr & funct7[5] (reg or imm): alu_sra sr & ~funct7[5] (reg or imm): alu_srl
alumux1_sel	default: rs1_out auipc | jal: pc_out
alumux2_sel	default: rs2_out jal: j_imm store: s_imm jalr, load, sr, other_imm: i_imm auipc: u_imm
cmpmux_sel	default: rs2_out slt, sltu (imm): i_imm
cmpop	default: funct3 beq: == bne: != blt, slt (reg or imm): $signed(rs1_out) < $signed(cmpmux_out) bge: $signed(rs1_out) >= $signed(cmpmux_out) bltu, sltu (reg or imm): rs1_out < cmpmux_out bgeu: rs1_out >= cmpmux_out
regfilemux_sel	default: alu_out lui: u_imm jal | jalr: pc_plus_4 slt, sltu (reg or imm): br_en load: lb/lh/lw/lbu/lhu (according to funct3)
mem_read	default: 0 load: 1
mem_write	default: 0 store: 1
mem_byte_enable	default: 4'b1111 sb: unique case (mem_addr_mod_4) 2'b00: mem_byte_enable = 4'b0001; 2'b01: mem_byte_enable = 4'b0010;

	2'b10: mem_byte_enable = 4'b0100; 2'b11: mem_byte_enable = 4'b1000; endcase sh: (mem_addr_mod_4 == 2'b00)? mem_byte_enable = 4'b0011 : mem_byte_enable = 4'b1100 sw: mem_byte_enable = 4'b1111;


pcmux_sel
Logic
IF / ID
ID / EX
EX / MEM
MEM / WB
4
PC
addr
I-MEM
data_out
Regfile
rs1
rs2
rd
rs1_out
rs2_out
load
data_in
Control
ROM
opcode
ctrl_word
SEXT
i_imm
u_imm
b_imm
s_imm
j_imm
alumux1_sel
alumux2_sel
aluop
ALU
a
b
f
cmpmux_sel
cmpop
CMP
rs1
cmpmux
br_en
D-MEM
addr
data_in
data_out
write
byte_en
read
mem_write
mem_read
mem_byte_enable
ZEXT
regfilemux_sel